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Si and InP Integration in the HELIOS project

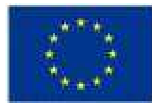
J.M. Fedeli

CEA-LETI, Grenoble (France)

ECOC 2009

Basic information about HELIOS

HELIOS
pHotonics ELectronics functional Integration on CMOS



www.helios-project.eu

- Large-scale integrating project (IP)
- Start date: 1 May 2008
- Duration: 48 months
- Total budget: 12 M€
- Total EC funding: 8.5 M€
- Consortium: 19 partners

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Objectives of HELIOS project

- Build a complete design and fabrication chain enabling the integration of a photonic layer with a CMOS circuit, using microelectronics fabrication processes.
- Development of high performance generic building blocks that can be used for a broad range of applications:
  - WDM sources by III-V/Si heterogeneous integration
  - Fast modulators and detectors,
  - Passive circuits and packaging
- Building and optimization of the whole “food chain” to fabricate complex functional devices.
- Investigation of more promising but challenging alternative approaches for the next generation of devices
- Road mapping, dissemination and training, to strengthen the European research and industry in this field and to raise awareness of new users about the interest of CMOS Photonics.

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Consortium

- Different but complementary skills are requested to fulfill the project objectives:
  - Industrial end-users to drive the project, define the components architecture and specifications

  - III-V industrials to develop III-V on silicon approach, benchmarking

  - CMOS foundries and design tools experts to ensure technological relevance, photonic/electronic convergence and facilitate further exploitation

  - CMOS photonics institutes to develop processes and enable the transfer to foundries

  - Academic laboratories to optimize generic building blocks and develop innovative architectures

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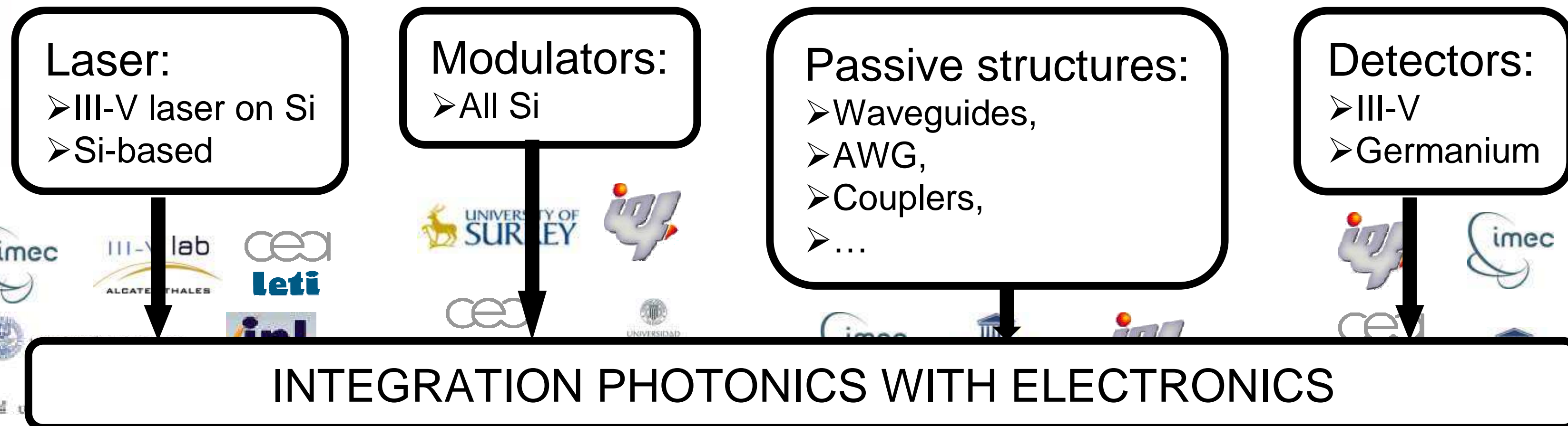
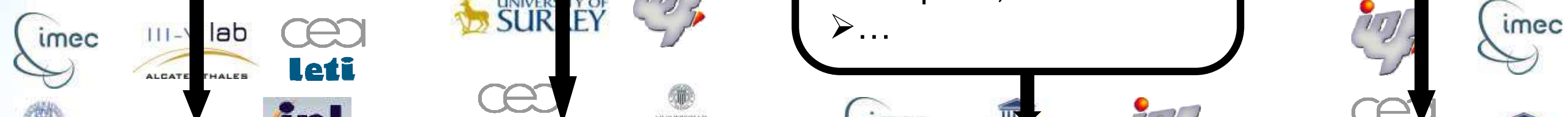
Applications

- The demonstrators and first applications are in the telecom/datacom field
  - 40Gb/s modulator
    - Integration of modulator, PD and drivers
  - 10x10 Gb/s transceiver
  - Mixed analog and digital transceiver module for multifunction antennas
  - Photonic QAM-10Gb/s wireless transmission system





PD: Photodiode
QAM: Quadrature amplitude modulation

Building blocks

Ge on Si			III-V-on-Si
UPS-IEF & LETI	UPS-IEF & LETI		IMEC
PIN	PIN	structure	MSM
~ 20 nA	~ 1 µA	Dark current at -1V	~1 nA
~ 1 A/W	~0.8 A/W	Responsivity	~1 A/W
42 GHz	~ 90 GHz	Bandwidth	-

Detectors:
- III-V
- Germanium

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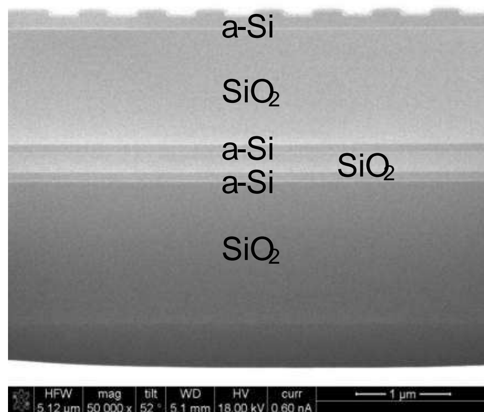
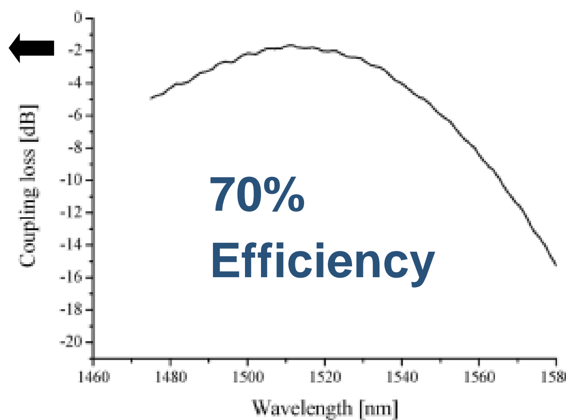
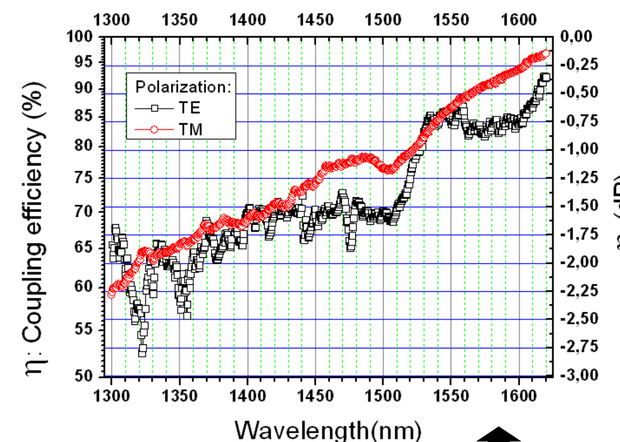
PD: Photodiode
QAM: Quadrature amplitude modulation

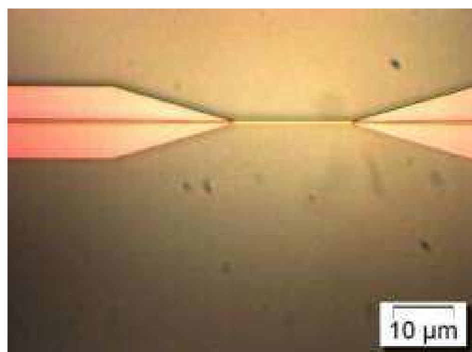
Building blocks





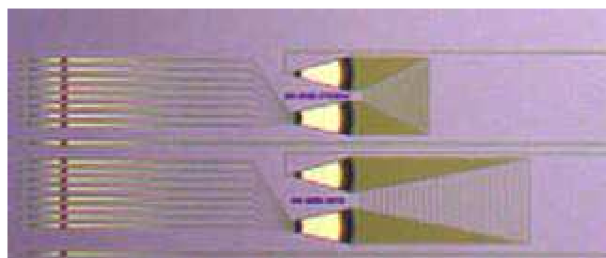
70% Efficiency





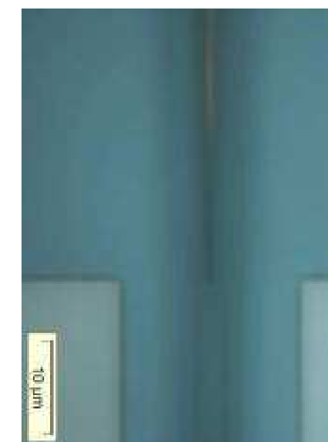
50 µm long transition

Loss: 0.1-0.2 dB at 1470-1580 nm



Passive structures:

- Waveguides,
- AWG,
- Couplers,
- …



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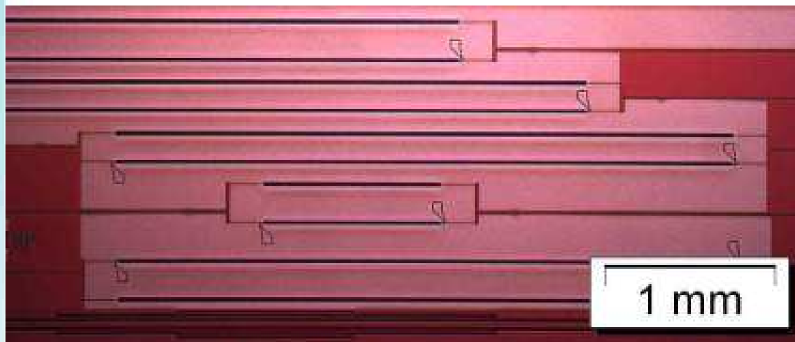
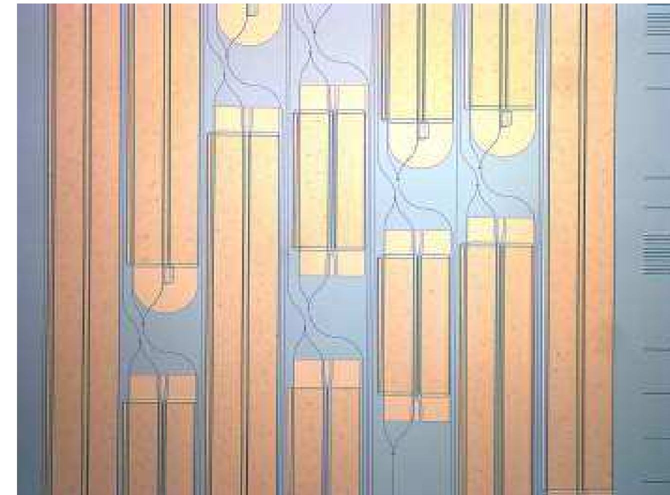
Building blocks





Modulators:
➢All Si

DC results :

- Insertion loss = 5 dB
- Contrast ratio up to 14 dB
- $V_{\pi}L_{\pi}$ = 5 V.cm

RF results

- BP 15GHz

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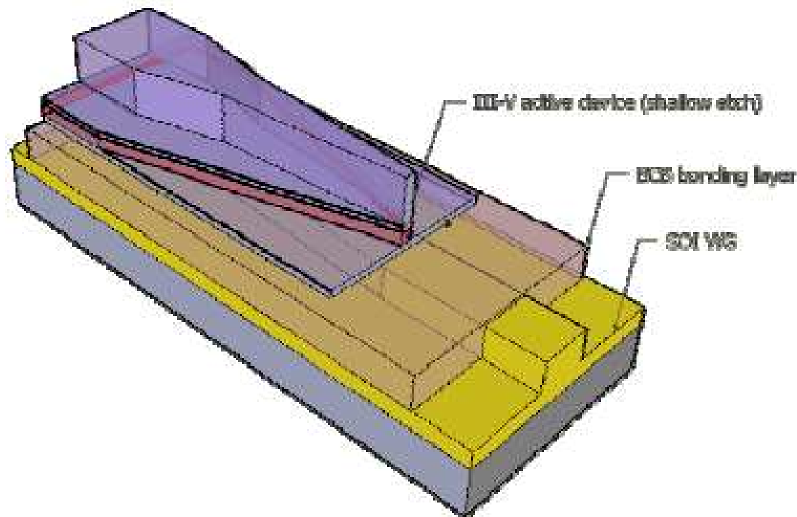
Specifications for laser



Laser:
➢III-V laser on Si

- Hybrid InP on Si
- BCB or SiO2 or ITO molecular bonding
- Multi λ in C-Band
- 3dBm output power min
- Single mode operation
- 30dB SMSR
- CW laser operation at 65℃
- Process on 200mm wafers

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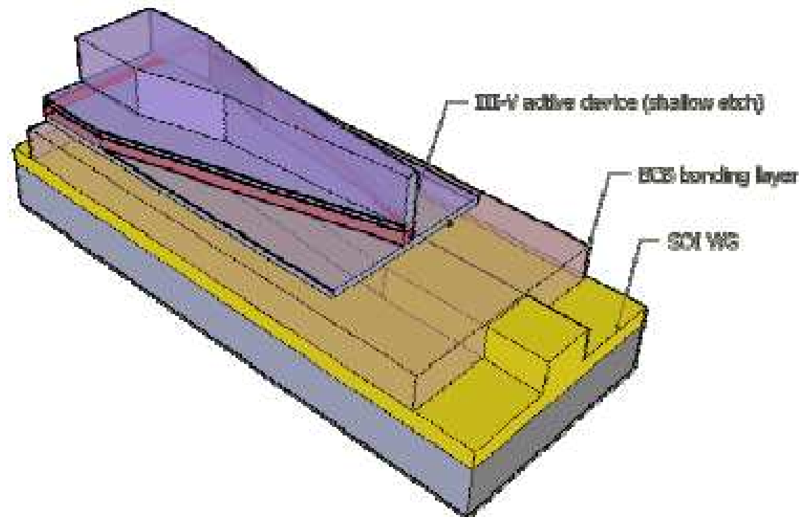
Building blocks developed to enable integration of InP on 200mm silicon wafers:



Laser:
➢III-V laser on Si

- Die-to-wafer SiO2/SiO2 molecular bonding
- Monitoring of contamination
- DUV lithography on die
- InP dry etching on 200mm
- Compatible cladding
- CMOS compatible non alloyed ohmic contacts for both n-type and p-type InP

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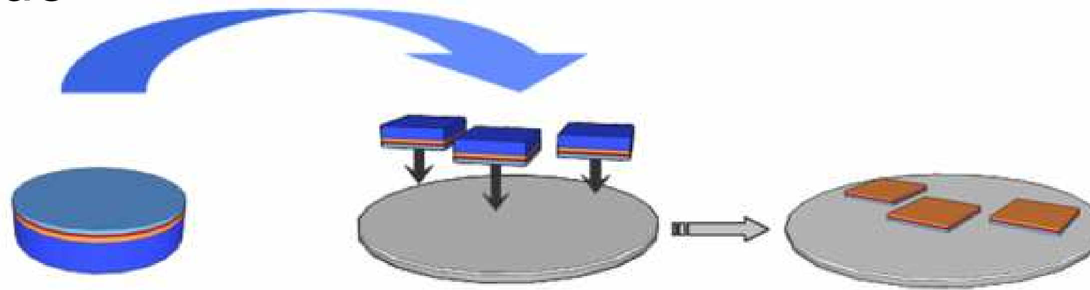
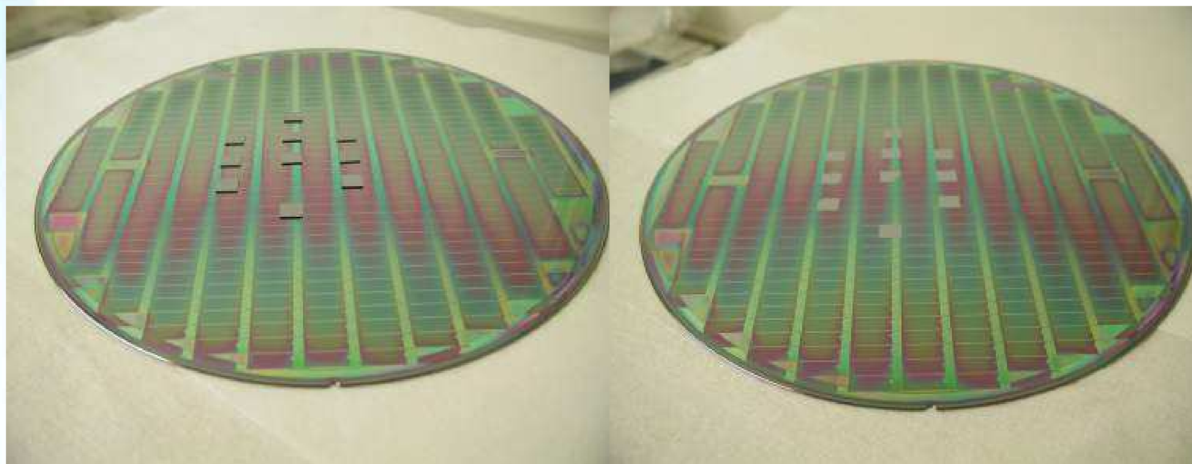
1- Die-to-wafer SiO_2/SiO_2 molecular bonding

- Low T process compatible with microelectronics technologies
- Bonding thickness controlled by CMP of deposited oxide





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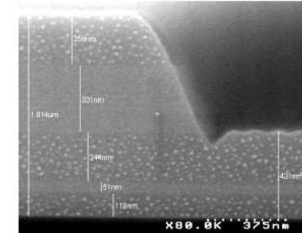
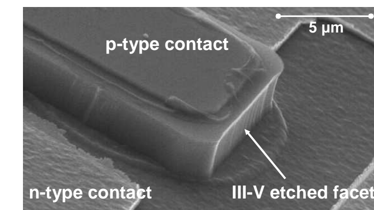
2- Dry etching of InP epilayers bonded on Si

- HBr etching (ICP mode):
  - 45°profiles ☹
  - Trenching ☹



J.M. Fedeli *et al.*, GFP'06

- Cl_2/H_2 (ICP mode):
  - Steep profiles achieved ➔ FP lasers on Si demonstrated ☺
  - Etch rate (~2µm/min) ➔ etch stop on thin epilayer difficult ☹
  - Etching quality very sensitive to the environment ☹
  - SiO_2 around the dice damaged by the plasma ☹



T. Dupont *et al.*,
post dealine paper, IPRM'08

- CH_4/H_2 (RIE mode):
  - Steep profiles ☺
  - Etch rate (~ 100nm/min) ➔ etch either thick or thin epilayers ☺
  - Etching quality not sensitive to environment ☺
    - Polymerization on inert surfaces (SiO_2,Si_3N_4,Si)
    - Etching only on InP dice

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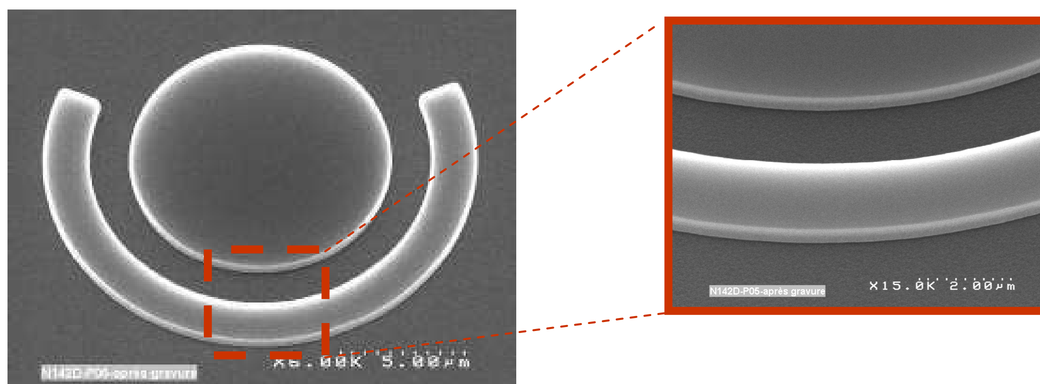
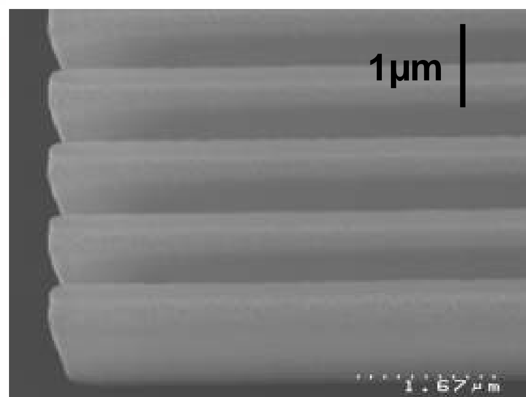
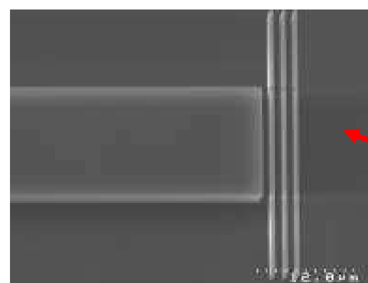
2- Dry etching of InP epilayers bonded on Si

- CH_4/H_2 (200W, 100mtorr, 40sccm, 20% CH_4) + O_2
  - Thin (400nm) InP microdisks. Steep profiles. No underetching

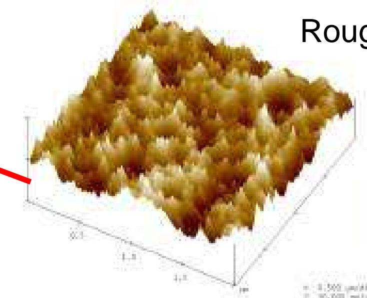


  - Thick (3.5µm) structures. High aspect ratios obtained.





AFM 2x2µm2
Roughness = 4nm rms



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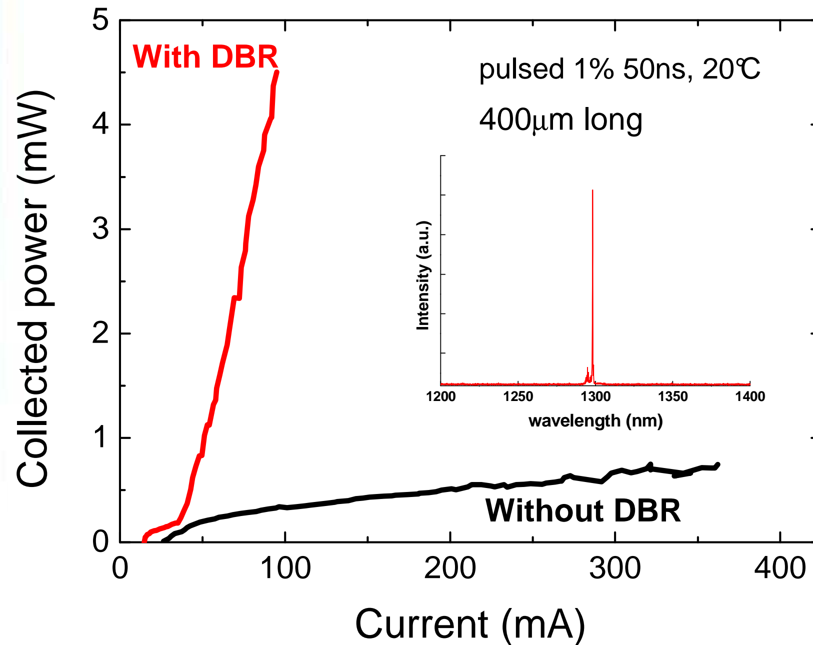
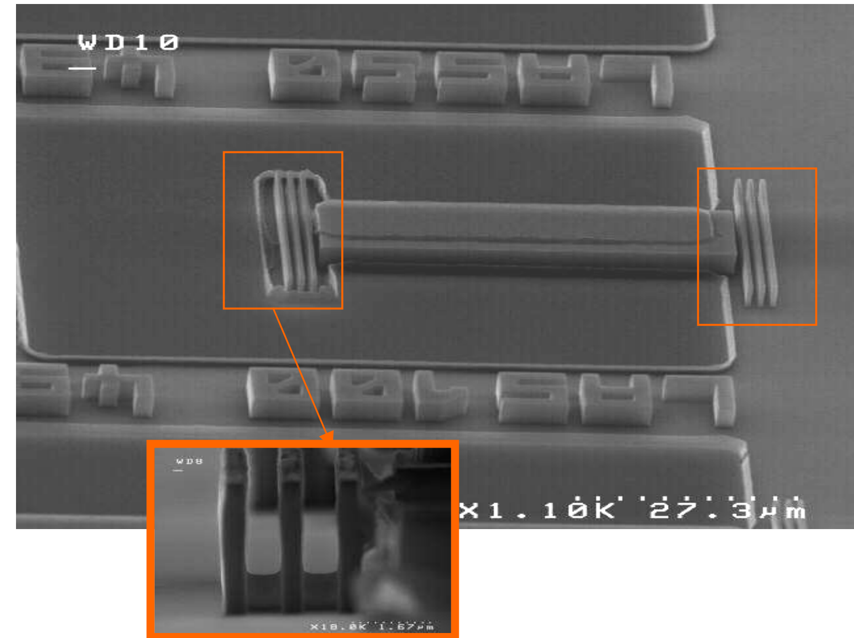
2 – Etched facets DBR lasers on silicon

- AlGaInAs active layer – 1.3µm
- individual die processed
  - $CH_4/H_2/O_2$ dry etching
  - metallization + lift-off





- pulsed operation at RT:
  - L = 400µm, 200µm
  - λ = 1.3µm
  - P > 4 mW

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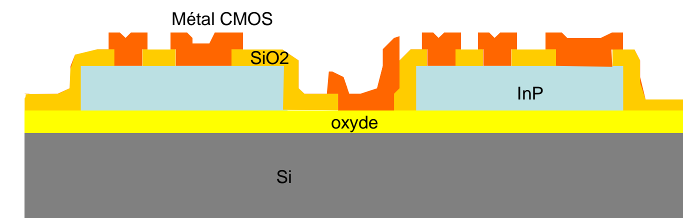
3 - CMOS compatible ohmic contacts

- Optoelectronics clean room
  - Gold-based metallization for ohmic contacts
    - Ti/Pt/Au on p-type InGaAs
    - Ni/Ge/Au/Ni/Au on n-type InP
  - Evaporation + lift-off
  - Annealing

- CMOS pilot line
  - Au is forbidden ➔ Ti/TiN/AlCu stack
  - Lift-off not used ➔ Subtracting way
    - Full sheet SiO_2 deposition, DUV litho
    - Oxide etching down to the III-V (TLM pads)
    - Full sheet metal deposition, DUV litho
    - Metal etching down to the oxide



  - InP dice on Si
    - 500nm thick N doped ($5x10^{18}$ cm^{-3}) InP
    - 500nm thick P doped ($3x10^{19}$ cm^{-3}) InGaAs

  - No annealing on the wafers

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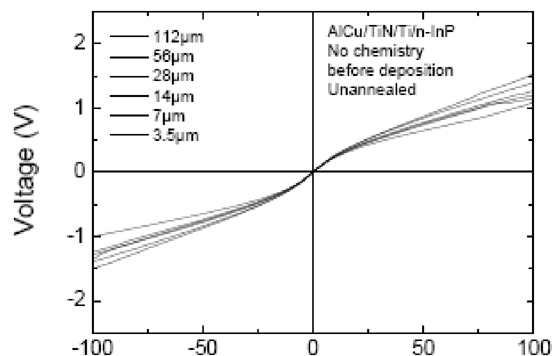
3 - CMOS compatible ohmic contacts

- TLM measurements on un-annealed dice

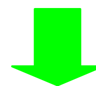
N doped-InP



$Rc = 1x10^{-4}\ \Omega.cm^2$

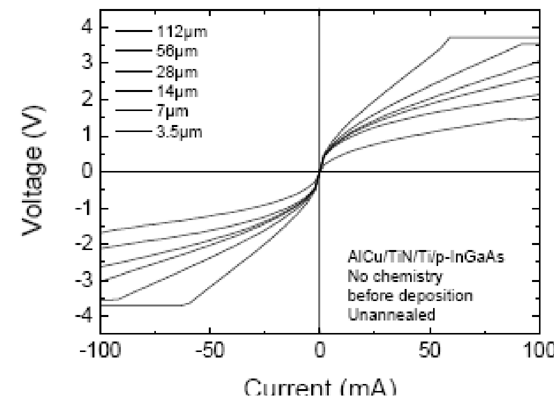
Schottky behavior

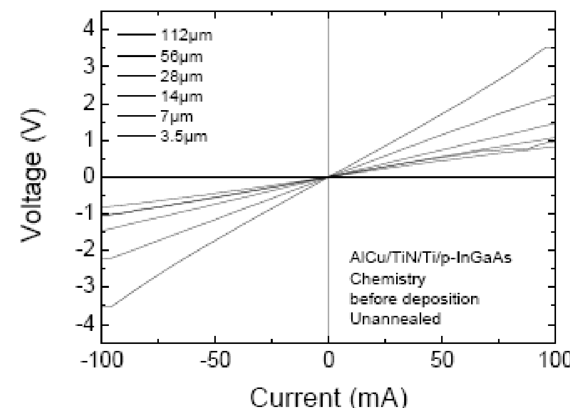
+ surface preparation



Ohmic behavior

P doped-InGaAs

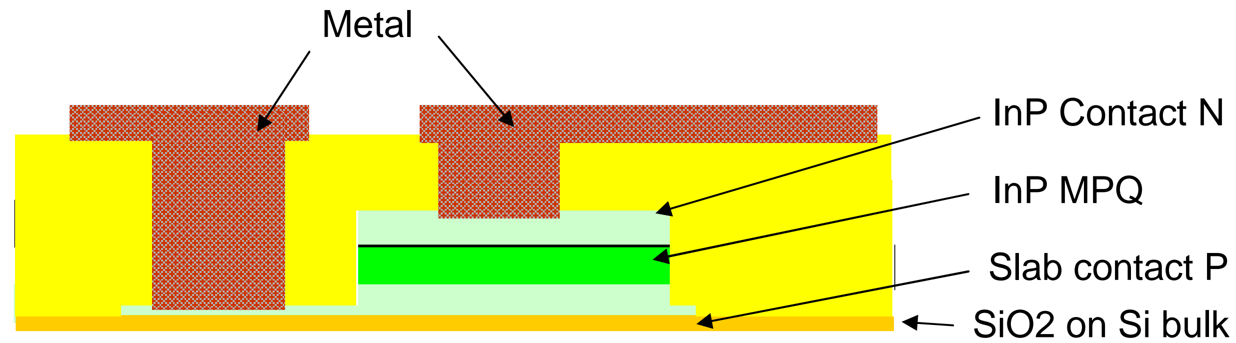


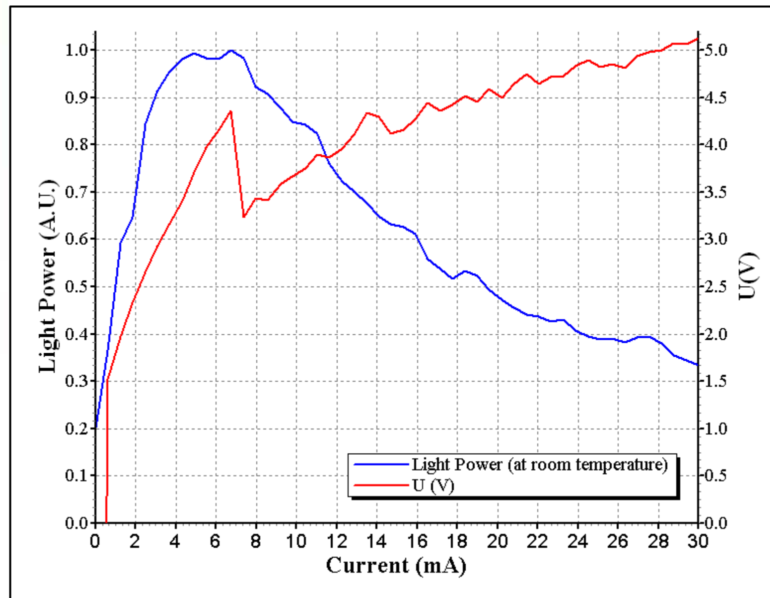


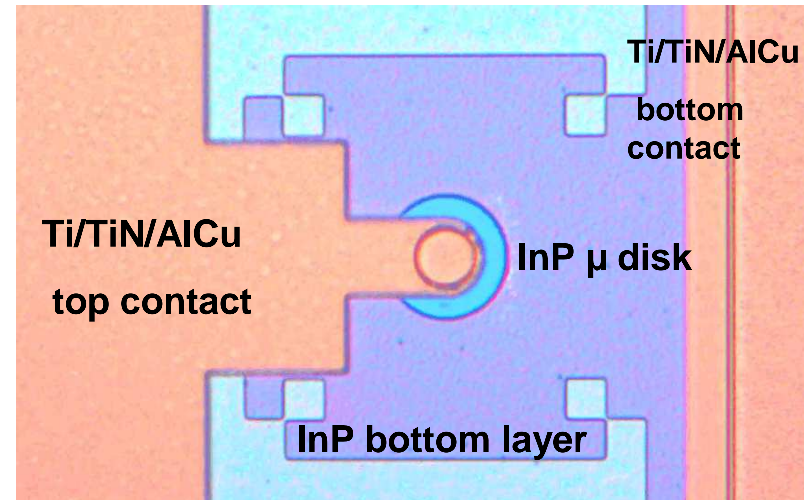
$Rc = 6x10^{-5}\ \Omega.cm^2$

Same metallization step ➔ non alloyed ohmic contacts on both p and n type materials

InP LED on Si fabricated in a 200mm EIC fab







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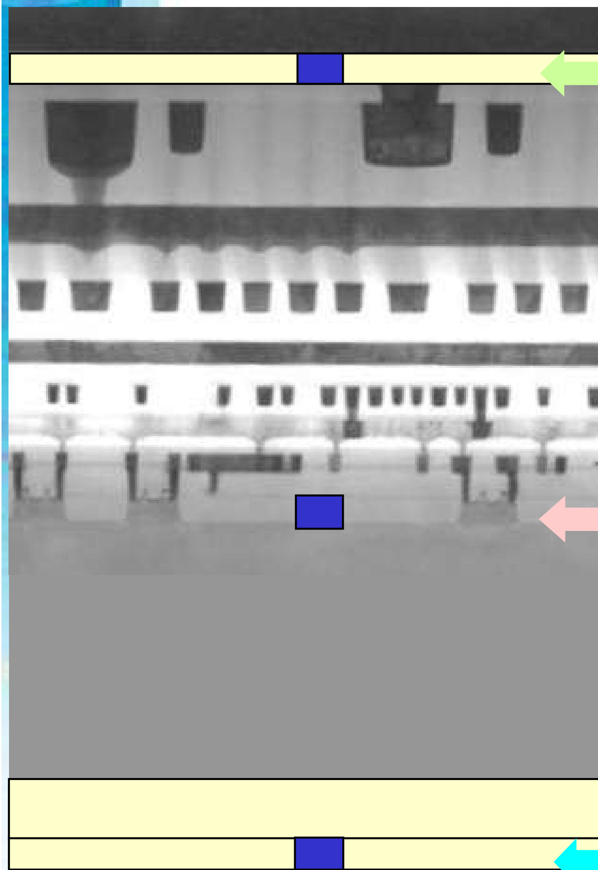
Integration of complex photonic functions with EIC



Photonic layer at the last levels of metallizations with back-end fabrication

1) Wafer bonding of PIC (high T℃)

2) BE fab(<400℃)

- Use of standard FE CMOS technologies
- Heterogeneous integration of III-V on Si
- High integration density (AboveIC)
- Multilevel process capability

Combined front-end fabrication

- Specific FE CMOS technology and library
- Flip-Chip hybridization of InP components
- Moderate integration density
- Efficient connections of EIC and PIC

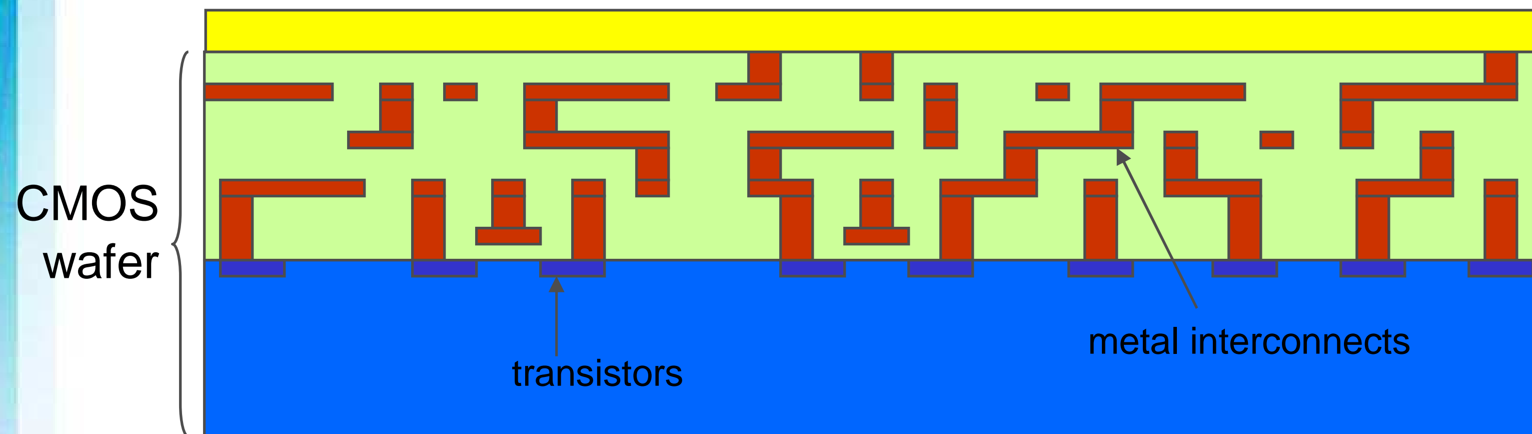
Backside fabrication

- BE fab(<400℃) or FE fab with wafer bonding
- Through substrate connections
- High integration density
- Heterogeneous integration of III-V on Si

BE: Back end FE:Front end

Step1: CMOS top layers preparation

- CMOS wafer planarized
- Deposition of SiO2 layer for bonding



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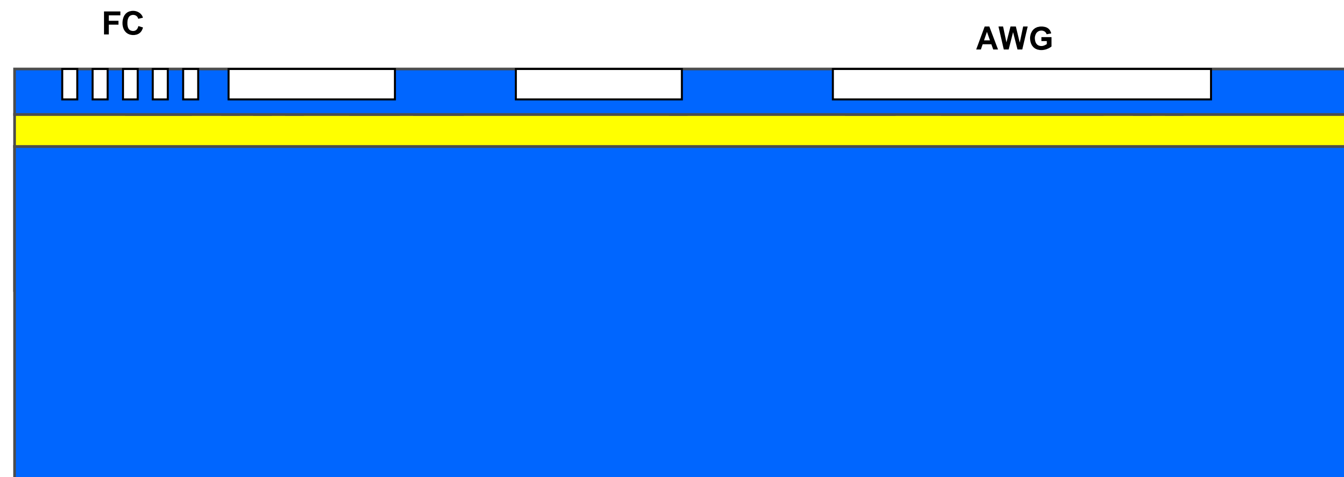
Step 2: Passive Silicon Photonic layer

- Litho 248nm of gratings, partial Si etch, stripping
- HMask deposition
- Litho 193nm of waveguide, etch HM, stripping, etch Si to the box



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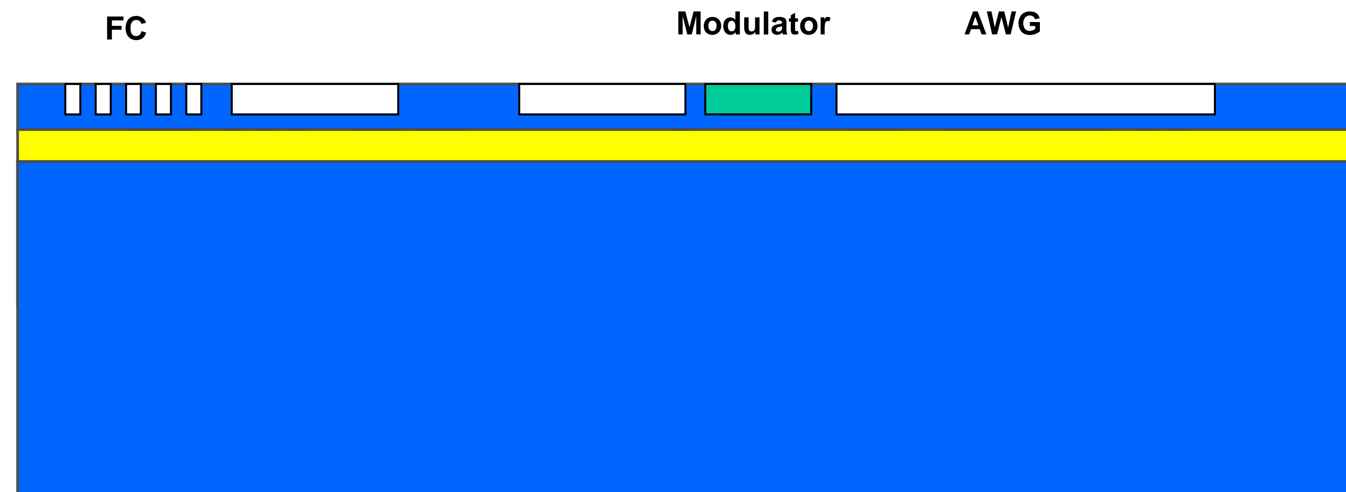
Step 3: Modulator Processing

- Lithos for implantation
- Different implantations
- Annealing



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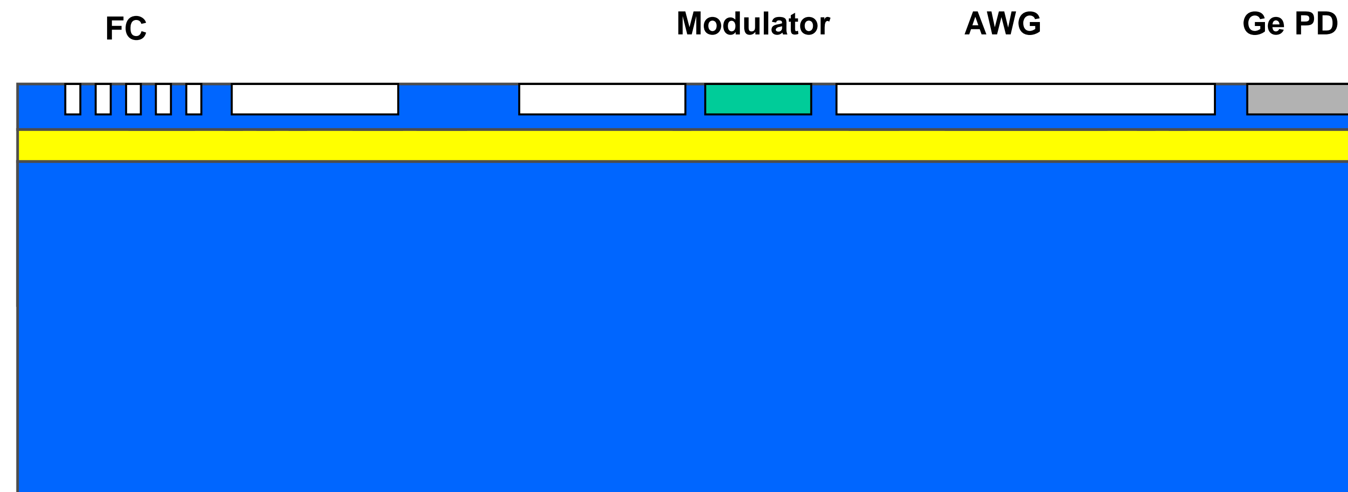
Step 4: Ge photodetector Processing

- Cavity formation
- Ge epitaxy in cavity
- P & N Implant



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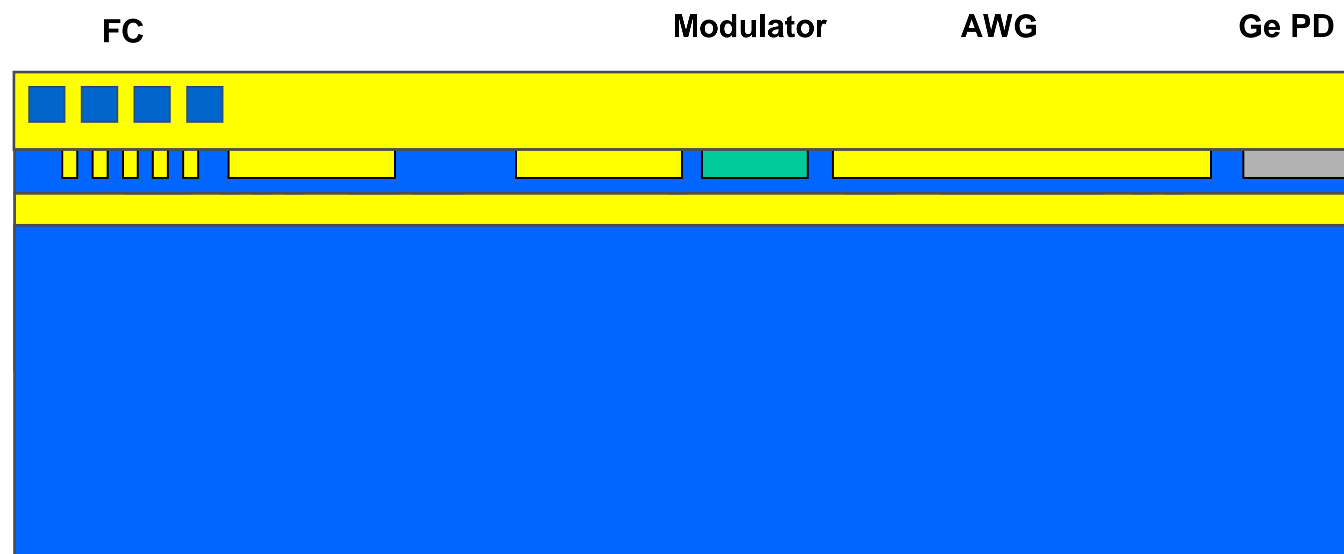
Step 5: Mirror & Planarization

- Fabrication of mirror
- Planarization



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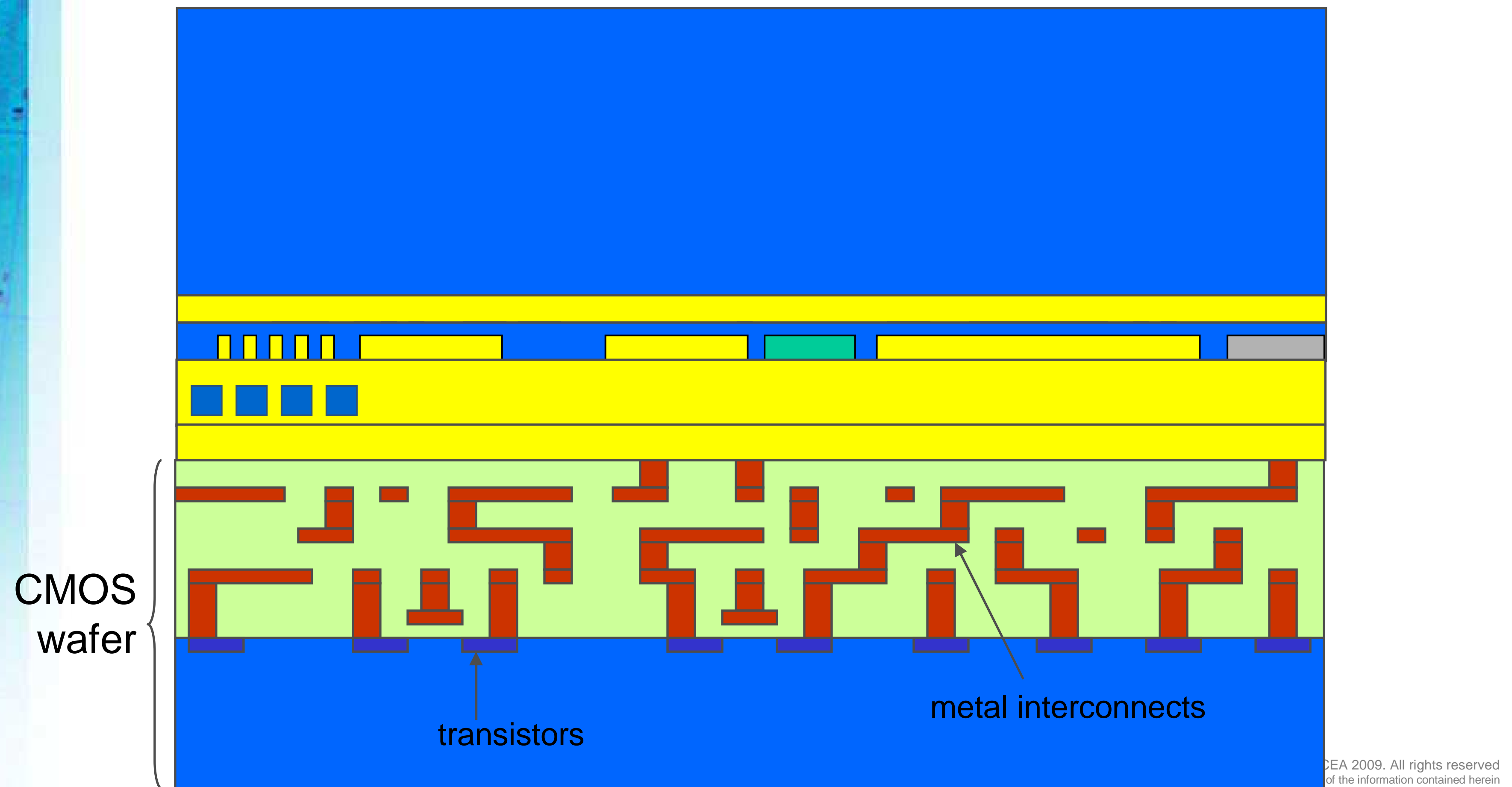
Step 6: Molecular wafer bonding

- Alignement of the two wafers (+-2µm) and bonding of photonic wafer on CMOS wafer



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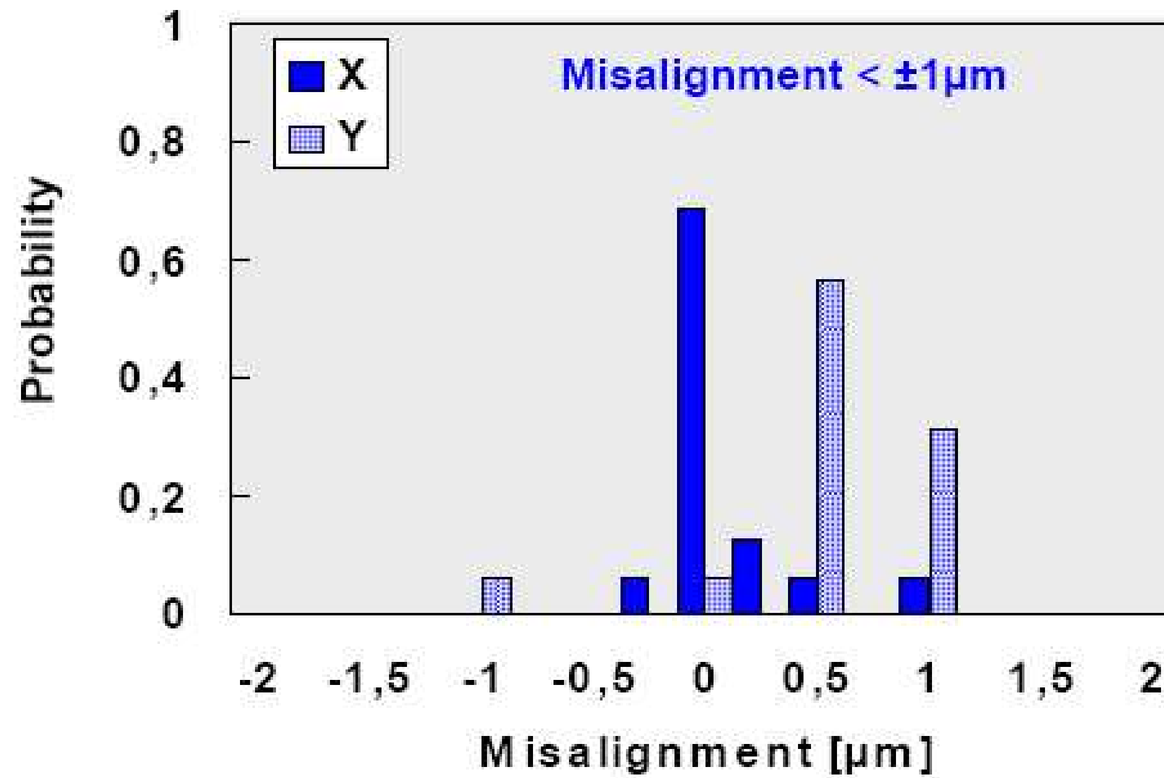
Alignment accuracy (wafer-to-wafer bonding)



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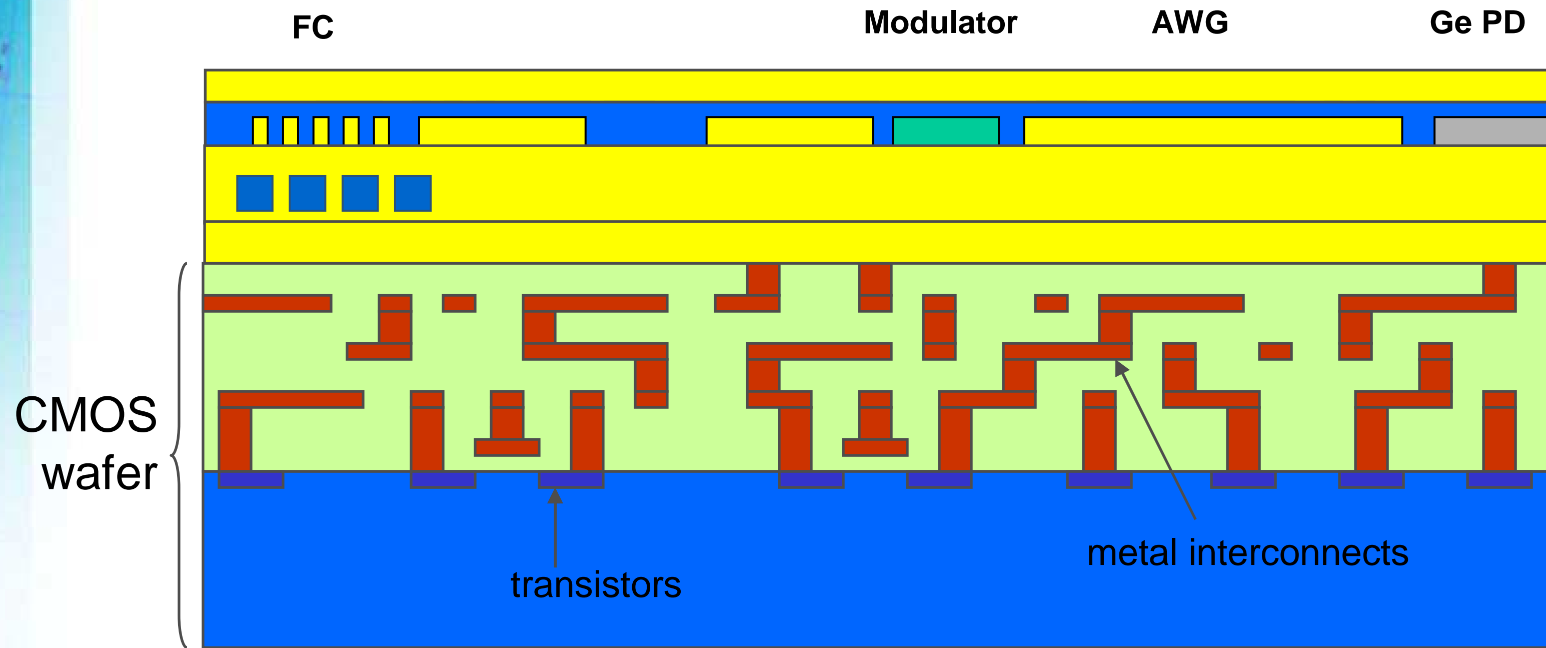
Step 7: Si Substrate removal

- Mechanical grinding
- Si chemical etching



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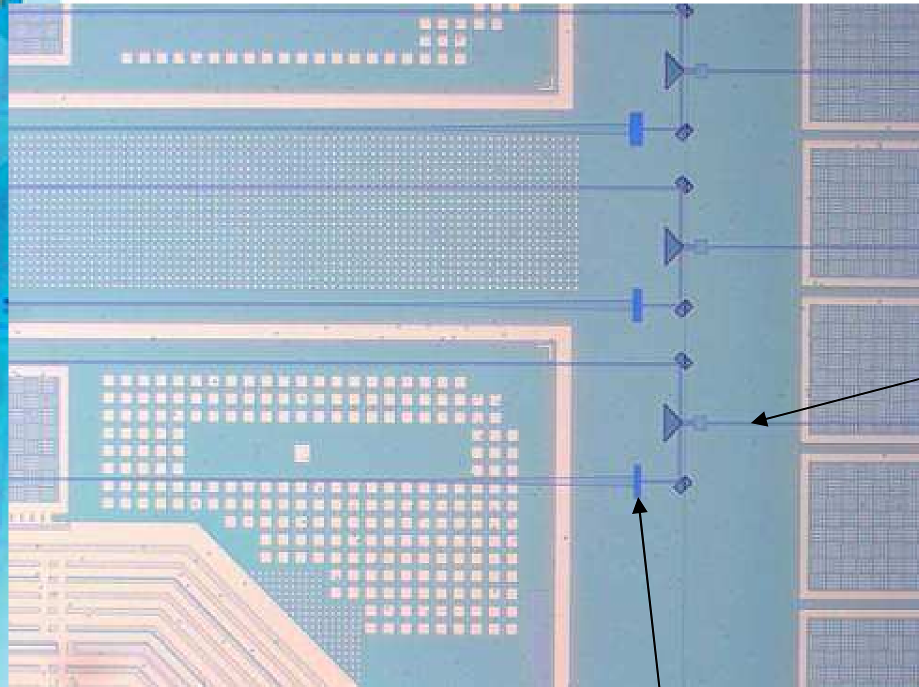
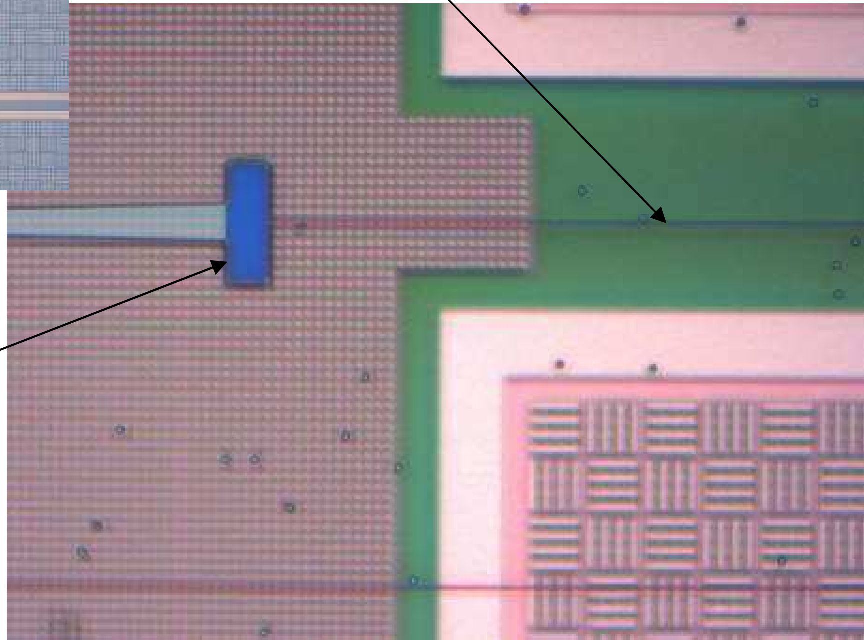
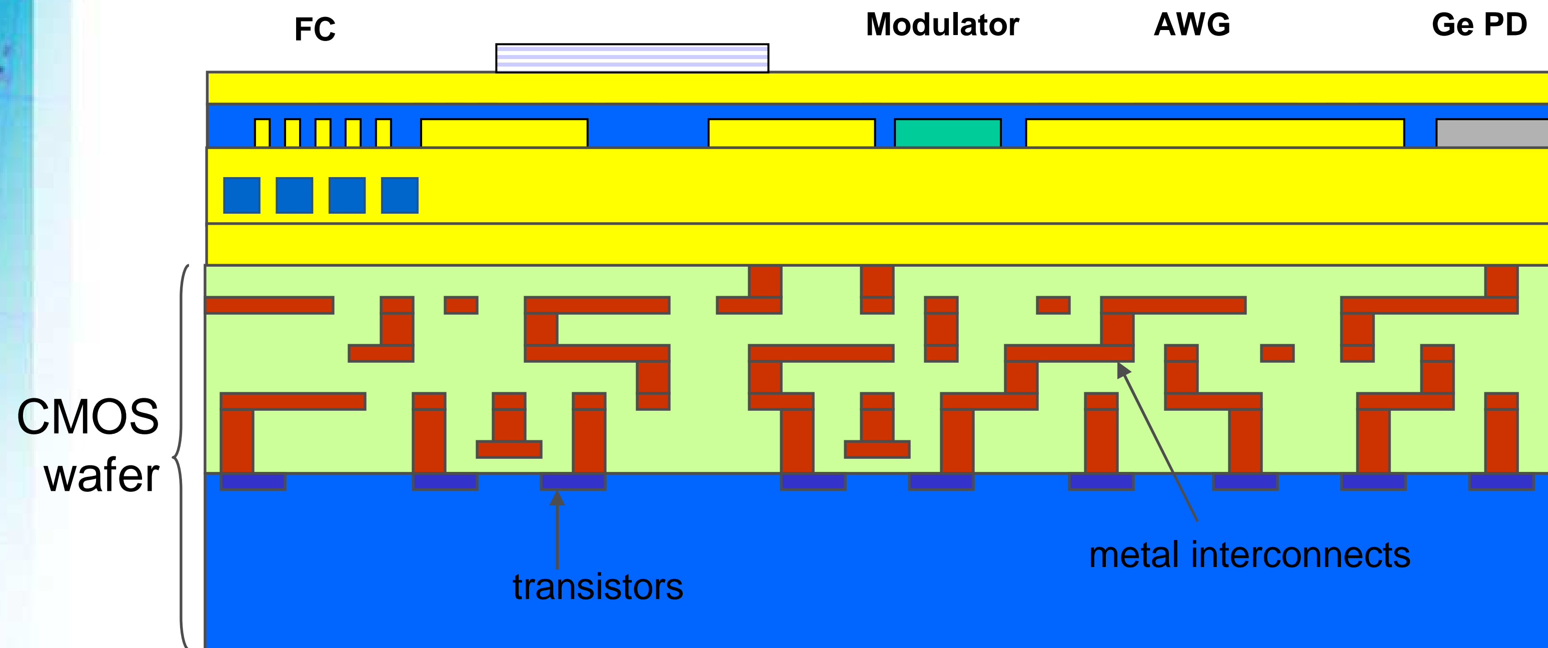
SOI wafer bonded on a CMOS wafer





Step 8: InP heterostructure bonding

- Bond small InP dice with herostructure on the remaining BOX
- InP substrate removal of the dies



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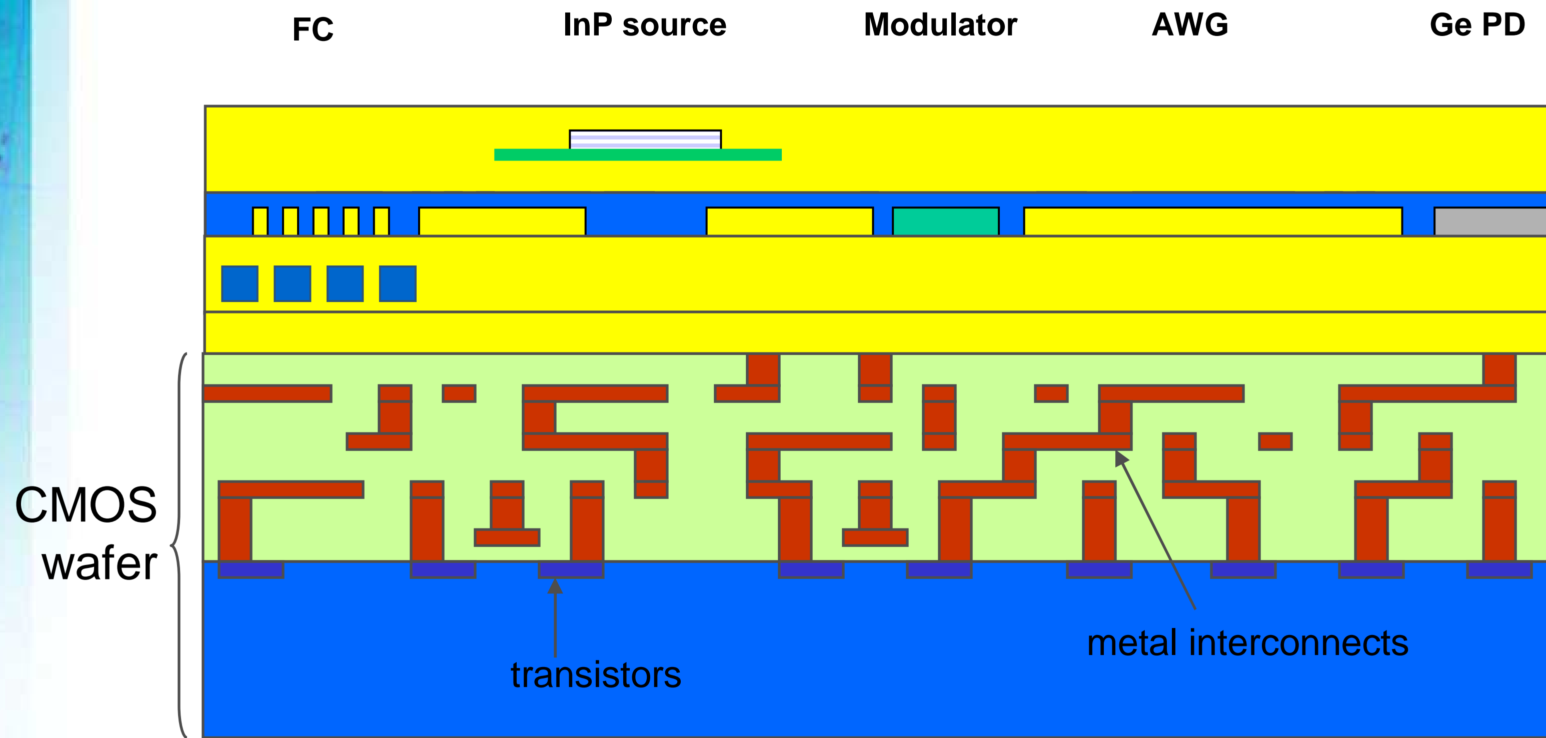
Step 9: InP heterostructure process

- Process InP source (InP etching)
- Planarized with SiO2



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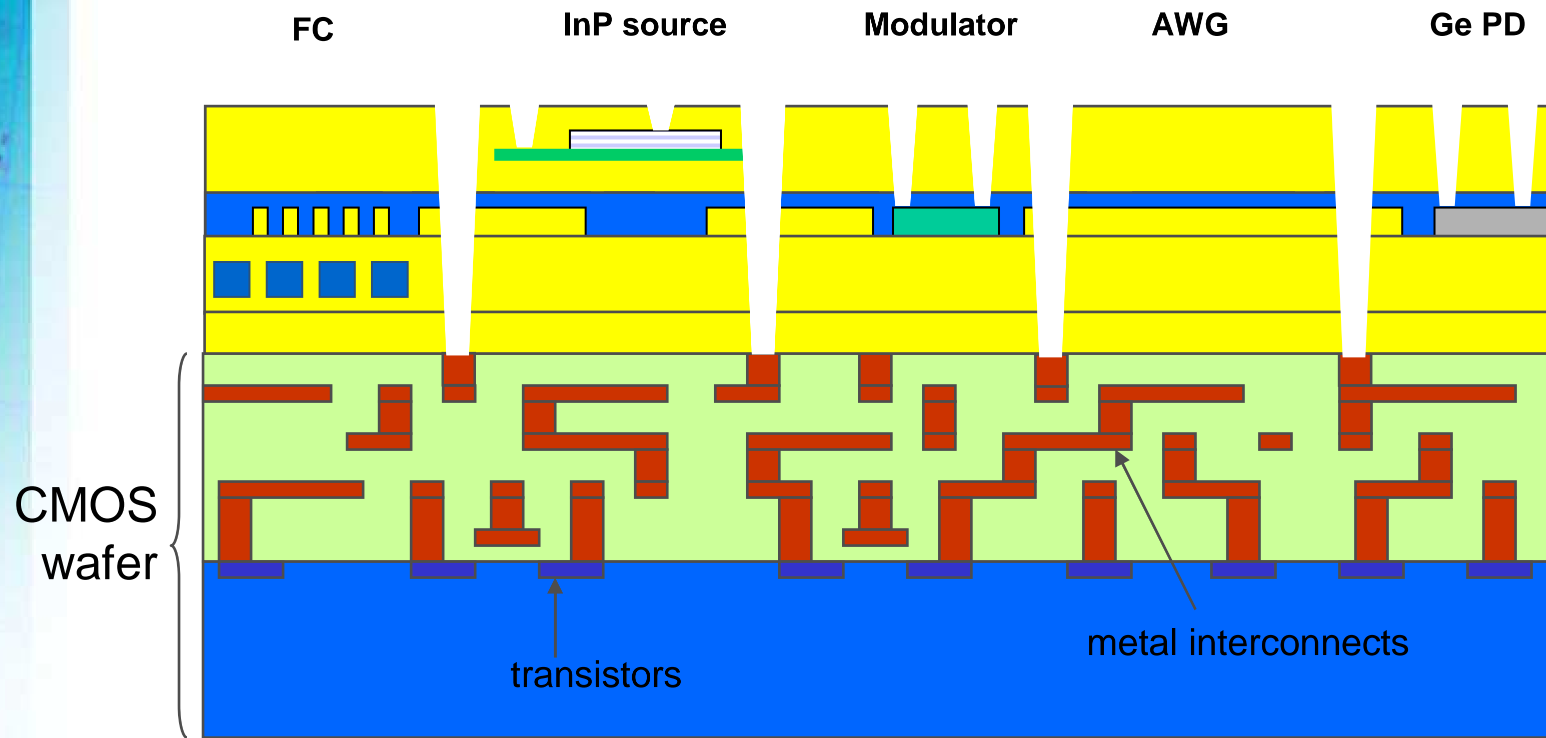
Step 10: Vias formation

- Lithos for different depths
- Etching SiO2



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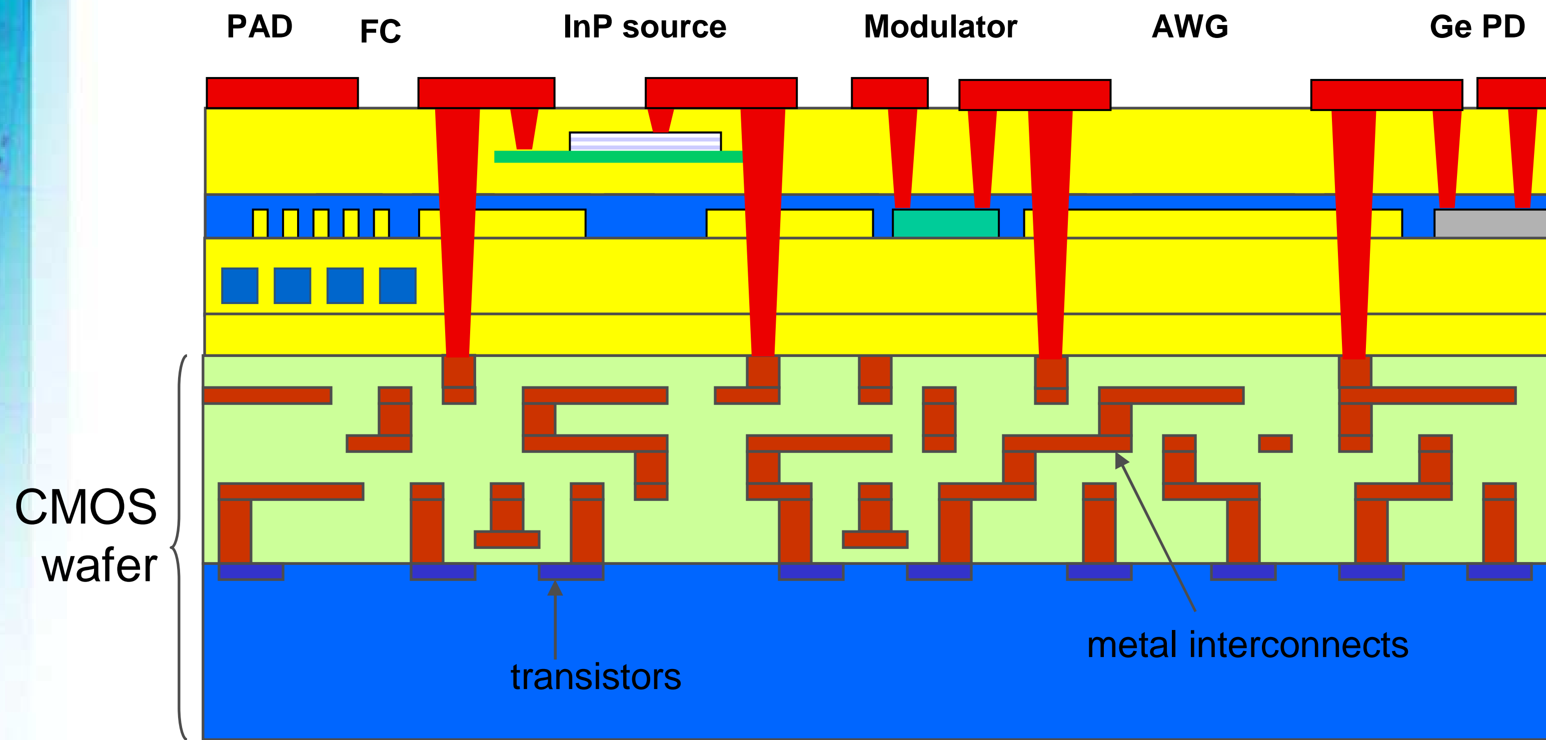
Step 11: Metal formation

- Metal deposition
- Metal etching



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Leti

Summary

- Optimisation of 200mm InP on Si technology on-going
  - Die to 200mm wafer molecular bonding
  - DUV lithography on die
  - InP etching
  - Compatible metallisation
- LED and Laser demonstrated on Si
- Two ways to integrate InP on CMOS
  - Above IC
  - Back side with TSV
- Contamination issue is manageable

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Acknowledgements

- All partners of HELIOS project

THANK YOU FOR YOUR ATTENTION !

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