Symposium: Real-time Digital Signal Processing for Optical Transceivers

FPGA based Prototyping of Next Generation Forward Error Correction

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Mitsubishi Electric Corporation, Information Technology R&D Center

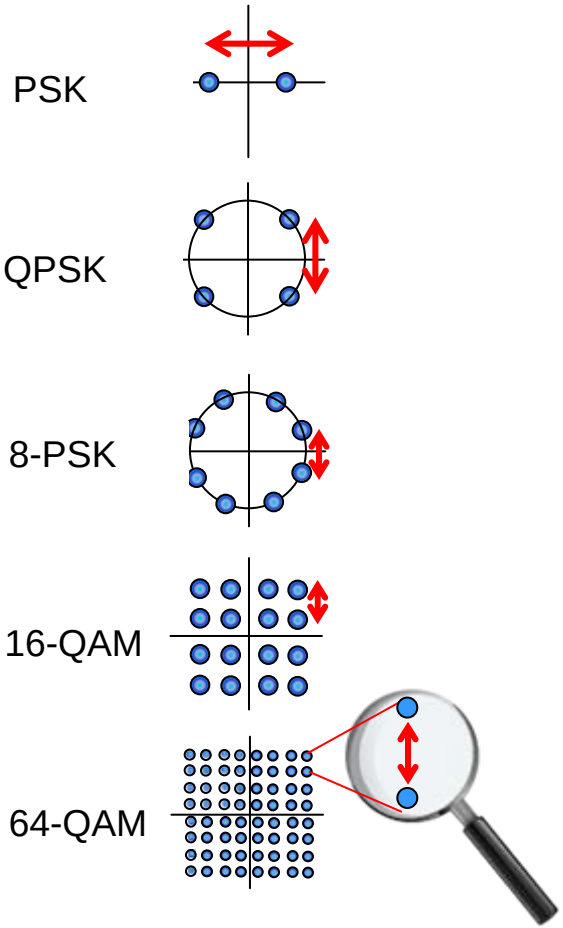
Outline

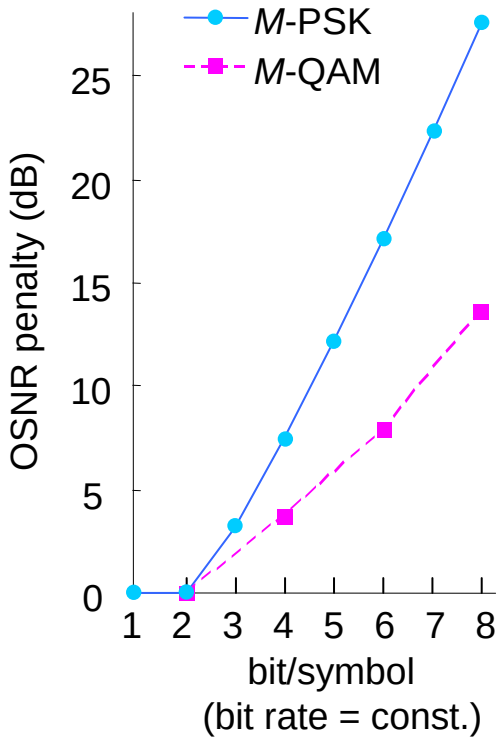
- Expectations of stronger FECs for 100Gb/s transmission
- Soft decision based LDPC + RS
- FPGA prototyping
- Error correction experiment
- LSI for 100G digital coherent

Expectations of Stronger FECs for 100Gb/s Transmission

100G Needs Higher OSNR

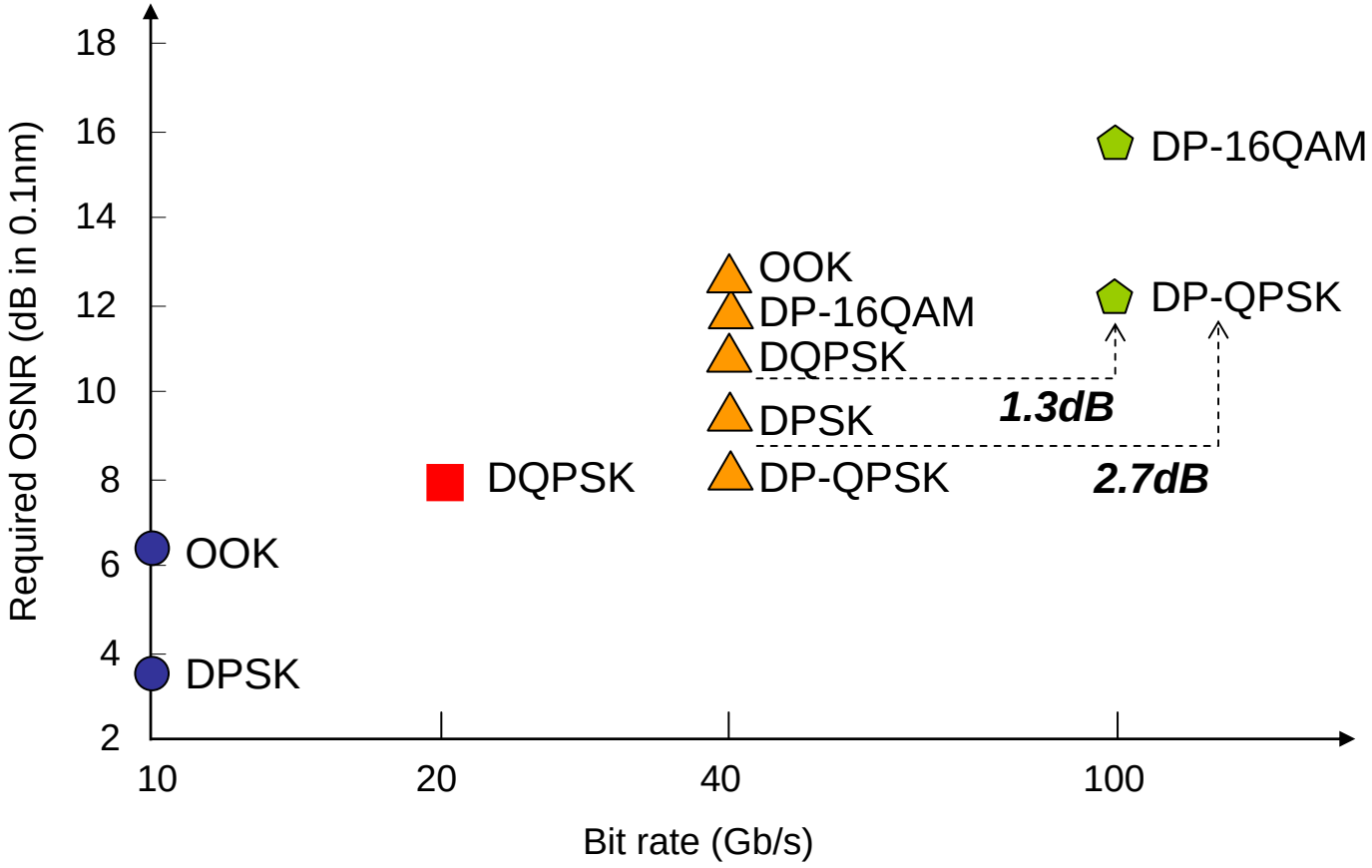
- We should not lose sight of the fact that multi-level modulation needs a higher SNR than binary formats.
- As the level of an M-ary modulation scheme increases, the Euclidean distance decreases, and it becomes more difficult to distinguish between states.
- The rate of decrease of the Euclidean distance is faster than the rate of noise bandwidth reduction.





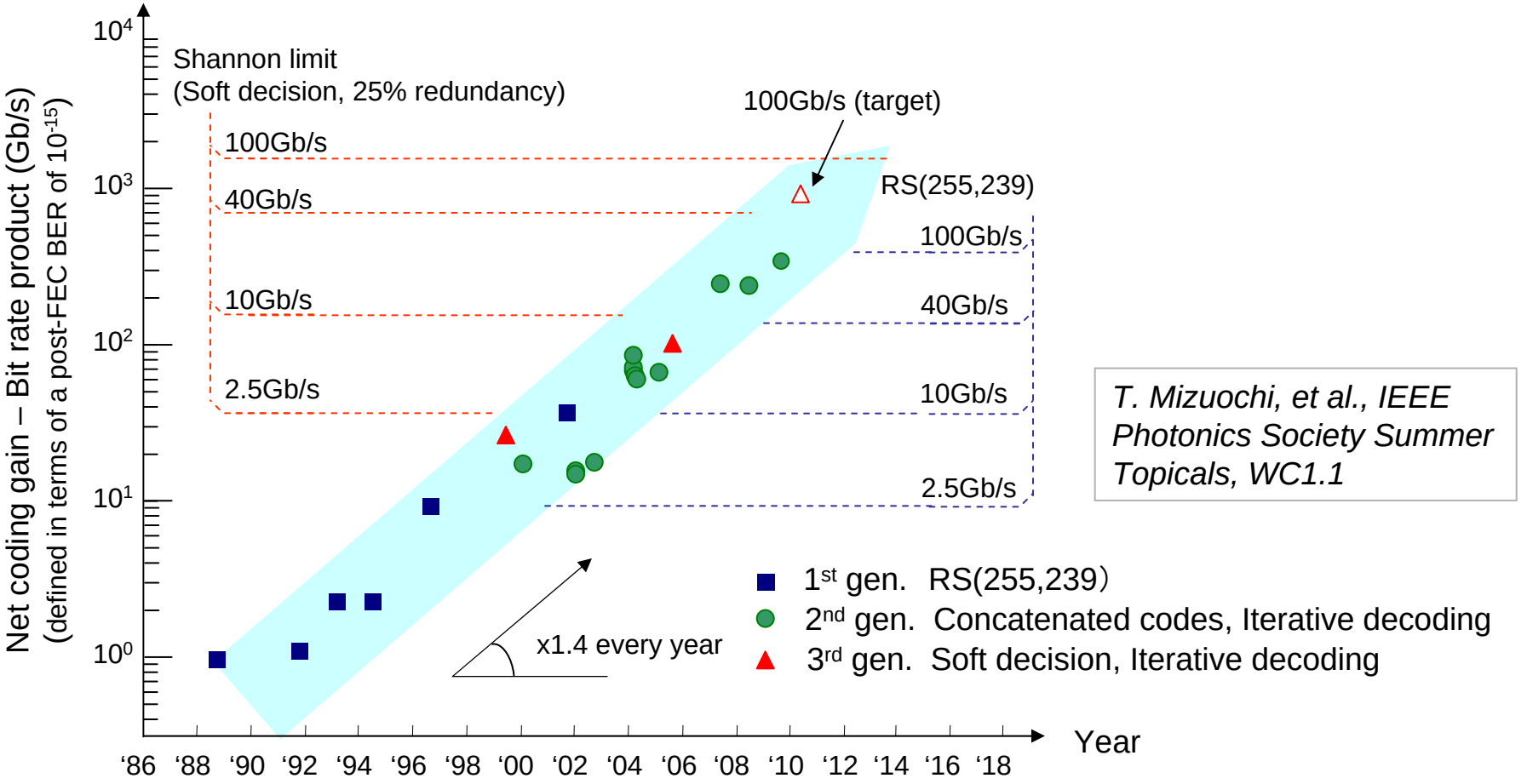
Toward 100Gb/s

- In order to deploy 100G over existing 40G systems, 1.3dB~2.7dB higher OSNR becomes mandatory.
- Stronger FEC can be a great help here



FEC Deployment in Optical Communications

- The product of (linear) NCG and bit rate (in Gb/s) shows a clear trend in that an improvement of 1.4 times has been achieved every year.
- This improvement has been achieved not by FEC algorithm improvements, but by LSI technology evolution.
- Very strong FECs can be a key enabler for DSP-based 100G transmission.



T. Mizuochi, et al., IEEE Photonics Society Summer Topicals, WC1.1

Soft Decision based LDPC + RS

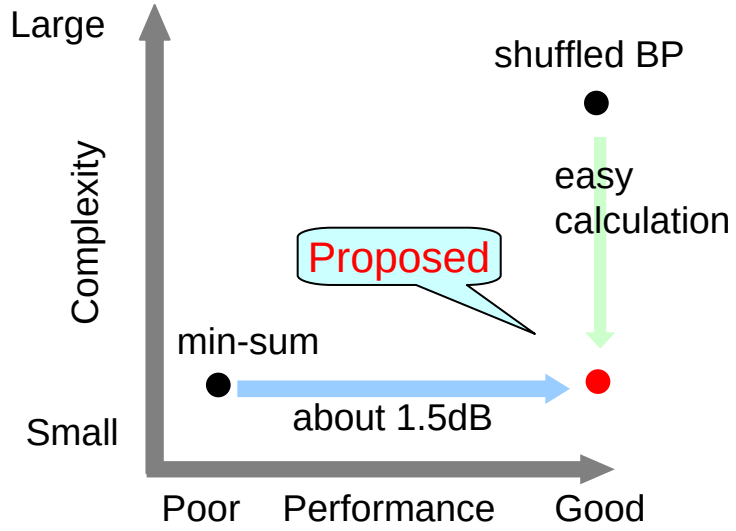
Low-Density Parity-Check Codes – LDPC –

A linear code, defined by a very sparse parity check matrix

- Invented by Robert Gallager in his 1960 MIT Ph.D. dissertation. Long ignored.
  - *R. G. Gallager, IRE Trans. Inform. Theory*, Jan. 1962.
- Re-discovered by D. MacKay in 1996.
- Can achieve very strong error correction capability
- First calculation for optical communications
  - *B. Vasic and I. B. Djordjevic., IEEE Photon. Technol. Lett., Aug. 2002.*

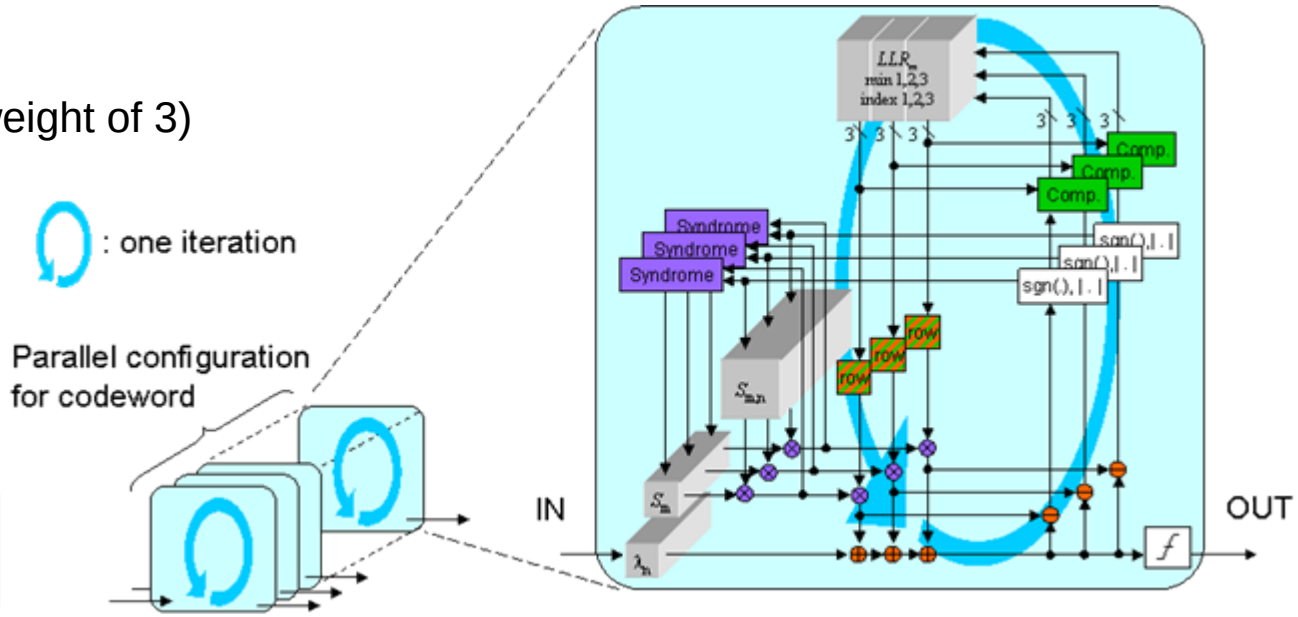
Decoding Algorithms and Circuit Complexity

- Conventional algorithms
  - *Shuffled belief propagation* (*BP*)
    - High-performance, but quite complex
  - *Min-sum algorithm*
    - Easy calculation, but poor performance
- Cyclically approx. δ-min algorithm (Proposed)
  - Simple LLR calculation
  - Mathematical function approximated by δ- and minimum functions
  - → nearly identical performance to Shuffled BP
  - → nearly 1/5 the circuit size of Shuffled BP



- Circuit configuration

  for one codeword's bit (a weight of 3)



Y. Miyata, et al.,
OFC/NFOEC2007, OWE5

Combating Error Floor

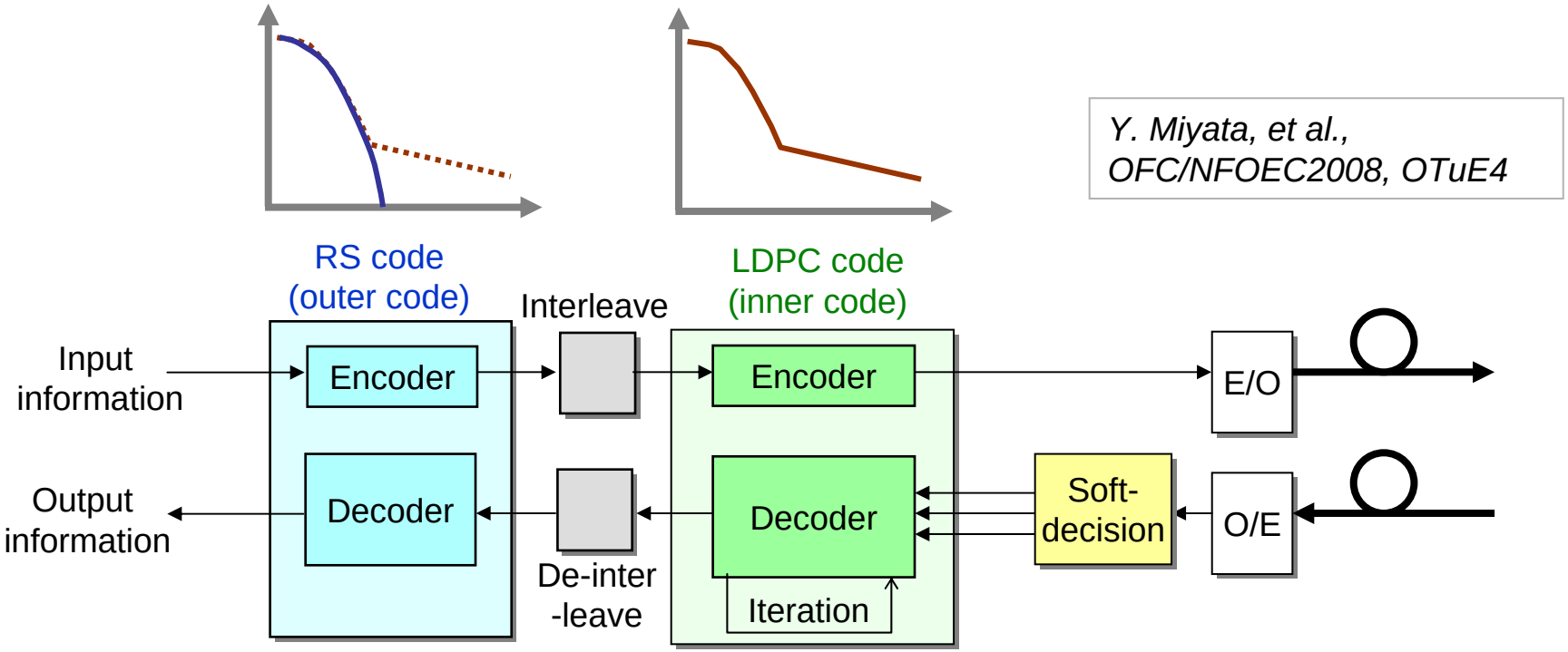
- How to eliminate the error floor

  (1) Increase the codeword length → 20,000 bits or longer are needed
  (2) Increase the redundancy → 35% or more is needed

  These can't be allowed in high speed optical communication systems
- Concatenating another weak code can effectively eliminate the unwanted error floor, without increasing circuit complexity.

Concatenated LDPC + RS

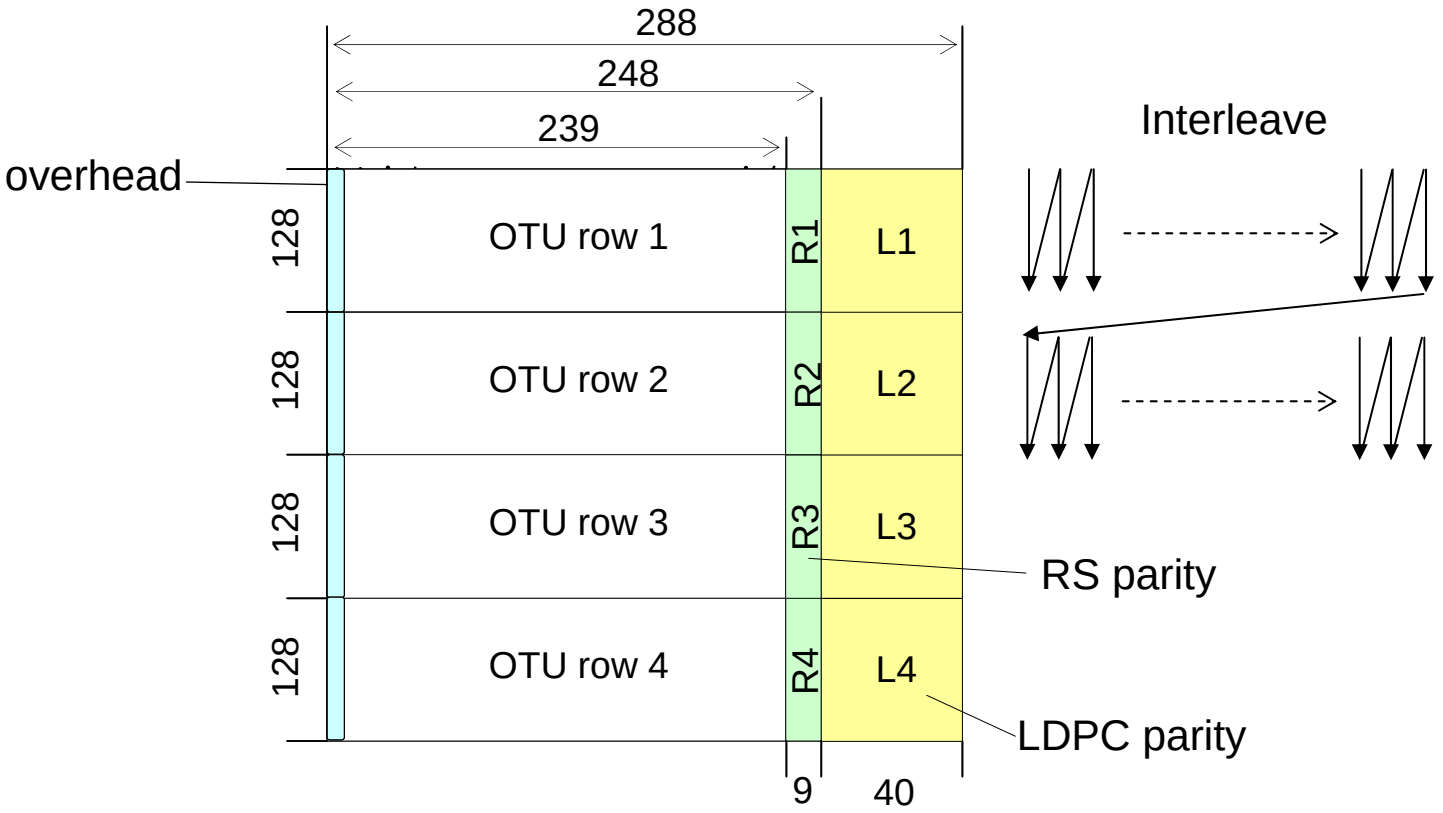
- **LDPC(9216,7936)** + **RS(992,956)**, 20.5% redundancy



Y. Miyata, et al.,
OFC/NFOEC2008, OTuE4

OTU4V Frame

- OTU4V frame for LDPC + RS
  - The length of the payload is the same as the OTUk frame
  - Enables transparent transmission of 100GbE client signals
  - Enables asynchronous multiplexing of multiple 10 Gb/s signals
  - Efficient parallel-processing of FEC enc./dec. and interleaver as a multiple of 128-parallelism

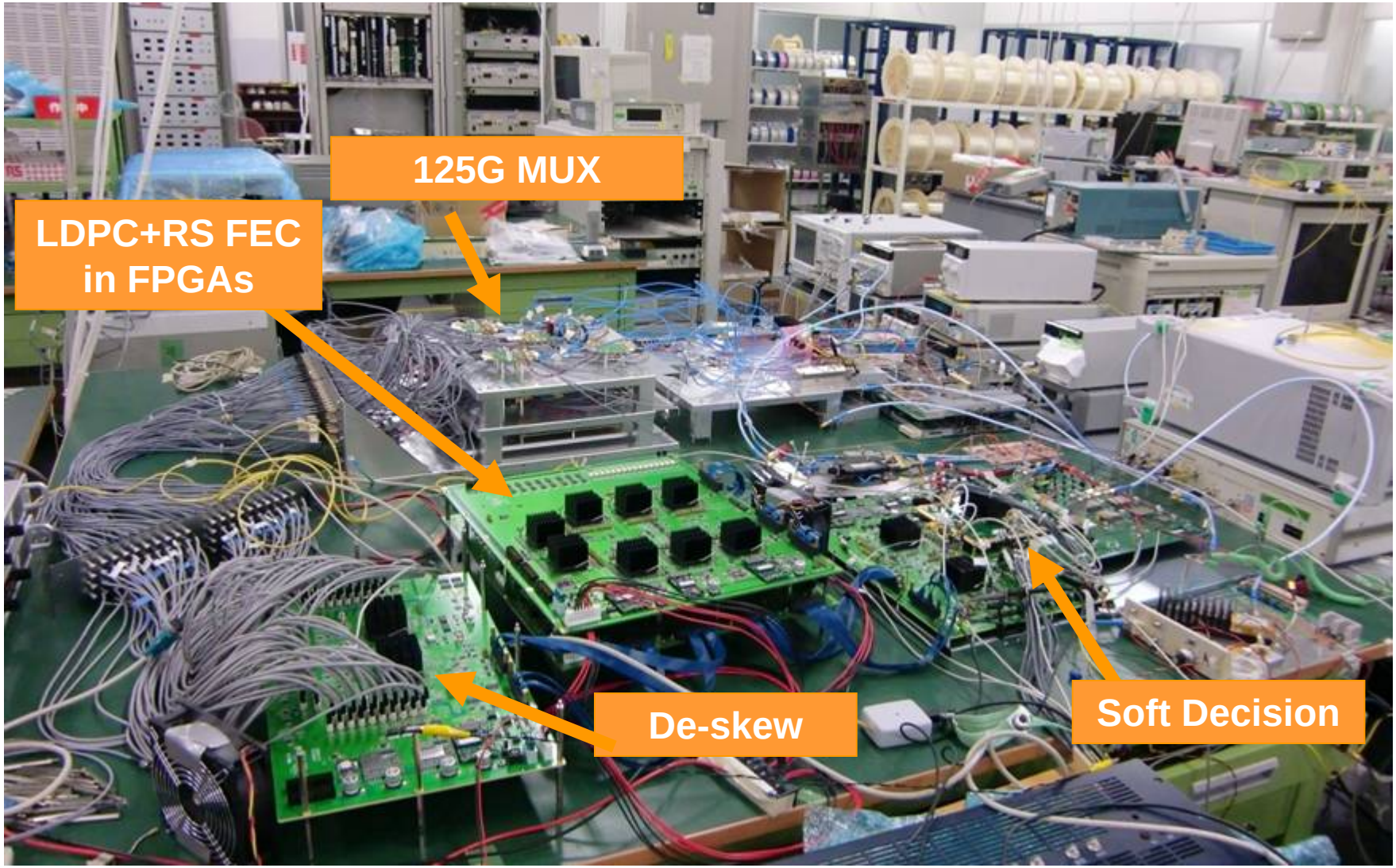


Y. Miyata et al., OFC/NFOEC2009, NThB2

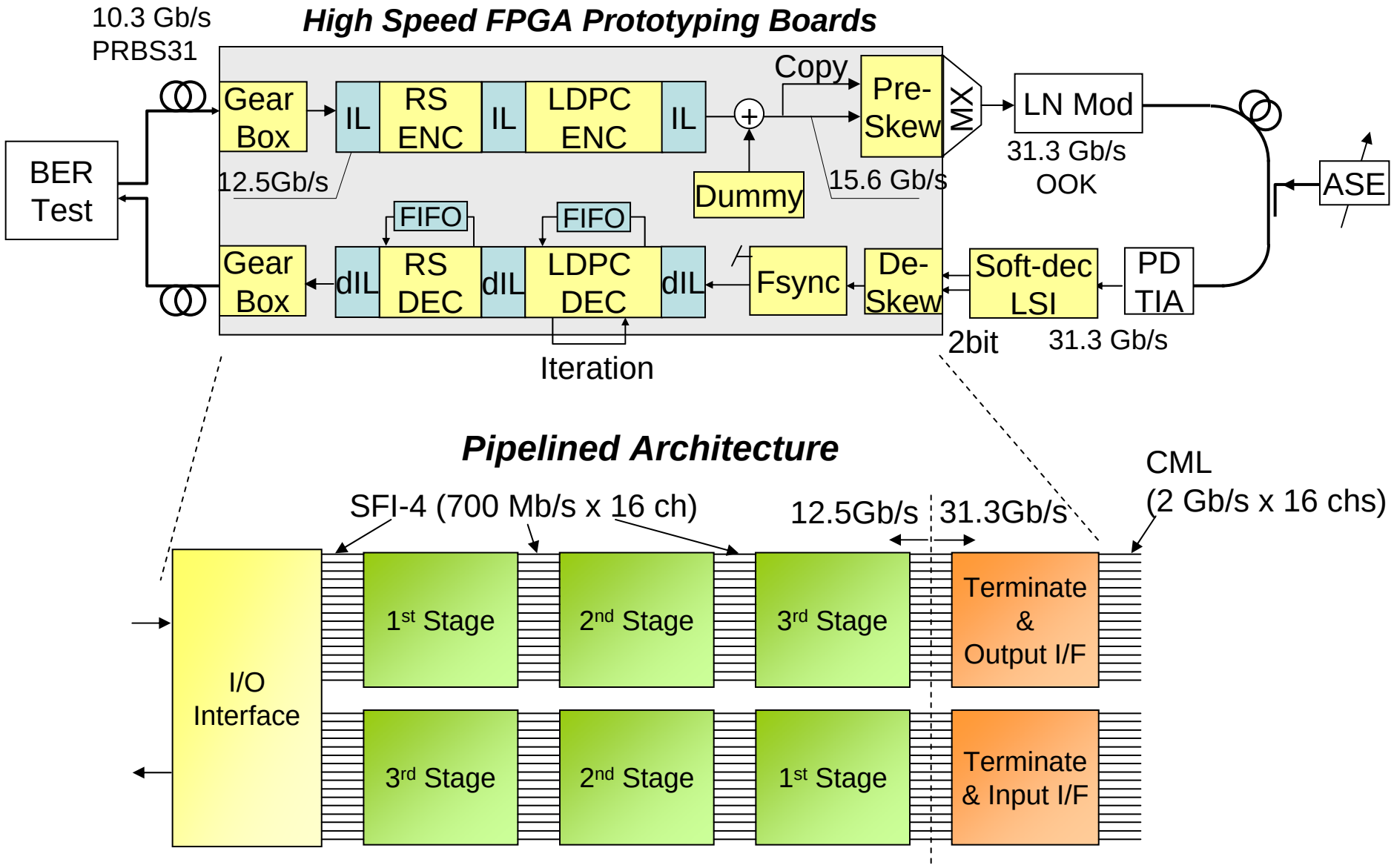
FPGA Prototyping

FPGA Prototyping

- Real-time emulation using high-speed FPGAs



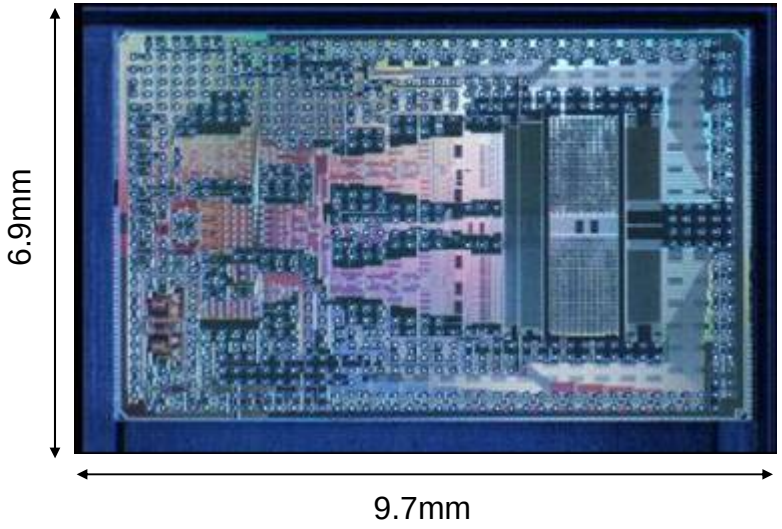
Set-up for FPGA Prototyping



31 Gsample/s Soft Decision LSI

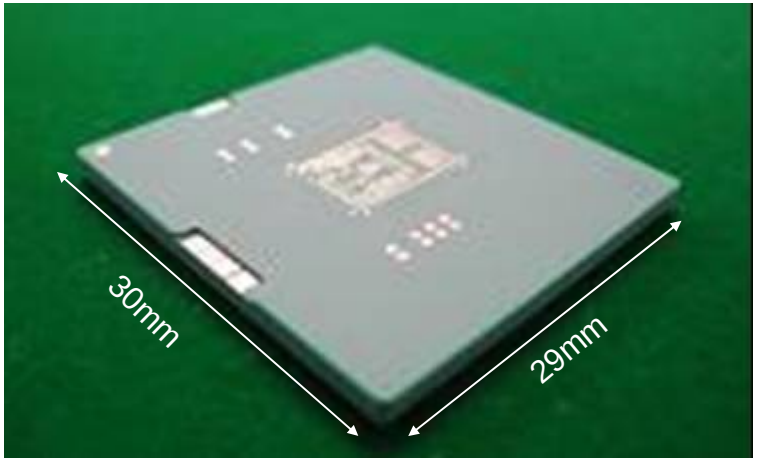
LSI Chip

- 0.13μm SiGe BiCMOS (f_T=200 GHz)
- 9.7mm x 6.9mm
- 14W (+3.3V)



Package

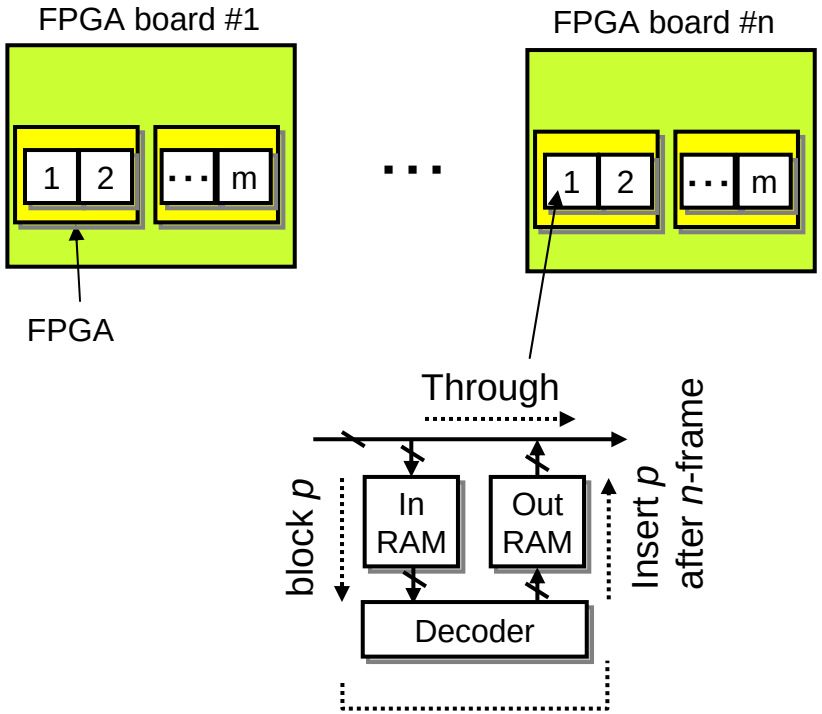
- Low temperature co-fired ceramic
- 30 mm x 29 mm x 2.15 mm
- 570 I/O pads

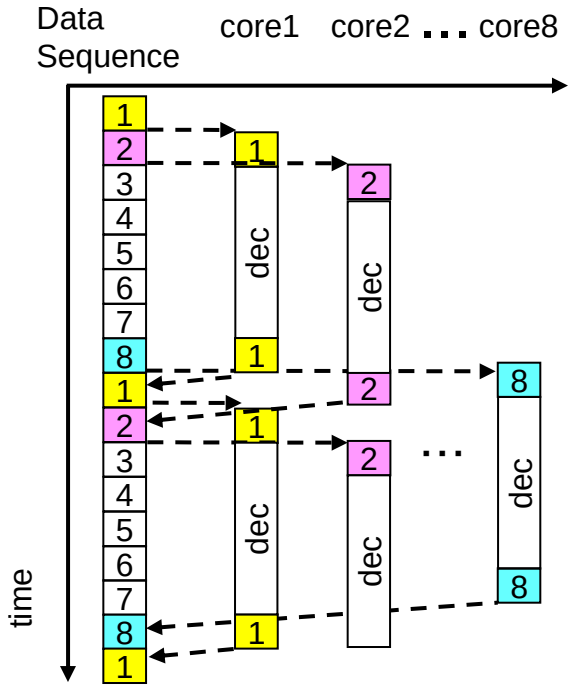


T. Kobayashi, et al., OFC/NFOEC2009, OWeE2

Pipelined Architecture

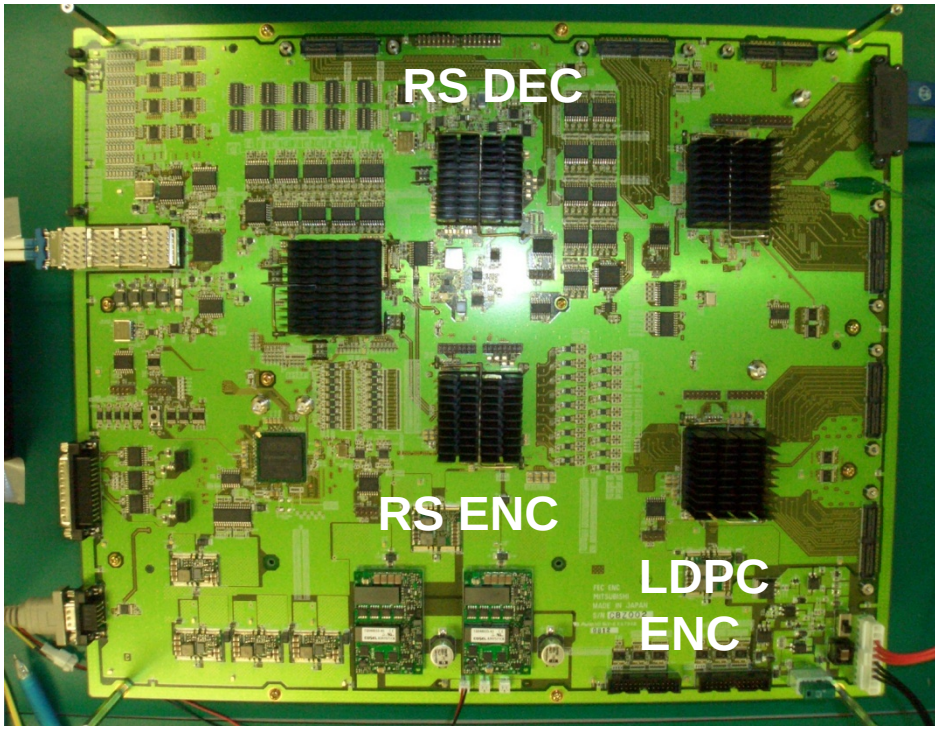
- In order to emulate the operation of a massive circuit, e.g. iterative decoding, a pipelined architecture was constructed from concatenated FPGAs.

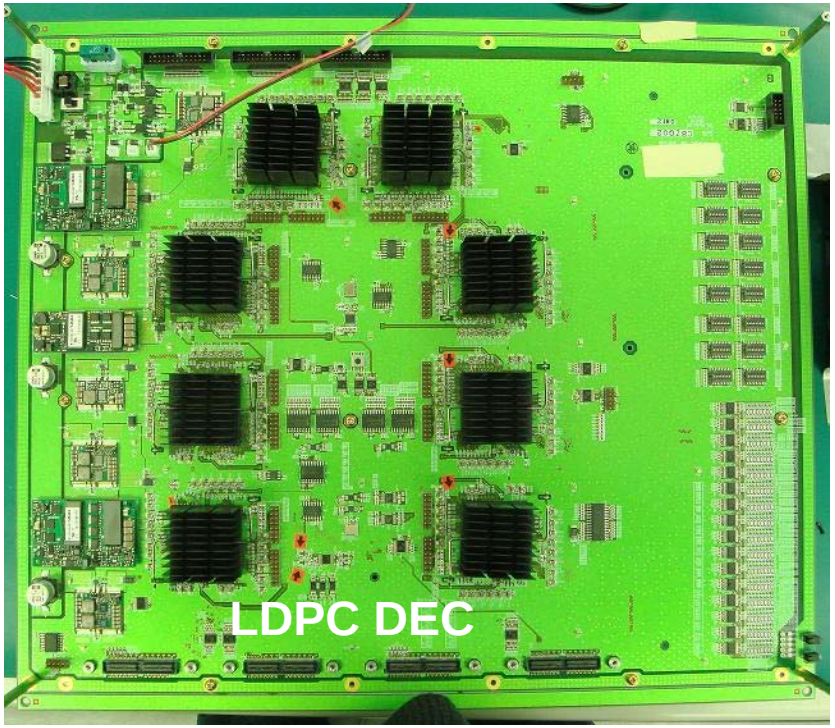




FPGA Boards

- Altera Stratix II
  - 2 Mgates
  - 100 MHz x 128=10 Gb/s throughput
- Pipeline
  - 8 x FPGAs on a board
  - n-concatenation = n x 8 x 2 (Mgates)

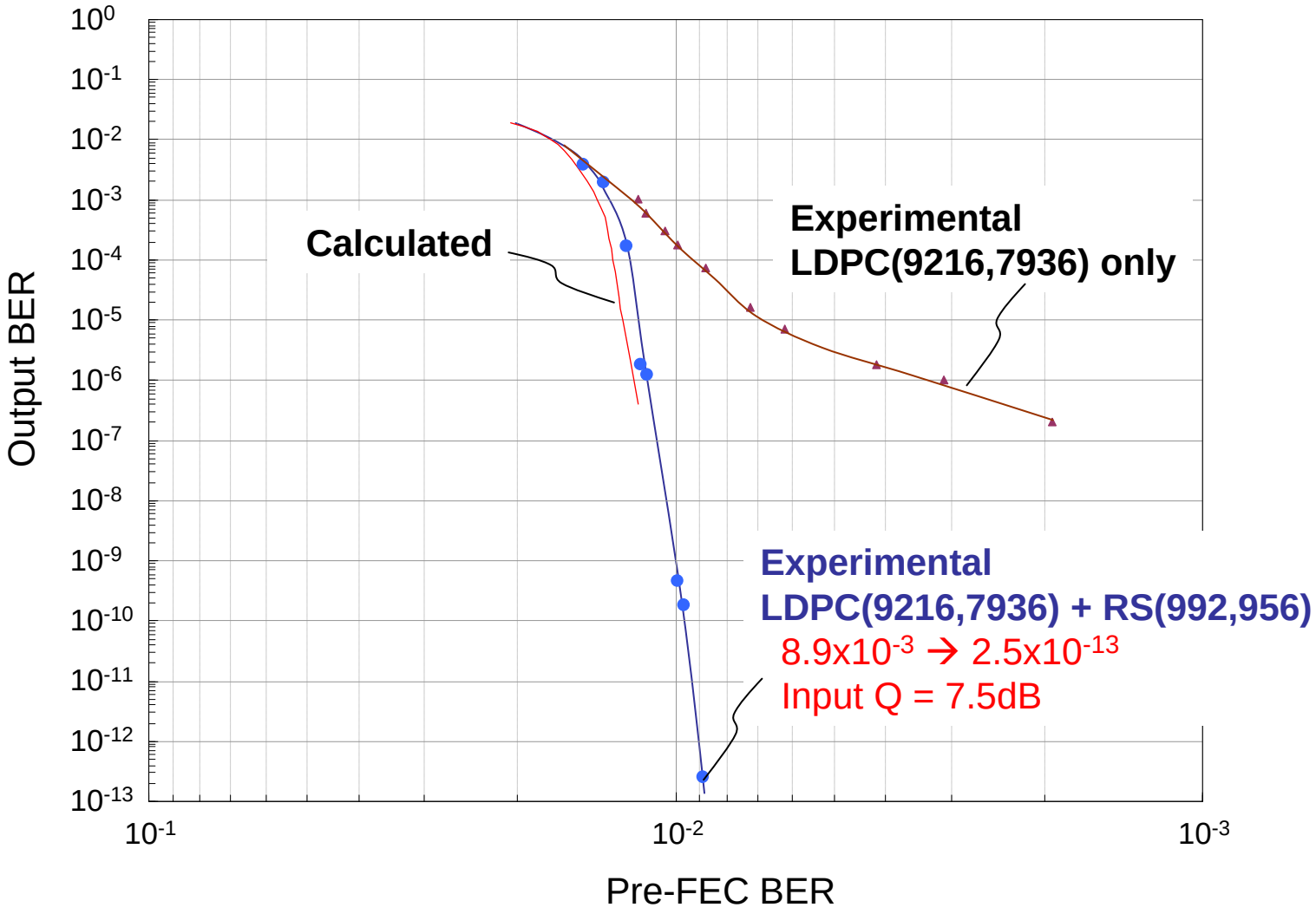




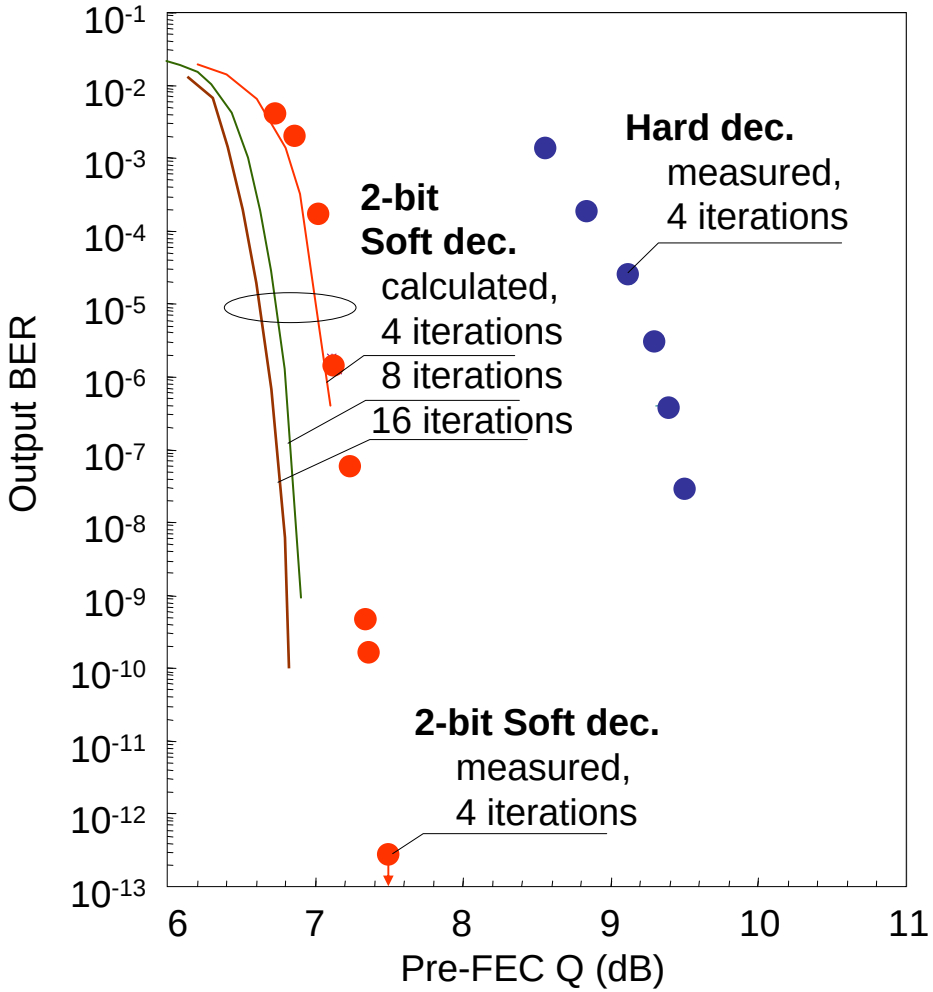
Error Correction Experiment

Experimental Results

31.3 Gb/s AWGN OOK, 2-bit soft dec., 4 iterations



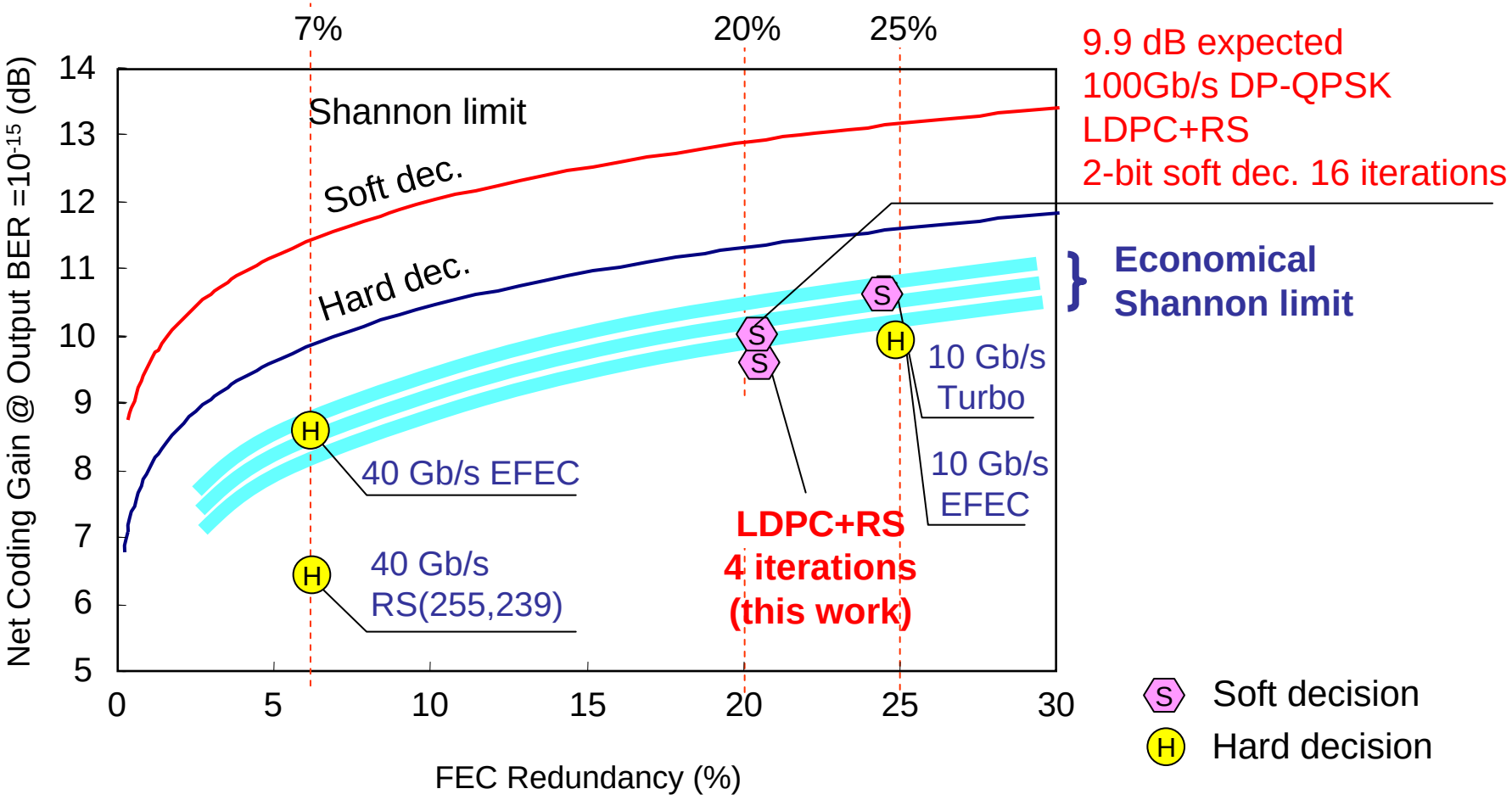
Hard/Soft dec. and Number of Iterations



- Soft dec.
  2.4 dB better than hard dec
- Number of iterations
  4, 8, 16
- Expected NCG @10^{-15}
  9.9 dB
  (1.2×10^{-2} → 1×10^{-15})
  2-bit soft dec.
  16 iterations

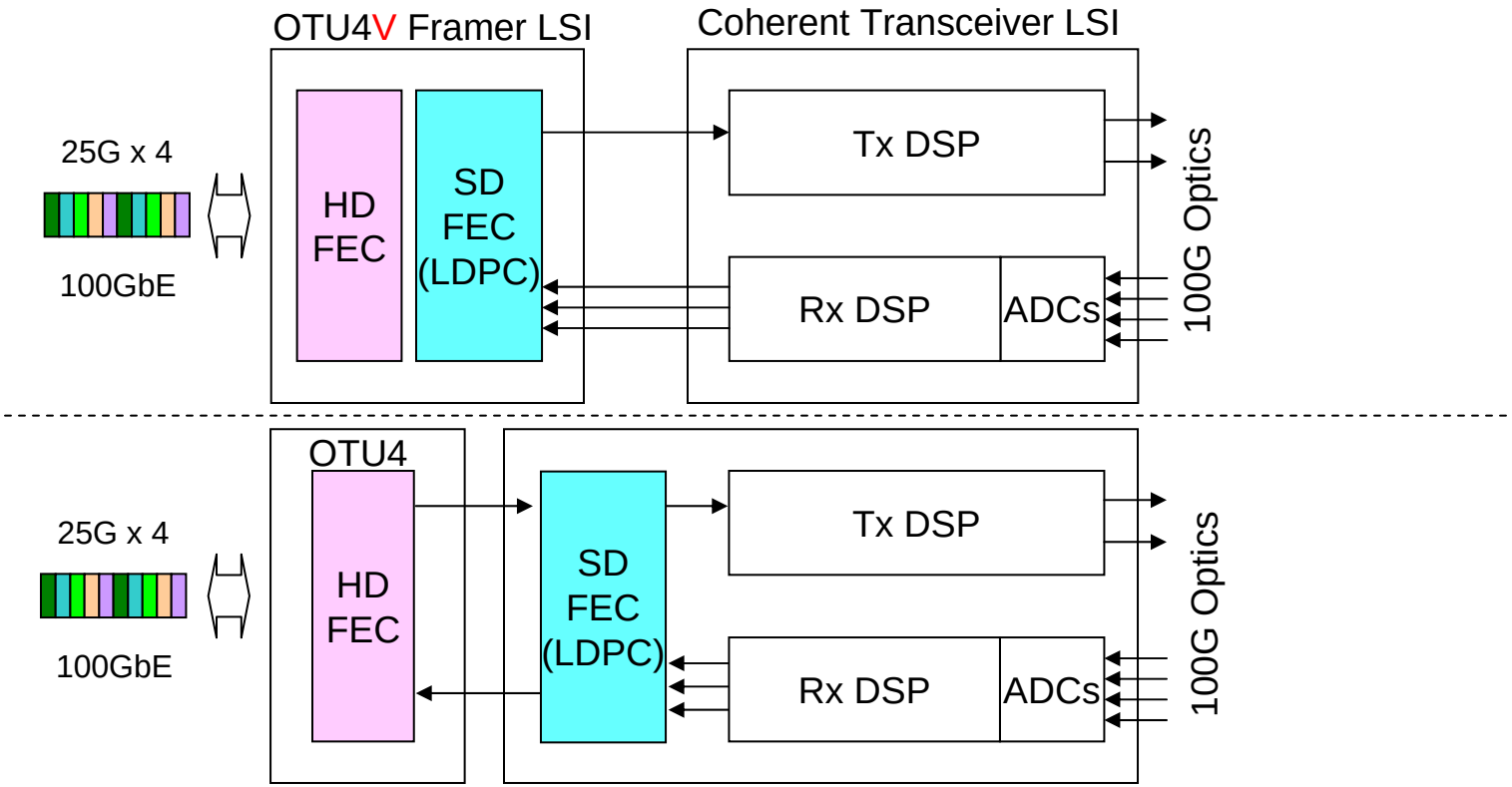
Comparison with Shannon Limit

- NCG of >9.9 dB can be expected for 100G DP-QPSK
  2-bit soft dec., 16 iterations
- Unseen limit = *Economical Shannon limit*
  1dB more gain needs >10M$



LSI for 100G Digital Coherent

Implementation in 100 Gb/s LSI



- FEC redundancy, Latency, Balance between hard dec and soft dec
  - 20% is preferable, 4~5x OTU4
  - xx% hard dec in OTU4 framer + yy% soft dec in coherent transceiver LSI
- LSI Technology, Expected performance
  - 45nm CMOS, < 30~50 Mgates
  - hopefully NCG of 10~11dB at BER=10^{-15}

Conclusions

- Expectations of stronger FECs for 100Gb/s transmission discussed
  - 1.3~2.7 dB stronger NCG than 40G EFEC is expected
- Soft decision FEC for coherent systems proposed
  - Concatenated LDPC + RS, Cyclically approximated δ-min algorithm
- FPGA prototyping developed
  - Pipelined architecture, 31.3 Gb/s throughput
- Error correction experiment carried out
  - 7.5 dB input Q can be corrected to 10^{-13} (2-bit soft dec., 4 iterations)
  - 9.9 dB NCG @10^{-15} is expected for 100G DP-QPSK
- 100G LSI issues discussed
  - Hard decision FEC in OTU4 framer LSI + soft decision FEC in coherent LSI
  - Further improvement of NCG : 10~11dB expected
  - Real ASIC for 100G may emerge in 2010~2011

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