Challenges for VLSI implementation of 100G digital coherent receivers

Hiroshi ONAKA
FUJITSU Limited
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Very much appreciate for cooperation by
- Fujitsu advanced technology
- Fujitsu Laboratories
Example configuration of 100G digital coherent LSI

Technical challenges

- Connection between ADC and DSP
- Lower power consumption
- Efficiency improvement of LSI development
### Technical challenge 1
Connection between ADC and DSP

<table>
<thead>
<tr>
<th>Case</th>
<th>Connection method</th>
<th>Technical Subjects</th>
</tr>
</thead>
</table>
| (a)  | ![Diagram](image)  | • Multichip configuration  
  - ADC: SiGe Bi-CMOS  
  - DSP: CMOS  
  • Connection with digital signal  
  • Tbips class digital interconnection between ADC and DSP  
  • Hybrid packaging of ADC and DSP |
| (b)  | ![Diagram](image)  | • Multichip configuration  
  - T/H: SiGe, InP etc.  
  - ADC Bank, DSP: CMOS  
  • Connection with analog signal  
  • Noise and crosstalk in connection of analogue signal  
  • Hybrid packaging of ADC and DSP |
| (c)  | ![Diagram](image)  | • Monolithic configuration  
  - All functions are integrated on Si  
  • Ideal configuration  
  - Direct connection on Si  
  - Feasibility of CMOS ADC  
  - Mixed signal system LSI design |
Discussion about power consumption of 100G MSA module in OIF

Power Dissipation

Assumption:
- Air temperature before module: 55° C
- Module temperature: ~70° C

Maximum power dissipation:

<table>
<thead>
<tr>
<th>Airflow</th>
<th>20 mm height with 13 mm fins</th>
<th>16 mm height with 17 mm fins</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 m/s</td>
<td>59W</td>
<td>65W</td>
</tr>
<tr>
<td>2 m/s</td>
<td>73W</td>
<td>80W</td>
</tr>
</tbody>
</table>

Question 31 - Maximum power allowed
- ≤ 80W

module size: 5 inch x 7 inch
6 inch x 8 inch
Technical challenge 2
Heating issue

40G DWDM 300pin MSA module
- Size: 5 inch x 7 inch
- Maximum power: ~ 30W

For 100G MSA module?

- 65W cannot be allowed considering junction temperature of transistor

- For 100G MSA module, it is necessary to decrease 35W or less, and target power of LSI should be about 15W

- Details will be discussed in next OIF meeting
Technical challenge 3
Efficiency improvement of VLSI development

Simulation speed

High

Low

DSP Specification

Algorithm design

Design of DSP algorithm (1)
VPI etc., MATLAB, C/C++

Algorithm only
Hardware is not considered

Introducing of functional program
and bit width definition

Design of DSP algorithm (2)
C/C++

Design of DSP algorithm (3)
System C

Adding implementation & restriction condition
in hardware architecture

Logic design

High-level synthesis

RTL code

Equivalence checking

RTL : Resister Transfer Level

Physical design
Logic synthesis, Place & route design
Advantages of High-level Synthesis

Automated design process that interprets an algorithmic description using C++/System C and creates RTL (Resister Transfer Level) code

- **Shortened design term**: Introducing automatic design at early stage
- **Decrease in design mistake**: Human error is prevented by automated synthesis
- **Expansion of design area**: Better architecture can be decided in consideration of trade-offs because various choices can design/evaluate in a short time
- **Easiness of design**: Decrease of description amount and increase of understanding level by enhancing abstraction level of design
All systems simulator including transmitter, transmission line, and receiver model

- Precise verification of DSP operation with restriction and condition of hardware by using all systems simulation

Transmitter model

- Signal Source
  - LD
  - Precoder
  - Mod.
  - Pol. Mux

Transmission line model

- X.I/Q
- Y.I/Q

Receiver model

- LD
- Controller
- 90° Optical Hybrid + O/E
- ADC
- DSP
- Error Detector

Controller

- H.I/Q
- V.I/Q

ADC

Error Detector

Precoder

Mod.

Pol.

SOP Rotate

CD Adder

PMD Adder

DGD = τ

90° Optica

Hybrid + O/E

ADC

DSP

Error Detector

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### Design example by using High-level synthesis

<table>
<thead>
<tr>
<th>Fixed Equalizer</th>
<th>Line number</th>
<th>Gate count</th>
</tr>
</thead>
<tbody>
<tr>
<td>C model (System C)</td>
<td>3,091</td>
<td></td>
</tr>
<tr>
<td>RTL (High-synthesis)</td>
<td>259,016</td>
<td>6.8M gates x2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Adaptive Equalizer</th>
<th>Line number</th>
<th>Gate count</th>
</tr>
</thead>
<tbody>
<tr>
<td>C model (System C)</td>
<td>328</td>
<td></td>
</tr>
<tr>
<td>RTL (High-synthesis)</td>
<td>42,712</td>
<td>3.4M gates</td>
</tr>
</tbody>
</table>

#### Comparison

- **Line number of Synthesized RTL increased to 100 times that of C model**
- **Line number of handwriting RTL increase to about 10 times that of C model**
- **Gate number by high-level synthesis confirms becoming the same as handwriting RTL**
Estimated gate counts of 100G DSP

Total: 26.2 M Gates
Summary

- 100G DSP can be realize on a realistic gate scale. Necessary to reduce power by half for 5 inch x 7 inch MSA module.

- High-level synthesis tool is very effective for development of 100G DSP.

- All system simulation is very useful for precise verification of ADC/DSP operation.