Hybrid Optoelectronic Router

Ryohei Urata,
Tatsushi Nakahara, Hirokazu Takenouchi, Toru Segawa, Ryo Takahashi

NTT Photonics Laboratories, NTT Corporation

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Electrical Routers

- Reduce power consumption
- Reduce size
- Increase performance
  - Increase throughput
  - Increase traffic engineering capability

For 92 Tb/s:

80 racks
>1 MegaWatt

Power consumption per rack/chassis

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Problem with Electrical Routers

- Excessive buffering and processing
- Problems at the interfaces (MUX/DEMUX)
  - High power consumption
  - Speed limited by electronic components

Header Processing Buffering

Switching

Line Card

Electrical Switch

Line Card

AWG

O/E    O/E    E/O    O/E    E/O    O/E    E/O

SPC: Serial-to-Parallel Converter
PSC: Parallel-to-Serial Converter
Photonic Router

High Capacity       Low Power
Compact          Low Latency

Electrical Router

Buffering
Label Proc.
Switching

Novel optical device and subsystem technologies for processing burst packets

New router architecture incorporating optical technologies
Hybrid Optoelectronic Router Node Architecture
Node Architecture

Label processor
Optical switch

λ1, λ2, λ3, λ4

AWG

PSC

RAM

SPC

Shared buffer

No contention ➔ Passes through transparently

Drop ➔ Add

Contention ➔ Forwarded to shared buffer
Node Architecture

- Label processor
- Optical switch

10 Gbit/s IP packet

Contestion Resolution:
1\textsuperscript{st} : To the Desired Port
2\textsuperscript{nd} : Buffering in CMOS
3\textsuperscript{rd} : Wavelength Conversion
4\textsuperscript{th} : Deflection Routing
Node Architecture

- Label processor
- Optical switch
- AWG
- Add/Drop
- Shared buffer
- RAM
- PSC
- SPC
- Optical switch
- AWG

Buffering in CMOS RAM
Traffic engineering between wavelength layers
3R regeneration based on TTL
Buffer supports various services

QoS, FEC, Multicast routing, Policy routing
Sub-Systems
Label Processor Sub-System

Detect input label, packet envelope  ▶️  Process label, configure switch

Merges SPC, PSC, clock generation for compact, low-power system

ECG: Electrical Clock-Pulse Generator, OCTA: Optically Clocked Transistor Array
Optical Switch

- Optical Switch
- AWG
- PSC
- CMOS
- Shared buffer
- Label processor
- Drop
- Add
$N \times N$ non-blocking switch for packet-level switching

Low power, compact, fast switching, scalable

TWC, FWC: Tunable, Fixed Wavelength Converter
DRR-TLD: Double-Ring-Resonator-Coupled Tunable Laser Diode

Control Signals from Scheduler
Label Swapped Packet
Shared Buffer

Label processor
Optical switch

AWG

PSC
SPC
CMOS

Shared buffer

Drop
Add
Shared Buffer

SPC: Serial-to-Parallel Conversion
PSC: Parallel-to-Serial Conversion

Selective buffering, high-level packet functions
Asynchronous burst mode compliant, low power, CMOS functionality
Conclusion

Optical Technology + Electrical Technology

Photonic Router

- Optical technologies for high-speed burst packet processing
- Node architecture for transparency and high functionality

- Optically Clocked Transistor Array (OCTA)
- Double-Ring Resonator Tunable Laser
- All-Optical Serial-to-Parallel Converter (SPC)
- Optical Clock-Pulse-Train Generator (OCPTG)