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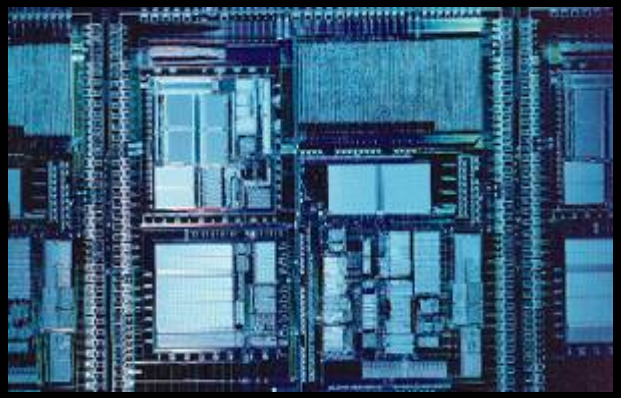
Future switching chips and semiconductor technology




Next generation switching ...

- **Network operator traffic increasing, originating by e.g.**
  - backhaul of wireless, VoIP,...
  - Increased Internet use
  - Change of user custom
  - e.g. peer-to-peer video, video on demand , rate of synchronization
  - Higher quality media
    - MPEG-4 320x240 ~500kb/s
    - MPEG-4 1280-720 ~6Mb/s = 12x
- **Challenge**
  - Design Technically feasible, power and cost effective solution to increase throughput in data transmission and data processing systems
- **My topic**
  - highlight some aspects to consider in next generation switching semiconductors based on bulk CMOS technology

Presented by :

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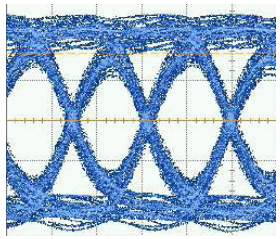
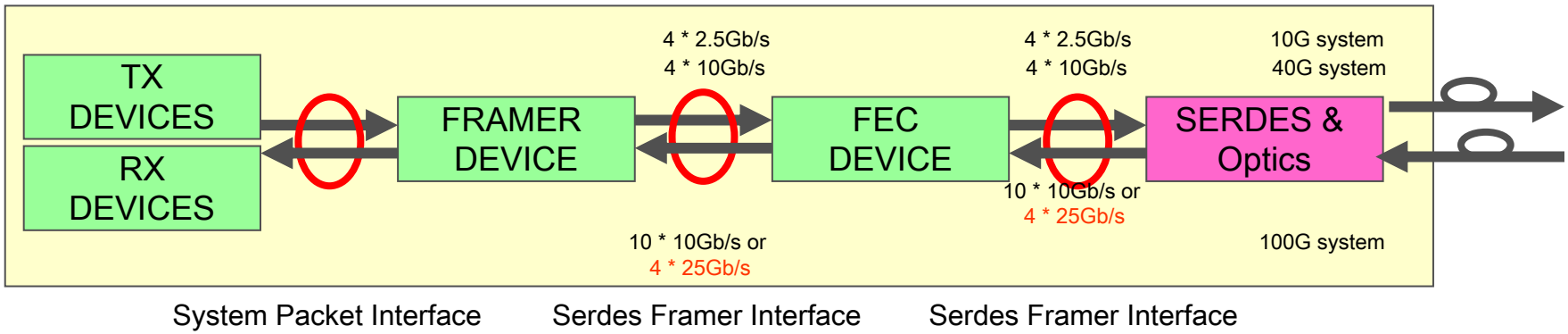
IO speed and design complexity increasing

- **Interface speed increase**
  - Standard Interfaces : DDR2, DDR2 PCIexpress, SATA,...
  - 10Gb/s , 40Gb/s, 100Gb/s systems (CEI)
  - assuming N serial electrical links to aggregate traffic
    - e.g. 40Gb/s system -> 4x10Gb/s...
  - max. IO frequency ?



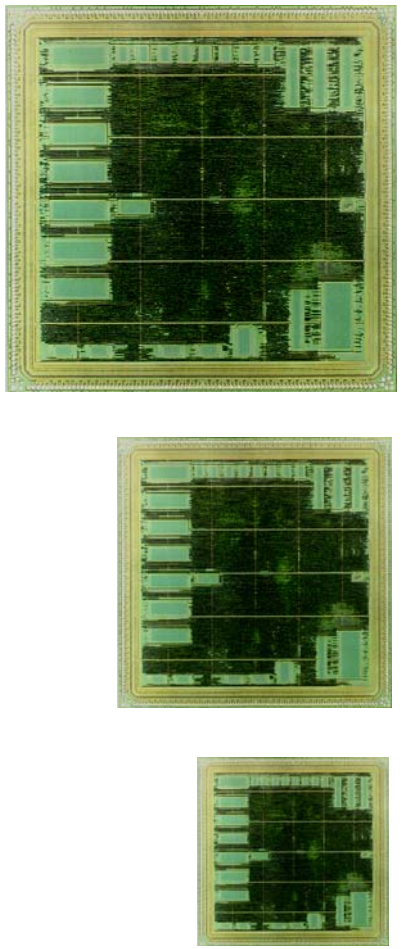


- **A 100G Ethernet (Packet oriented traffic) Switch fabric ...**
  - N serial IO interfaces
  - N x 100G switching capacity
  - ~1/10 * N Mpps packet processing
  - ~1/10 * N Gb/s interfaces (to backplane)
  - A core router with 10 interfaces needs
    - 10 SERDES Interfaces * 4 (25G) lanes * (TX+RX)
    - 1 Tb/s switching capacity

Moores Law - getting to the border ?

- **Law :Complexity doubles every 1.5 to 2 years**
- **Technology nodes scale by factor of S ~0.7**
- **130nm -> 90nm -> 65nm -> ...**
- **Yesterday :**
  - Area scales ~ S*S = 0.5
  - Performance scales ~ 1/S = 1.3
  - Capacitance scales ~ S = 0.7
  - Voltage scales ~ S = 0.7
  - Dynamic Power ~f*C*V ² = 0.45

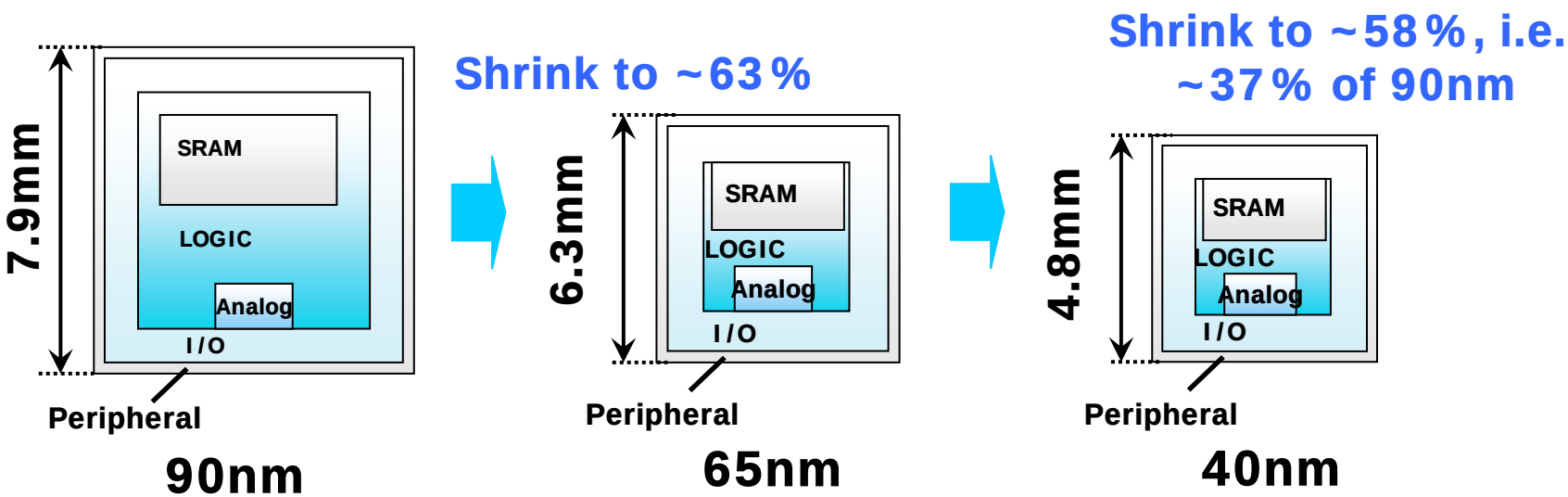
- **Tomorrow:**
  - Area scales ~ S ~0.8-0.7
  - Performance scales ~ 1
  - Capacitance scales ~ S ~ 0.7
  - Voltage scales ~ 1
  - Dynamic Power ~f*C*V ² ~ 0.8
  - 2nd and 3rd order effects get visible



Scalings are not the same : e.g. Area

- **Example of identical chip configuration**

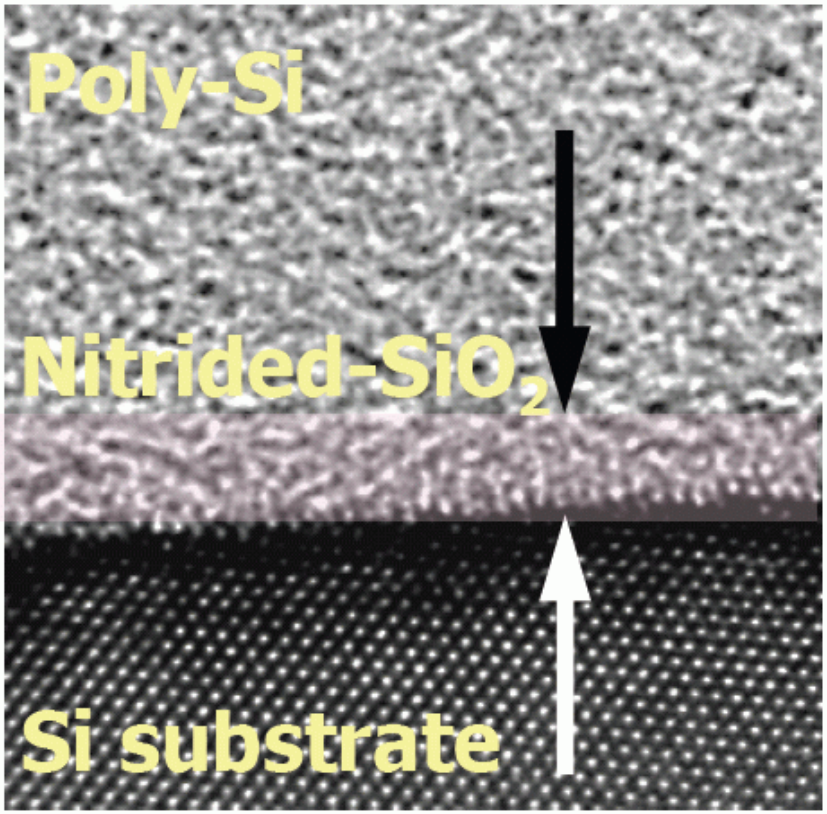
Node	LOGIC	SRAM	ANALOG, SERDES		PLL	Pad, IO, &scribe
	Ratio	Ratio	Analog ratio	Digital ratio	Ratio	Ratio
90nm	1.00	1.00	1.00	1.00	1.00	1.00
65nm	0.51	0.65	1.00	0.51	1.00	0.85
40nm	0.25	0.33	1.00	0.25	1.00	0.75



Origin of Variations

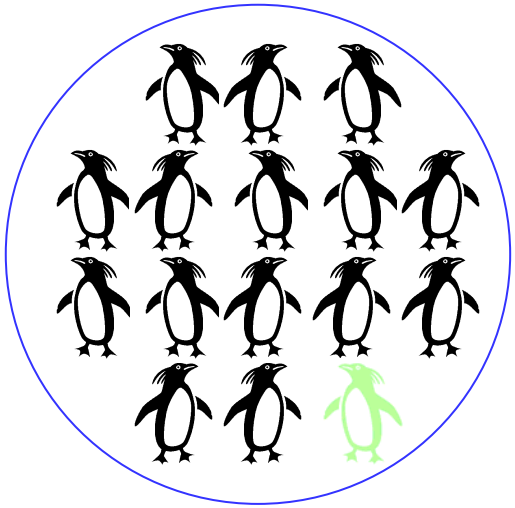
- **Lithography**
  - 193nm immersion litho for 40nm structures
  - OPC (WYSINWYG)
  - critical dimensions
  - Depth of focus
- **Transistor**
  - Variation between N and P
  - Stress/strain effects
- **Interconnect**
  - Metal width/height variation
  - Dielectric variation
  - Via/contact quality
- **Random or Deterministic**
  - delay variation at low voltages
  - e.g. orientation dependant performance

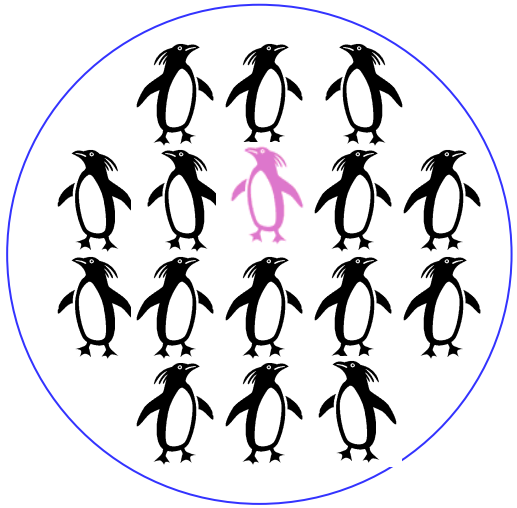
1nm-thick Gate Oxide

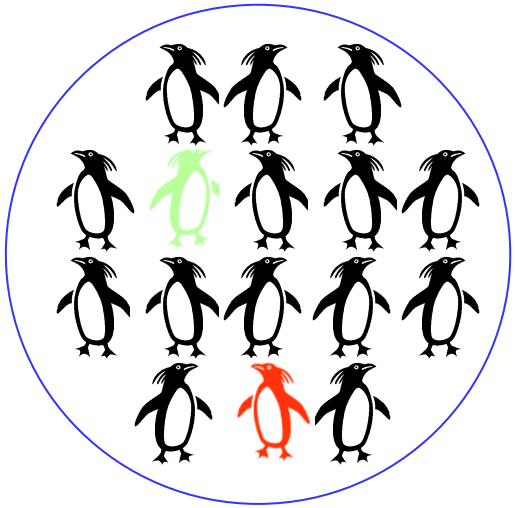


Variations ... and what is normal ?

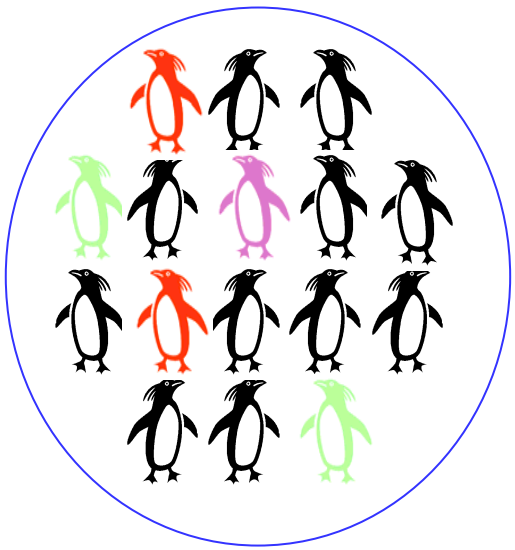
90nm CMOS

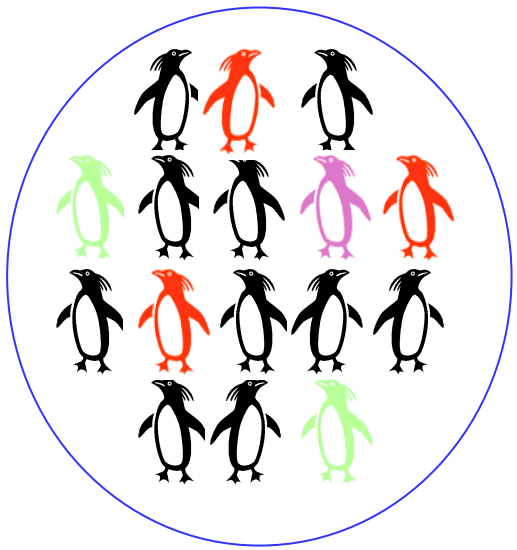


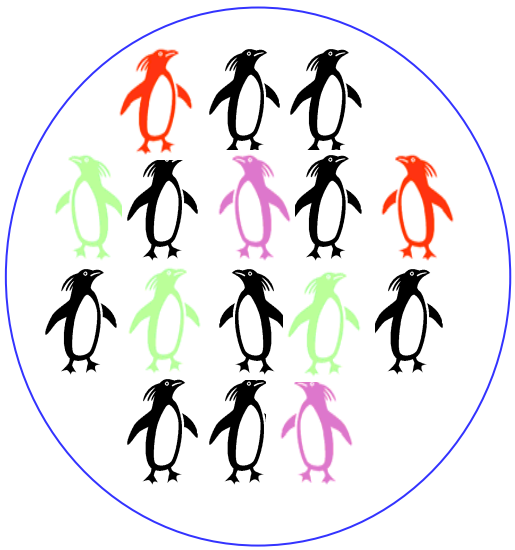




40nm CMOS and beyond

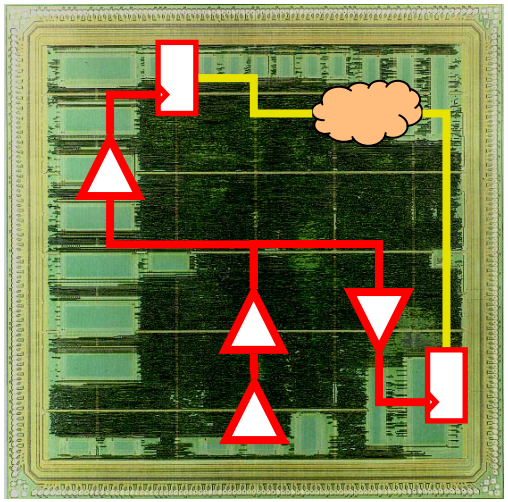






Fully synchronous design ?

- **Example Assumptions:**
  - 170 ps/square in X direction
  - 140 ps/square in Y direction
  - clock enters at bottom centre
  - signal starts at top left
  - chip is 10x10 squares



	1	2	3	4	5	6	7	8	9	10
1	0	170	340	510	680	850	1020	1190	1360	1530
2	140	310	480	650	820	990	1160	1330	1500	1670
3	280	450	620	790	960	1130	1300	1470	1640	1810
4	420	590	760	930	1100	1270	1440	1610	1780	1950
5	560	730	900	1070	1240	1410	1580	1750	1920	2090
6	700	870	1040	1210	1380	1550	1720	1890	2060	2230
7	840	1010	1180	1350	1520	1690	1860	2030	2200	2370
8	980	1150	1320	1490	1660	1830	2000	2170	2340	2510
9	1120	1290	1460	1630	1800	1970	2140	2310	2480	2650
10	1260	1430	1600	1770	1940	2110	2280	2450	2620	2790

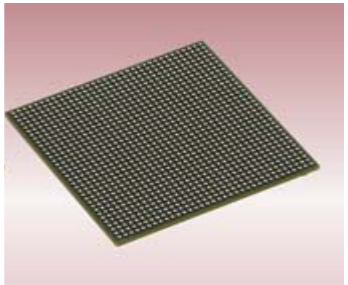
- **Clock :**
  - 10 Y + 5 X = 2400 ps clock latency
  - 20% of clock latency = On Die Variation

- **Data :**
  - travel from top-left to bottom right
  - register to register transfer

- **Can get 500MHz only from top-left to centre**
  - Need to limit speed or max. distance

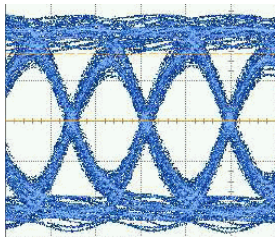
Power density

- **Telecom switching ASIC**
  - diesize 15 X 15mm = 2.25cm2
  - 18 Watt (@3.3V) = 6A
  - 20W (@1V) = 26 A
  - Power density : 17 W/cm2
  - Total design Power: Still increasing
    - Reason : complexity, Speed, dynamic power and leakage
  - Package : 40 x 40 mm
  - Power density : 2.4 W/cm2

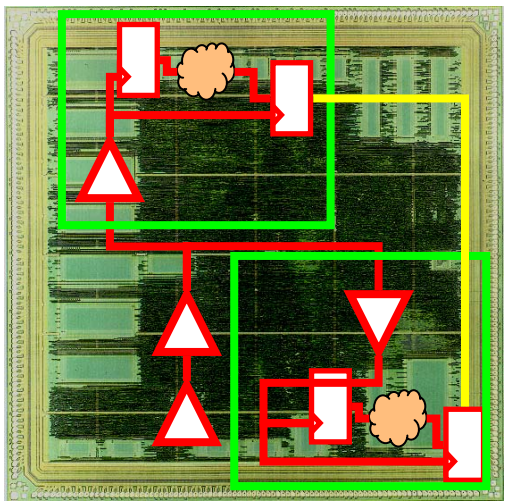


- **Electrical cooker plate**
  - 8 cm radius / 16cm diameter = 201 cm2
  - 1500 Watt, 220V = 6.8 A
  - Power density : 7.5 W/cm2

Future expectations



- **Interfaces speed to increase, but stay ~28G**
  - more parallel lanes
  - No chip-design without package
- **design granularity to become more coarse**
  - Past : transistor -> cells
  - Today : Intellectual Property
  - Future : SW controlled
- **New technology to allow further integration**
  - add-on to base CMOS (RF, Ultra-low power)
- **Implementation flows change**
  - Hierarchical : consider region like a chip on PCB
  - independently clocked regions
  - Power density increasing
  - consider peak vs. average datarate
  - Variations on chip : local/global similar range, wafer to wafer
  - Interconnect between regions : Low swing/differential at higher speed ?
  - Design style : synchronous or asynchronous ?



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THE POSSIBILITIES ARE INFINITE