



EMLC 2010
January, 18th 2010

**« Silicon ecosystems in Europe:
the key to competitiveness »**

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SITELESC Chairman, STMicroelectronics Crolles Dir.

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Agenda

- SCs: a true « Key Enabling Technology »
Political Moves and societal needs
- Europe's stand point in applications/systems
- CMOS technology challenges
- Equipment: Lithography R&D in Europe
- Silicon ecosystems in Europe
- The Grenoble-Crolles success story
- Conclusions


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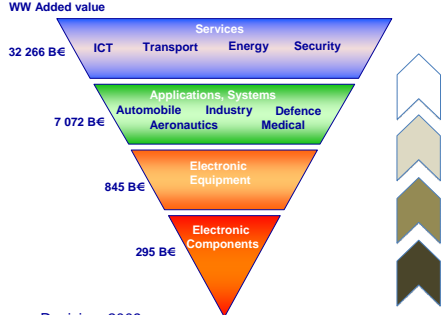
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Electronics leverage competitiveness and added value

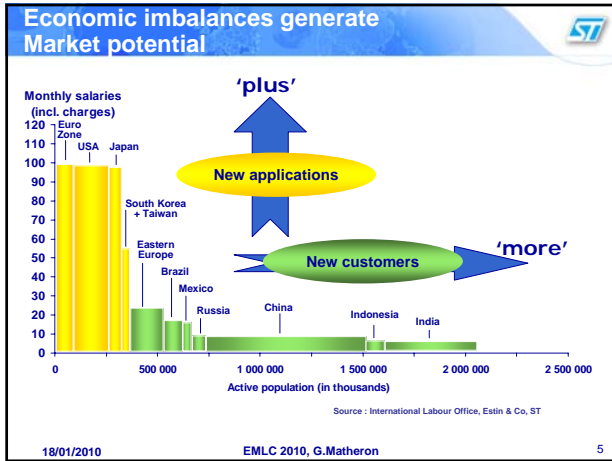


WW Added value

Category	Value (BE)
Services (ICT, Transport, Energy, Security)	32 266
Applications, Systems (Automobile, Industry, Defence, Aeronautics, Medical)	7 072
Electronic Equipment	845
Electronic Components	295

Source: Decision, 2009

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Key Enabling Technologies (KETs)

- European Commission communication (30 September 2009):

The Conclusions of the Competitiveness Council of 28 May 2009 pointed out "that it is of particular importance to maintain strong R&D investments in high-tech industries in Europe. They provide the most important manufacturing sectors with indispensable technologies" and looked forward "to the Commission's initiative to develop a pro-active policy for enabling high-tech industries".

Based on current global research and market trends the following could be regarded as the most strategically relevant KETs, given their economic potential, contribution to solving societal challenges and knowledge intensity:

Micro- and nanoelectronics, including semiconductors, are essential for all goods and services which need intelligent control in sectors as diverse as automotive and transportation, aeronautics and space. Smart industrial control systems permit more efficient management of electricity generation, storage, transport and consumption through intelligent electrical grids and devices;

Other highlighted KETs:
 Nanotechnology Photonics Advanced materials Biotechnology

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New opportunities for Electronics in Europe

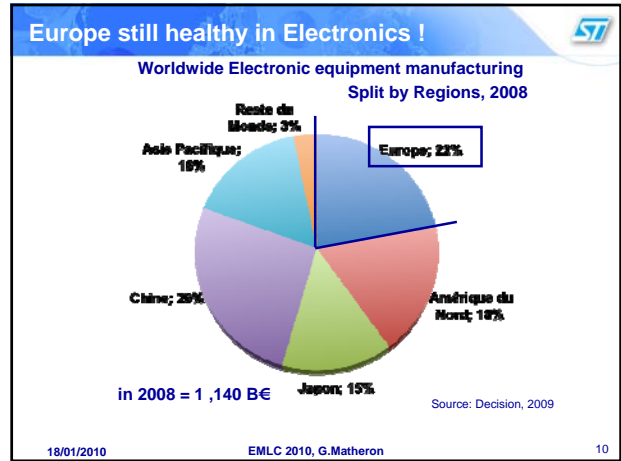
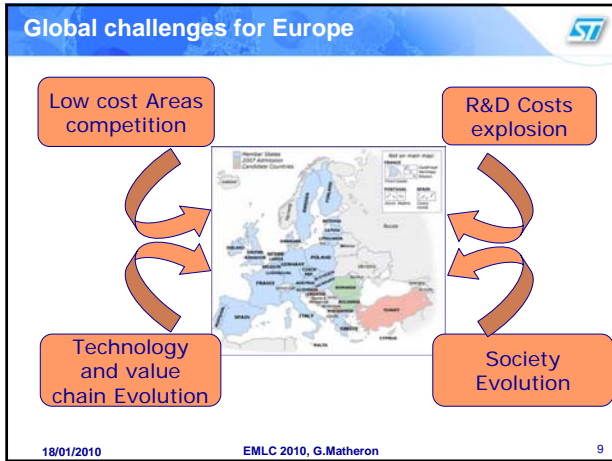
- **Tremendous applications of electronics** in front of us: energy savings, healthcare technologies, digital identityLife will never be the same as before!
- **Innovation** still very active in the 'old continent'. One issue: Transforming swiftly scientific firsts into market successes
- Electronics ideally positioned to enable a **Sustainable World**
- **Perfect fit between components and systems** manufacturers: Portfolio of technologies, Geographic proximity, Used to work together, a **>400 M people market** to experiment new standards
- All the **building blocks** are here.
- We need a strong **European industrial policy**

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European Semiconductor Industry fueled by European Market Leaderships

European Leadership in key industry sectors: Automotive, Industrial, Medical, Power & Wireless Communication

Electronic systems OEM rankings

AUTOMOTIVE REGION OF HQ	INDUSTRIAL REGION OF HQ	MEDICAL REGION OF HQ	POWER REGION OF HQ	WIRELESS COMMUNICATIONS REGION OF HQ
1 EUROPE	1 EUROPE	1 USA	1 EUROPE	1 EUROPE
2 JAPAN	2 USA	2 EUROPE	2 USA	2 USA
3 USA	3 EUROPE	3 EUROPE	3 EUROPE	3 KOREA
4 EUROPE	4 EUROPE	4 USA	4 EUROPE	4 EUROPE
5 USA	5 USA	5 JAPAN	5 USA	5 EUROPE
6 EUROPE	6 USA	6 JAPAN	6 TAIWAN	6 KOREA
7 USA	7 USA	7 USA	7 TAIWAN	7 JAPAN
8 EUROPE	8 JAPAN	8 JAPAN	8 JAPAN	8 EUROPE
9 EUROPE	9 USA	9 JAPAN	9 USA	9 JAPAN
10 USA	10 USA	10 USA	10 USA	10 CHINA

SOURCE: ISUPPLI 2009

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- ### Key challenges for Electronics in Europe
- Maintain innovation at the highest level (incremental & disruptive) with better university-industry transfers and R&D tax credits
 - Maintain a solid manufacturing infrastructure whenever possible (despite the overall environment making too often delocalisation the easiest and cheapest solution)
 - Leverage the advantage of the close coupling in Europe of demand / design / technology&innovation / manufacturing = build up and maintain solid « ecosystems »
 - Exchange rates: \$ vs. €! Competitiveness risk
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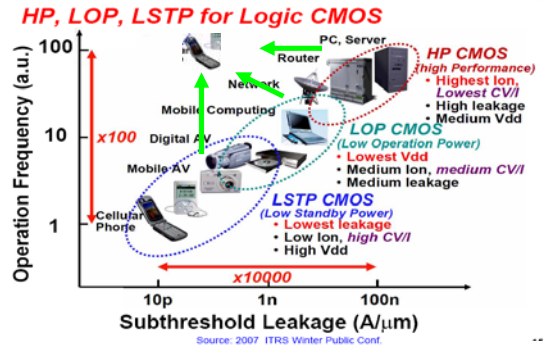
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Low Power Design Solution Needs

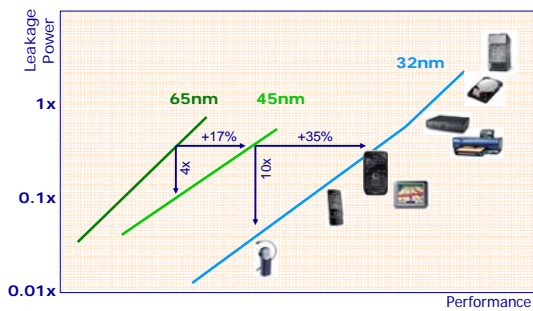


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CMOS Technology Evolution HKMG Benefits

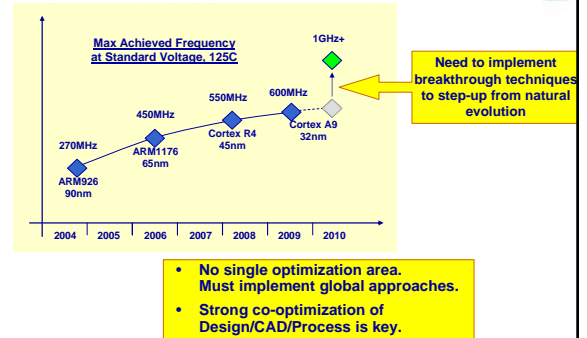


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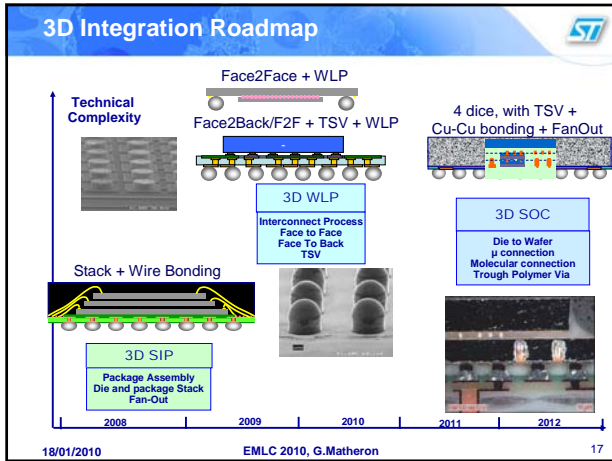
The GHz+ Implementation Challenge



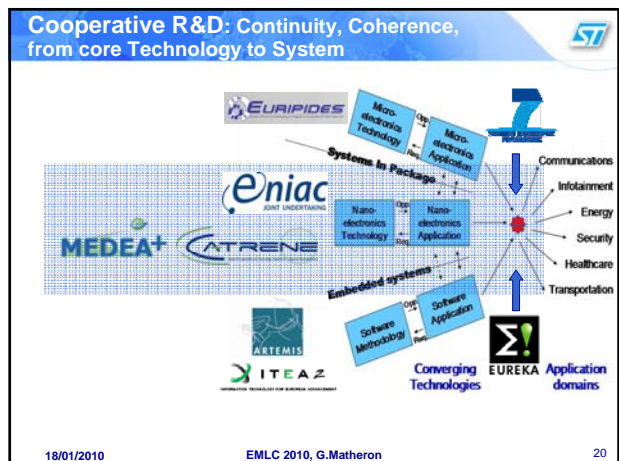
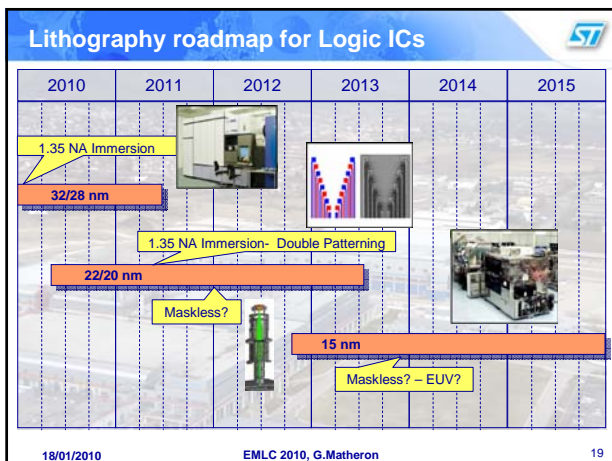
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European R&D cooperation in lithography



IMMERSION LITHOGRAPHY : LIQUID (MEDEA+) and LENS (ENIAC)

- **LIQUID : Lithography based on Quite extreme Ultra High NA optical Immersion Development (2005-2008). Effort : 495 Persons Years.**
 - Immersion lithography to produce 45nm feature with optical lithography.
 - First extension towards the 38nm node



- **LENS : Lithography Enhancement towards NanoScale (2009-2011)** started in 2009. Effort = 158 Persons Years
 - Two alternative approaches, both based on existing immersion scanners, for the patterning of 32nm and 22nm technology.



- Double exposure
- Pitch doubling

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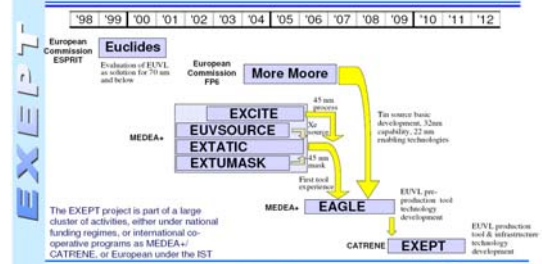
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European cooperation in EUV litho EXEPT project within CATRENE programme



EXEPT : 1326 Persons Years (the largest CATRENE project)

Previous complementary activities



Extrem UV Entry Point Technology development

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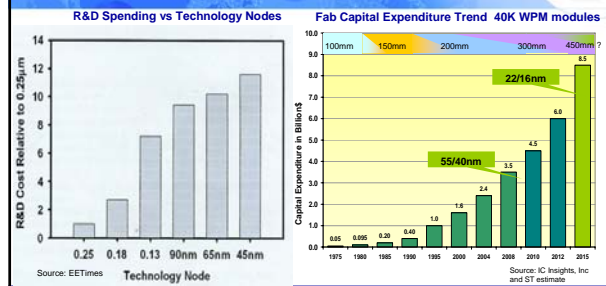
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Advanced CMOS challenges



R&D and manufacturing costs are exploding!

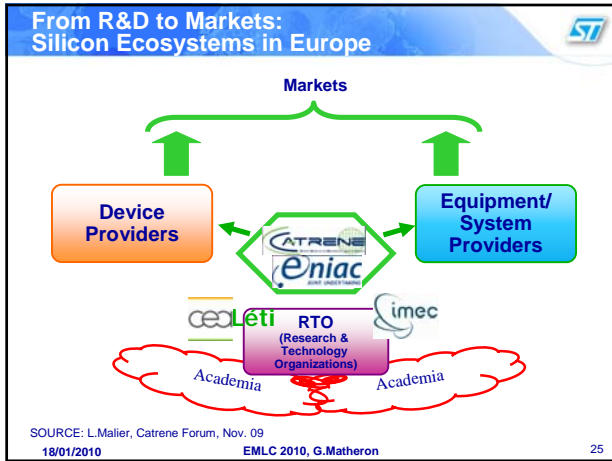
The answers:

1. Alliances for R&D and production
2. Robust Technologies, first-time silicon success and fast ramp-up in volume

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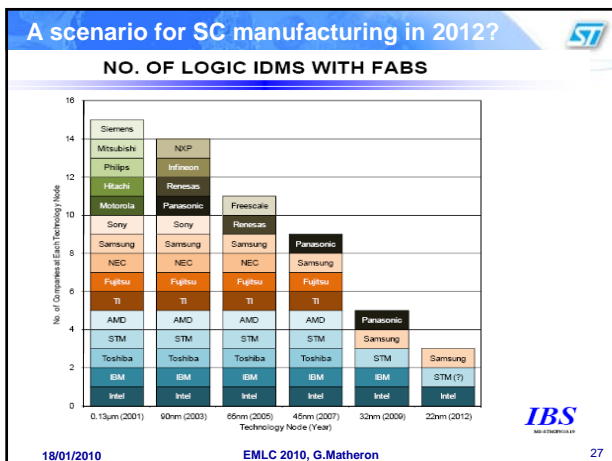


Industry Competitiveness: high again on the political agendas in Europe?

Silicon Saxony in Germany,
Point one in the Netherlands,
Minatec-Minalogic in France,
Catania cluster in Italy,
Eindhoven/Leuven/Aachen triangle...

- **Competitive clusters** mixing science, education and high-tech industry
- All aiming at better **efficiency** through focusing and political **visibility** through impact on added value and jobs created

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Changes in the European SC landscape

A world wide 'economic war' for mastering the micro-nanoelectronics industry

Transistors count: + 30% per year
 Transistor cost: -20% per year → Heavy R&D and industrial investment

2 sites only in Europe for general purpose SC manufacturing on 300mm wafers: Grenoble-Crolles and Dresden

Crolles has the ingredients for success:
 -IBM alliance
 -Coopération with LETI-MINATEC
 -National and local support: 'Nano2012'

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Microelectronics in Grenoble area

since the early ages

LETI/EFCIS	Thomson SC	SGS-Thomson	STMicroelectronics
1st Startup from LETI	Common Program with LETI	With LETI+CNET + Philips sc	Crolles 2 Alliance with NXP and FSL (2003-2007)
1st French MOS Technology	100 mm Wafers 1 μm Technology CMOS and BICMOS	200 mm Wafers 0.5 μm Technology MOS and BICMOS	IBM (2008-) 300 mm Wafers Submicron Technology
60's-70's	80's	90's	00's

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Employment impact in Rhone-Alpes area

ST Crolles 4000

+ Direct 4000

+ Indirect 8000

Total Rhône-Alpes ~ 16,000 jobs plus 9,000 in France

In addition, ST:
#1 employer in the area
#1 exporter in the area

Yearly expenses ~900 M€
incl > 500 M€ in Rhone-Alpes
Yearly local tax > 100 M€

Etude Reverdy et al. Dec 2007

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The loop to deliver value to the customers

Customer DVD player

Customer DVD player

BACK END

Malaysia, Philipina, China

DESIGN

DESCRIPTION

LAYOUT

MASKS GENERATION

FRONT END

SILICON WAFERS MANUFACTURING

FINAL TEST

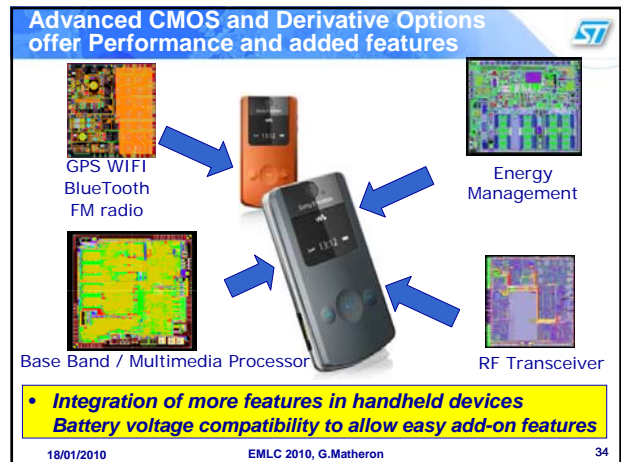
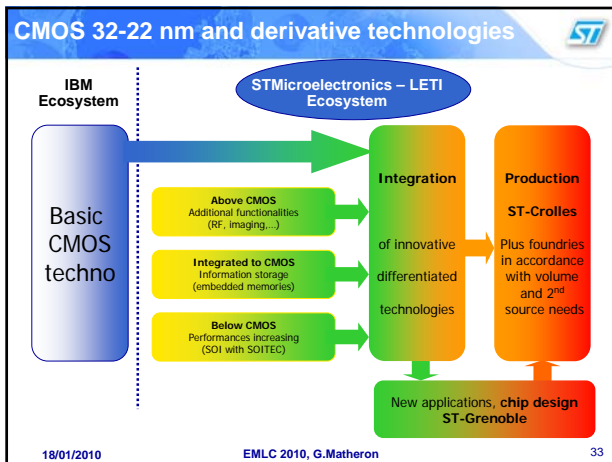
PACKAGING

WAFERS TEST

ST ERICSSON

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ST Crolles products and customers

ST Crolles products and customers

Customers: Thomson, Sony Ericsson, Nintendo, RIM, HP, Alcatel-Lucent, SIRIUS, NOKIA, SAMSUNG, CISCO SYSTEMS, LG, Apple, PHILIPS, Western Digital.

Product Categories: Communications, Computer Peripherals, Digital Consumer, Automotive.

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Cleanroom C200
200 mm Waters down to 120 nm 7200 w/w

Cleanroom C300
300 mm Waters down to 22 nm actual 2 800 w/w future 4 500 w/w

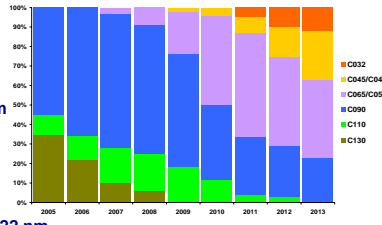
Cumulated investment ~4 B\$
5000 direct jobs on site

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ST Crolles 300 mm – Manufacturing



- **Volumes in 65/55nm**
 - Wireless
 - Consumer
 - Automotive
- **Mix change in 45/40 nm**
 - Wireless
 - Computer
- **Setting tools for 32/28/22 nm**
High K Metal Gate
- **Capacity** ~ 2800 wafers per week in 2009, 3600 w/w end 2010, up to 4500 w/w at full built-out



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ST Crolles answers to the Manufacturing challenges



- **Labor Cost** : High Productivity via Full Automation
- **Direct Labor Productivity** : via Operator Tasks Elimination (eg lot dispatching by computers) and Integrated WIP Management (MES, AMHS)
- **Labor Productivity and Flexibility** : via Computer Integrated Wafer Manufacturing
- **Dimension of Scale** : via competitive Fab sizing



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ST Crolles 300mm clean room views




Automatic transport of FOUP 300mm

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ST Crolles: Successful Design and Processing of SOCs



- **Teaming up talents:**
 - 200mm and 300mm Manufacturing
 - Advanced CMOS and Derivatives Technology development
 - Advanced CAD and Design Solutions
 - Labs for characterization, qualification and failure analysis
 - Process to Design Interface and Coordination
 - Process and Platform Qualification
 - Equipment to Process capability
- **Attracting partners:**
 - IBM on derivative value-added processes
 - ASML on immersion lithography and OCP
 - MENTOR Graphics on CAD close to process

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