Silicon nanowires patterning using UV-assisted graphoepitaxy DSA lithography

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Directed Self-Assembly (DSA) of block-copolymers, which is an affordable, simple and versatile lithography technique, is still highly investigated as a potential solution for the next generation node in the CMOS industry. DSA graphoepitaxy approach provides physical confinement between two "sidewalls" of fixed surface energy, which will generate well defined line/space structures with a variety of block copolymer materials and process environment [1,2,3]. However, most pilot-line compatible processes found in literature use Electron Beam Lithography (EBL) to generate the guiding structures because non-preferential grafted polymer layers can be incorporated between the HSQ resist (oxide guiding templates) and an inorganic transfer layer [4]. When using a 193nm-immersion lithography, such integration flow is not advised because the 193nm resists are acrylate-based resists that flow during the different annealing steps (CD uniformity and roughness performances impacted). Guiding templates made of standard immersion "hardmask" stack material with proper surface functionalization (sidewalls attractive to one block, bottom non-preferential) are rare.

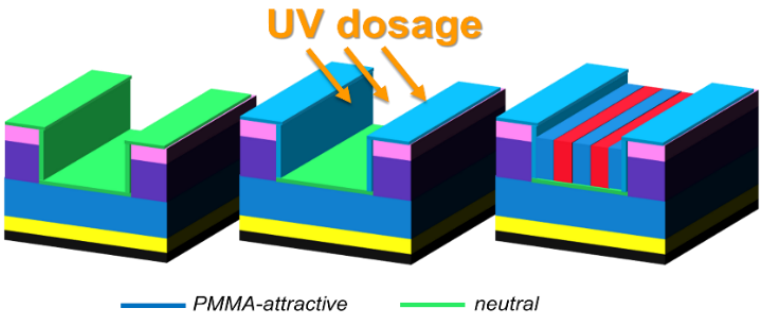
This work presents a smart surface modification technique for precise control over the surface affinity of topographic gratings used for the 300mm graphoepitaxy of PS-*b*-PMMA lamellar block copolymer (figure1). Guiding template manufactured for DSA of BCP is herein compatible with conventional 193nm dry lithography using standard SiARC/SOC materials stack. The method uses the property of various copolymers brushes to undergo UV-induced oxidation. Coupled with simulated intensity profiles inside a 3D grating structure, we present a way to precisely select the free surface energy distribution inside the grating. In this work, both homo-polystyrene and PS-*r*-PMMA thin films grafted to the surface of the grating are modified. The result is non-preferential wetting promoted at the bottom interface while sidewalls are left highly PMMA attractive. Topographic gratings for DSA combined with such UV-modification technique provides tremendous versatility in the final assembly and design of PS-*b*-PMMA line/space features.

This specific DSA process was implemented on the 300mm pilot line at Leti, and incorporated in a process flow for the creation of nanowires-like transistor as depicted in figure 2. Single crystalline silicon nanowires patterning on SiO_2 layer (from SOI substrate), achieved after the last Si etching step of the cut level, is especially highlighted (figure 3). The PS lamellae are also used as a mask through several etching steps to produce *in fine* high aspect-ratio structures inside silicon (figure 4). Different PS treatment (e-beam, UV or plasma curing) before etching transfer are moreover investigated in order to improve the final line roughness of Si fins. The best etching strategy will be selected based on the LWR-3σ and PSD studies done at each critical steps of the integration flow. As perspectives, the integration flow presented in this paper will be employed for patterning Si/SiGe nanowires.

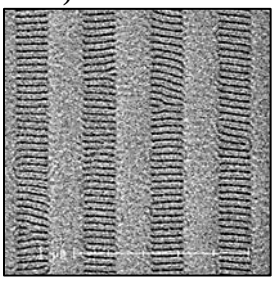
References:

[1] Jeong, S-J. et al. Directed self-assembly of block copolymers for next generation nanolithography. Materials today 2013, vol.16, n. 12
[2] Tsai, H. et al, two-dimensional pattern formation using graphoepitaxy of PS-b-PMMA block copolymers for advanced Finfet Device and circuit fabrication. ACS Nano 2014, 5(5), pp 5227-5232
[3] Girardot, C. et al. Pulsed Transfer Etching of PS−PDMS Block Copolymers Self-Assembled in 193 nm Lithography Stacks. ACS applied materials & interfaces 2014, 6, 16276-16282
[4] Tsai, H.-Y. et al. Sub-30 nm pitch line-space patterning of semiconductor and dielectric materials using directed self-assembly. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures 30, 06F205 (2012)

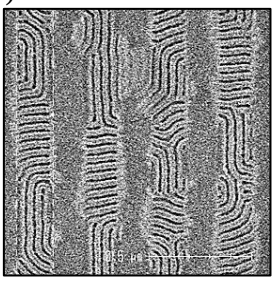
a) UV-assisted graphoepitaxy



b) Without UV



c) Intermediate UV dose



d) Strong UV dose

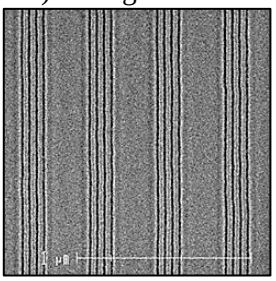
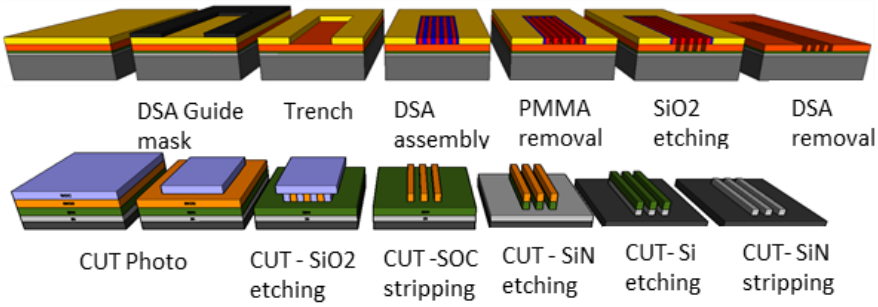


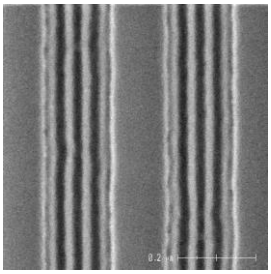
Figure 1: a) Principle of UV-assisted graphoepitaxy approach that consists in grafting a PS-*r*-PMMA layer and then exposing the pattern sidewall to UV exposure. b), c), d) Top-view CDSEM image after DSA without UV exposure, an intermediate UV dose and strong UV dose, respectively.

a)

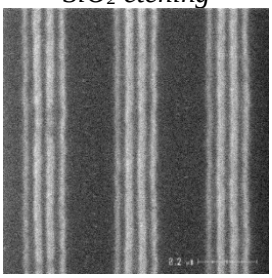


b)

PMMA removal



SiO_2 etching



Si etching

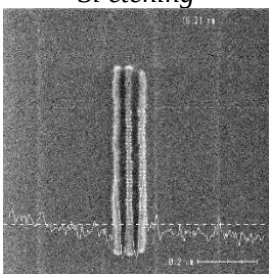


Figure 2: a) The DSA integration flow used to pattern silicon nanowires on SOI substrate b) Top-view CDSEM image after PMMA removal, SiO_2 and final Si etching with the cut level.

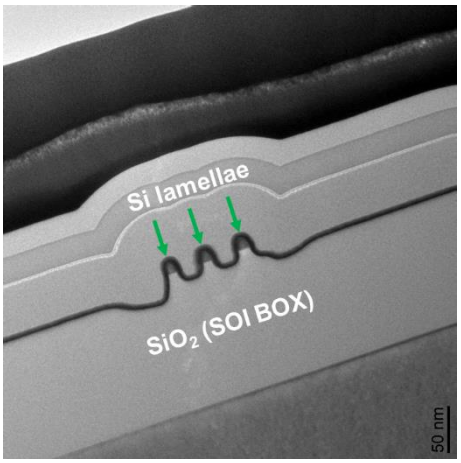
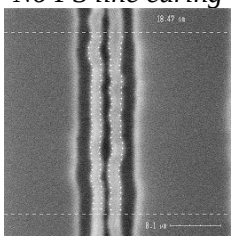


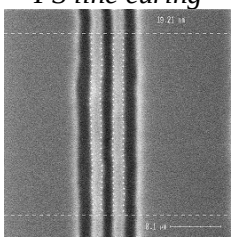
Figure 3: Cross-sectional TEM image of a 3-active Si fins achieved after the last Si etching step of the cut level.

a)

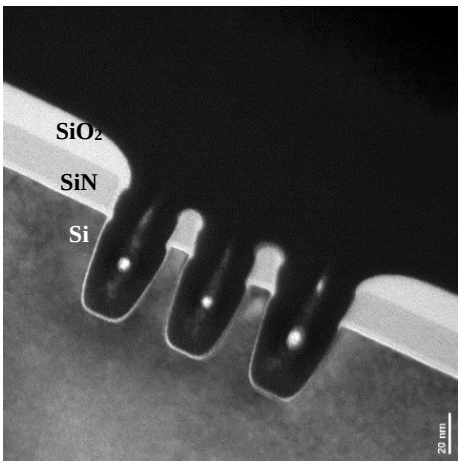
No PS line curing



PS line curing



b)



Si fin depth ~45nm
Si fin width ~10nm

Figure 4: a) Top-view CDSEM image after Si etching without and with PS line curing b) TEM image after Si etching showing two fins with a height of 45nm and a width of 10nm.