# 25th EUROPEAN SYMPOSIUM ON RELIABILITY OF ELECTRON DEVICES, FAILURE PHYSICS AND ANALYSIS

# ESREF 2014 Berlin, Germany

**September 29 – October 2, 2014**
**Technische Universität Berlin**
**www.esref2014.org**

## Programme

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**IEEE - Reliability Society**

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# Welcome Message from the Conference-Chair

ESREF 2014, the 25th anniversary of the European Symposium on Reliability of Electron Devices, Failure Physics and Analysis takes place in Berlin (Germany) from September 29 to October 2, 2014.

This international symposium continues to focus on recent developments and future directions in quality and reliability management of materials, devices and circuits for micro, nano, and optoelectronics. It provides a European forum for developing all aspects of reliability management and innovative analysis techniques for present and future electronic applications.

To characterize the dynamic potential of Berlin, I personally like to use the term “city of the unexpected”. Take on the surprise which Berlin offers its people, be it visitors or locals. And we, the organizers of ESREF 2014, take our part by making the conference itself an unexpected one – unexpectedly productive with 5 topical tracks, a special merge of tutorials, sessions and workshops. While focusing on rapidly growing topics like organic devices, 3D packaging and wide bandgap (power) devices, the conference is solidly grounded on industry oriented fundaments of microelectronics, power devices and respective failure analysis. For the first time, the European FIB User Group, EFUG, is integrated as one large topical track in the conference programme. Along with the 5 topical tracks come 4 tutorials, 3 workshops and altogether 8 invited presentations in order to create a unique innovative and well-structured programme.

Our main focus in 2014 is organic devices. Two keynote speeches, highlighting aspects from industry and research institutes, bring the huge progress in the world of organic devices to the ESREF community. On the other hand, a topical track on organic devices composed of tutorials, invited presentation, session and workshop may also create attraction to the organic device community that ESREF is the right place to communicate about reliability and failure analysis.

The technical programme of ESREF 2014 has been defined by the Technical Programme Committee, which was organized in ten subcommittees devoted to the various aspects of reliability physics and failure analysis, respectively. The papers presented at this conference are the result of a strict preselection from 248 extended summaries, followed by an extensive peer review and mentoring action supported by more than 150 specialists. The Technical Programme Committee has selected 92 works to be presented as oral papers and 55 as posters. This conference would not be possible without the commitment and expertise of all these contributors.

Two major innovations will be introduced in Berlin: For the first time at ESREF, we organize an Author's Gallery, a posted wall for the oral presenters in order to foster intense exchange about the presentations during the breaks after the sessions. Plus, we start with a smartphone app for advanced interaction throughout the programme, easier communication with the exhibitors and other special features that make ESREF in Berlin a contemporary conference of 2014.

Let the different spices served at ESREF2014 inspire you.
Last but not least, expand your Berlin experience with our social event arranged in the Berlin club scene area “Kulturbrauerei”.

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Christian Boit

# ESREF 2014 Committees

## Organizing Committee

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### B: Focused Ion Beam and European FIB User Group

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### C: Reliability & Failure Mechanisms of Organic Devices

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### D: Power Devices Reliability

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### E: Failure Analysis

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### F: Chip-Package Interactions and 3D Reliability & Failure Mechanisms

I. De WOLF IMEC (BE)
M. HECKER GLOBALFOUNDRIES (GER)

### G: Reliability & Failure Mechanisms in Packages and Assembly

H. FREMONT IMS, University of Bordeaux (FRA)
K. WEIDE-ZAAGE University of Hannover (GER)

### H: Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics

M. BAFLEUR LAAS (FRA)
O. AUBEL GLOBALFOUNDRIES (GER)

### I: Reliability & Failure Mechanisms of Wide Bandgap Devices

M. UREN University of Bristol (UK)

### J: Reliability & Failure Mechanisms of Photonic and Special Devices

F. ALTMANN Fraunhofer IWM Halle (GER)
M. VANZI University of Cagliari (IT)

### Poster Session and Best Poster Selection Chair:

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### Best Paper Selection Chair:

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# ESREF 2014 -
# The App for your mobile device

**Visit http://app.esref2014.org**
**on you smartphone, tablet or personal computer**

- to create and save your personal programme
- to get the full up-to-date information
- to search for speakers, presentations, and more
- to download the proceedings
- to connect with conference visitors, speakers, exhibitors
- to find your way around the venue or to the social event
- to receive instant messages about current conference events
- to experience one of the latest features of ESREF 2014

Works on Android 4.1, BlackBerry OS 10, iOS 6 and later, as well as on all mainstream desktop browsers.

# Author's Gallery

The Author's Gallery is an additional communication and exchange offer for oral presenters. In the break after the respective session, the presentration slides will be pinned to a movable wall like a poster in the exhibition/catering area. The organizers will take care of printing the slides and putting them up. The oral presenters should attend to their wall after the session is ending. Those participants of the audience who want to discuss topics of the presentations in more detail than the discussion during the session allows, may approach the presenter in the break for more intense exchange.

The Author's Gallery is one more instrument to contribute to a satisfying networking oppportunity at the conference. It adds the chance of intense exchange and discussion, so far characteristic for poster presentations, to the oral presentations as well.

# Keynote Speeches

Tue-A-08:30-**Keynote**
**Organic photovoltaic stability: Designed to last**
*Jan Gilot, Ronn Andriessen*
*Solliance/Holst Centre, Netherlands*

Since the discovery of Organic PhotoVoltaics (OPV) in the early 1990's, a lot of effort was put on further increasing the efficiency and to up-scale the devices to cells and modules. Today, power conversion efficiencies of 10 - 12% have been reported by using different processing approaches as well as different device architectures. Also up-scaling has been demonstrated on R2R coating and printing processes as well as R2R vacuum deposition. However, device, cell and module stability research only started around 2005 to become a serious point of attention for the OPV community. Initiatives like ISOS and round robins tests of OPV devices clearly showed the importance of standardizing test protocols in order to allow for better interlaboratory comparisons. This actually accelerated the progress in the field of understanding device failures as well as of identifying lifetime enhancing strategies for technical and chemical measures.

This presentation will explain, starting from a baseline OPV architecture, how layer-by-layer improvements can enhance both device performance and stability. We present how fundamental understanding of dominating failure mechanisms can guide material and architecture selection. Our insights into the degradation mechanisms stem from combinatorial device testing, systematic variation of ageing conditions as well as detailed analytical investigations. Combination of reliability-driven device design and a proper barrier and encapsulation technology are the foundations of an OPV designed to last.

Tue-A-09:10-**Keynote**
**OLEDs quality and reliability**
*Volker van Elsbergen*
*Philips Research, Aachen, Germany*

Organic light-emitting diodes (OLEDs) are a new and attractive class of solid-state light sources and they are emerging as a compelling candidate to replace conventional lighting systems. OLEDs provide potential for power-efficient large area light sources which will substantially contribute to energy efficient lighting. In addition, they combine revolutionary properties. They are thin and flat, and can be transparent, color-tunable, and flexible, enabling light sources with an unprecedented grade of flexibility in terms of design and application.

This talk will give an introduction to the OLED technology, present today's status of OLED lighting products, and will outline the future of OLED lighting. Special attention will be given to quality aspects, failure mechanisms, and reliability. Topics that will be covered comprise:

- operational lifetime
- uniformity of light emission
- shelf life and encapsulation
- reliability and short circuit behavior
- thermal stability
- instability of charge carrier injection and transport

## Invited Presentations

Tue-A-10:20-**Invited**
**Robustness Validation – A Physics of Failure Based Approach to Qualification**
*Werner Kanert (Infineon, GER)*

Tue-B-10:20-**Invited**
**Precise nanofabrication with multiple ion beams for advanced circuit edit**
*Huimeng Wu (Carl Zeiss LLC, Peabody MA, USA)*

Tue-C-13:10-**Invited**
**Massive scale organic photovoltaic manufacture**
*Frederik Christian Krebs (Tech. Univ. of Denmark, Roskilde, DK)*

Wed-A-13:30-**Invited**
**Enabling Higher Fault Isolation Resolution through Advanced Optics**
*Derryck T. Reid (Heriot-Watt University, UK)*

Wed-B-13:30-**Invited**
**Lifetime Modeling and Simulation of Power Modules for Hybrid Electrical / Electrical Vehicles**
*Markus Thoben (Infineon, GER)*

Wed-C-13:30-**Invited**
**Reliability of Wafer Level Chip Scale Packages**
*René Rongen (NXP Semiconductors, Nijmegen, NLD)*

Thu-A-08:30-**Invited**
**Performance - Reliability Trade-Offs for High-K RRAM**
*Nagarajan Raghavan (Singapore Univ. of Techn. and Design, SIN)*

Thu-C-08:30-**Invited**
**MEMS Reliability – Current Status and Challenges**
*Mervi Paulasto-Kröckel, Jue Li (University Aalto, FIN)*

## Tutorials

Tue-C-10:20-**Tutorial**
**Organic semiconductors: Novel materials for optoelectronic application**
*Selina Olthof (University Köln, GER;*
*Jens Meyer (Philips Research, Aachen, GER))*

Wed-A-08:30-**Tutorial**
**Asking The Right Questions (be)for(e) Failure Analysis**
*Peter Jacob (EMPA, Zürich, CHE)*

Wed-B-08:30-**Tutorial**
**Drift and reliability mechanisms in GaN based power devices for high voltage switching applications: The current understanding**
*Hans-Joachim Würfl (FBH, Berlin, GER)*

Wed-C-08:30-**Tutorial**
**Managing the Effects of Mechanical Stress on the Reliability of 3D IC Stacks**
*Ehrenfried Zschech (FhG IZFP, Dresden, GER); Valeriy Sukharev (Mentor Graphics,Fremont CA, USA); Riko Radojcic (San Diego CA, USA)*

## Exchange Papers

**Best Paper at the IEEE International Reliability Physics Symposium (IRPS) 2014**

Mon-A-18:20-Exchange
**Electromigration Failure of Circuit – Like Interconnects: Short Length Failure Time Distributions with Active Sinks and Reservoirs**
*Tony Oates and Ming-Hsien Lin*
*TSMC Ltd., Hsinchu, Taiwan*

**Best Paper related to Reliability at the IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) 2014**

Mon-A-18:40-Exchange
**Study of (correlated) Trap Sites in SILC, BTI and RTN in SiON and HKMG Devices**
*Erik Bury[1,2], Robin Degraeve[1], Moonju Cho[1], Ben Kaczer[1], Wolfgang Goes[3], Tibor Grasser[3], Naoto Horiguchi[1], Guido Groeseneken[1,2]*
*[1] IMEC, Belgium; [2] KU Leuven, Belgium;*
*[3] TU Wien, Austria*

**Outstanding Paper at the International Symposium for Testing and Failure Analysis (ISTFA) 2013**

Mon-A-19:00-Exchange
**Laser Voltage Imaging and Its Derivatives, Efficient Techniques to Address Defect On 28nm Technology**
*Thierry Parrassin[1], Guillaume Celi[1], Antoine Reverdy[2], Sylvain Dudit[1], Michel Vallet[1], Philippe Perdu[3], Dean Lewis[4]*
*[1] STMicroelectronics, Crolles, France; [2] Sector Technologies, Gieres, France; [3] Centre National d'Etudes Spatiales (CNES), Toulouse, France; [4] IMS laboratory, University of Bordeaux, Talence, France*

# Workshops

## 18th European FIB Users Group Meeting (EFUG2014)

Tue-B-13:10-14:50-**Workshop**

### Preliminary programme

**Problems and solutions when using FIB to prep nanostructures for TEM**
*Filip Lenrick, Lund University, Sweden*

**TEM Sample Preparation by Xe Plasma FIB**
*Salord[1], A. Delobbe[1], T. Hrncir[2], A. David[3], P. Sudraud[1], F. Lopour[2], [1]Orsay Physics, [2]TESCAN Brno, [3]Biophy Research*

**Maximizing Circuit Edit Efficiency by Adding Nanoprobing Capability**
*Andreas Rummel, Andrew J. Smith, Stephan Kleindiek Kleindiek, Germany*

**Extending Dualbeam Applications with the Helios PFIB**
*David Donnet, FEI Company*

Poster:

**Low temperature FIB cross section: application to indium micro bumps**
*L. Dantas de Morais, S. Chevalliez, S. Mouleres, SOFRADIR*

## 15th EUFANET Workshop

Wed-A-15:50-17:30-**Workshop**

### Copper sample prep challenges and solutions

You are cordially invited to attend and actively participate in this workshop and enjoy technical debates on copper sample preparation challenges and solutions. The preliminary agenda is:

**Overview of copper challenges, an intro**
*t.b.d*

**Chip access:** Comparative Study on Decapsulation for Copper and Silver Wire-Bonded Devices
*Michael Obein, Digit Concept, France*

**Cu as part of the defect:** Copper dendrites growth in package: physical isolation and characterization
*Giuseppe Giuga, STMicroelectronics, Italy*

**Preparation techniques for preservation of grain structure:**
Metallography issues, for instance for EBSD
*t.b.d.*

**Open questions**

**Wrap up**

## Annual ESREF-ECPE Power Devices Workshop

Wed-B-15:50-17:30-**Workshop**

### Reliability of Passive Devices

Experts in this field will make brief statements and then the audience and the experts will discuss issues of interest, as it was done at ESREF conferences in the 22 previous years.

**Introduction**
*Moderator: Eckhard Wolfgang, ECPE, Germany*

**Modeling of failures**
*Moderator: Mauro Ciappa, ETH Zurich/CH*

**Embedded Capacitors**
*Helene Fremont, IMS-Bordeaux, France*

**Film Capacitors**
*Patrick McCluskey, CALCE/USA*

**Corona Discharge in Film Capacitors with AC Load**
*Peter Jacob, EMPA, Switzerland*

## 3D & CPI & Harsh Environment Workshop

Thu-C-13:30-14:10-**Workshop**

### Preliminary programme

**Intro**
*Ingrid DeWolf, IMEC, Belgium*

**Can we live with stress in 3D/CPI?**
*Speaker: Ingrid DeWolf, IMEC, Belgium*

**Do we need dedicated (new) reliability tests (and detection methods) for 3D/CPI related failure mechanisms?**
*Speaker: Didier Bloch, LAAS, France*

**Are new failure analysis techniques such as magnetic imaging, GHz SAM, lock-in thermography sufficient to tackle all FA issues in 3D/CPI. What do we need more?**
*Speaker: Frank Altmann, Fraunhofer IWM Halle, Germany*

**Room: A • 18:00**

## Official Opening

*Christian Boit, Eckhard Langer, Philipp Scholz*

**Room: A • 18:20**

## Exchange Paper IEEE IRPS 2014

**Electromigration Failure of Circuit – Like Interconnects: Short Length Failure Time Distributions with Active Sinks and Reservoirs**
*Tony Oates and Ming-Hsien Lin*
*TSMC Ltd., Hsinchu, Taiwan*

**Room: A • 18:40**

## Exchange Paper IEEE IPFA 2014

**Study of (correlated) Trap Sites in SILC, BTI and RTN in SiON and HKMG Devices**
*Erik Bury[1,2], Robin Degraeve[1], Moonju Cho[1], Ben Kaczer[1], Wolfgang Goes[3], Tibor Grasser[3], Naoto Horiguchi[1], Guido Groeseneken[1,2]*
*[1] IMEC, Belgium; [2] KU Leuven, Belgium; [3] TU Wien, Austria*

**Room: A • 19:00**

## Exchange Paper ISTFA 2013

**Laser Voltage Imaging and Its Derivatives, Efficient Techniques to Address Defect On 28nm Technology**
*Thierry Parrassin[1], Guillaume Celi[1], Antoine Reverdy[2], Sylvain Dudit[1], Michel Vallet[1], Philippe Perdu[3], Dean Lewis[4]*
*[1] STMicroelectronics, Crolles, France;*
*[2] Sector Technologies, Gieres, France;*
*[3] Centre National d'Etudes Spatiales (CNES), Toulouse, France;*
*[4] IMS laboratory, University of Bordeaux, Talence, France*

**Room: A • 19:20**

## Exhibition Opening

*Jan Gaudestad*

ESREF 2014 is a conference where the commercial exhibition has been tightly integrated into the technical symposium. Among other measures taken at ESREF 2014, the Author's Corner and the poster session are set up in the exhibition area allowing for an intimate connection between presenters, exhibitors and symposium attendees.

**Exhibition Area • 19:40**

## Opening Reception

Networking is one of the core benefits when you attend a conference of your business community. So why not have a "Get together" right at the start of the conference? With food & drinks co-sponsored by Hamamatsu, we'll explore the area that we will use in the days to come and the exhibitors will already have their booths open.

Tue-A-08:30

**Keynote 1** **Organic photovoltaic stability: Designed to last**

*Jan Gilot, Ronn Andriessen, Solliance/Holst Centre, NLD*

Tue-A-09:10

**Keynote 2** **OLEDs quality and reliability**

*Volker van Elsbergen, Philips Research, Aachen, GER*

**09:50 - 10:20 Coffee Break • Exhibition area**

**Room: A**

## Quality and Reliability Assessment – Techniques and Methods for Devices and Systems

*Chairs: Fausto Fantini, Werner Kanert*

Tue-A-10:20-**Invited**
**Robustness Validation – A Physics of Failure Based Approach to Qualification**
*Werner Kanert*
*Infineon, Germany*

Tue-A-10:50
**A design tool to study the impact of mission-profile on the reliability of SiC-based PV-inverter devices**
*Nicolae Cristian Sintamarean[1], Huai Wang[1], Frede Blaabjerg[1], Peter De Place Rimmen[2]*
*[1] Aalborg University, Denmark; [2] Danfoss Power Electronics A/S, Denmark*

Tue-A-11:10
**Copper wire interconnect reliability evaluation using in-situ HTSL tests**
*Amar Mavinkurve, Leon Goumans, Orla O'Halloran, Rene Rongen, Mark-Luke Farrugia*
*NXP Semiconductors, Netherlands*

Tue-A-11:30
**Robust Electromigration Reliability Through Engineering Optimization**
*Wee Loon Ng[1], Kheng Chok Tee[1], Junfeng Liu[1], Yong Chiang Ee[1], Oliver Aubel[2], Chuan Seng Tan[3], Kin Leong Pey[4]*
*[1] GLOBALFOUNDRIES, Singapore; [2] GLOBALFOUNDRIES, Germany; [3] Nanyang Technological University, Singapore; [4] Singapore University of Technology and Design, Singapore*

Tue-A-11:50
**Empirical BEOL-TDDB evaluation based on I(t)-trace analysis**
*Oliver Aubel[1], Armand Beyer[1], Georg Talut[1], Martin Gall[2]*
*[1] GLOBALFOUNDRIES, Germany; [2] Fraunhofer IKTS, Germany*

**Room: B**

## Focused Ion Beam and European FIB User Group

*Chairs: Hugo Bender, Frank Altmann*

Tue-B-10:20-**Invited**
**Precise nanofabrication with multiple ion beams for advanced circuit edit**
*Huimeng Wu, David Ferranti, Lewis Stern*
*Carl Zeiss Microscopy, LLC, United States*

Tue-B-10:50
**Advanced FIB sample preparation techniques for high resolution TEM investigations of HEMT device structures**
*Michél Simon-Najasek[1], Frank Altmann[1], Susanne Hübner[1], Andreas Graff[1], Helmut Jung[2]*
*[1] Fraunhofer Institute for Mechanics of Materials IWM, Germany; [2] United Monolithic Semiconductors GmbH, Germany*

Tue-B-11:10
**Local thickness and composition analysis of TEM lamellas in the FIB**
*Christian Lang[1], Matthew Hiscock[1], Cheryl Hartfield[2], Michael Dawson[2]*
*[1] Oxford Instruments, United Kingdom; [2] Oxford Instruments, United States*

Tue-B-11:30
**Efficient and flexible Focused Ion Beam micromachining of Solid Immersion Lenses in various bulk semiconductor materials – an adaptive calibration algorithm**
*Philipp Scholz[1], Norbert Herfurth[1], Michael Sadowski[1], Ted Lundquist[2], Uwe Kerst[1], Christian Boit[1]*
*[1] Technische Universität Berlin, Germany; [2] DCG Systems, United States*

Tue-B-11:50
**Focused ion beam contact to non-volatile memory cells**
*Clemens Helfmeier[1], Rudolf Schlangen[2], Christian Boit[1]*
*[1] Technische Universität Berlin, Germany; [2] Nvidia, United States*

**Room: C**

## Reliability & Failure Mechanisms of Organic Devices

*Chairs: Philippe Perdu, Jerome Touzel*

Tue-C-10:20-**Tutorial**
**Organic semiconductors: Novel materials for optoelectronic application**
*Selina Olthof[1], Jens Meyer[2]*
*[1] University Köln, Germany;*
*[2] Philips Research, Aachen, Germany*

**12:10 - 13:10 Lunch Break • Room: Exhibition Area**

Room: A

## Quality and Reliability Assessment – Techniques and Methods for Devices and Systems

*Chairs: Fausto Fantini, Werner Kanert*

Tue-A-13:10
**As-grown donor-like traps in low-k dielectrics and their impact on intrinsic TDDB reliability**
*Baojun Tang[1], Kristof Croes[1], Yohan Barbarin[1], Yunqi Wang[2], Robin Degraeve[1], Yunlong Li[1], Maria Toledano-Luque[1], Thomas Kauerauf[1], Juergen Bommels[1], Zsolt Tokei[1], Ingrid De Wolf[1]*
*[1]IMEC, Belgium;*
*[2]University of Oxford, United Kingdom*

Tue-A-13:30
**Physics-of-Failure Assessment Methodology for Power Electronic Systems**
*David Squiller[1], Hannes Greve[1], Patrick McCluskey[1], Elena Mengotti[2]*
*[1]The University of Maryland, College Park, United States;*
*[2]ABB Switzerland Ltd., Corporate Research, Switzerland*

Tue-A-13:50
**Influence of dicing damages on the thermo-mechanical reliability of bare-chip assemblies**
*Matthias Steiert, Jürgen Wilde*
*University of Freiburg, Germany*

Tue-A-14:10
**Study of EM void nucleation and mechanic relaxation effects**
*Giulio Marti[1], Lucile Arnaud[1], Yves Wouters[2]*
*[1]STMicroelectronics, France;*
*[2]SIMAP, France*

Tue-A-14:30
**Assessment methodology of the lateral migration component in data retention of 3D SONOS memories**
*Lifang Liu*
*IMEC, Belgium*

Room: B

## Focused Ion Beam and European FIB User Group

*Chairs: Hugo Bender, Frank Altmann*

Tue-B-13:20-15:40-**Workshop**

European FIB User Group Workshop
see details on page 11

Room: C

## Reliability & Failure Mechanisms of Organic Devices

*Chairs: Thomas Riedl, Ralf Heiderhoff*

Tue-C-13:10-**Invited**
**Massive scale OPV manufacture**
*Frederik C. Krebs*
*Technical University of Denmark, Denmark*

Tue-C-13:50
**Transparent conductive gas diffusion barriers**
*Andreas Behrendt, Christian Friedenberger, Tobias Gahlmann, Sara Trost, Andreas Polywka, Patrick Görrn, Thomas Riedl*
*University of Wuppertal, Germany*

Tue-C-14:10
**Comprehensive analysis of the efficiency roll-off in phosphorescent organic light-emitting diodes**
*Sebastian Wehrmeister*
*University of Augsburg, Germany*

Tue-C-14:30
**Investigating UV Stability of Polyfluorene Triarlyamine-based Blue Light-emitting Copolymers**
*Nathan Chander[1], Michael Cass[2], Ji-Seon Kim[1]*
*[1]Imperial College London, United Kingdom; [2]Cambridge Display Technology, United Kingdom*

**14:50 - 15:20 Coffee Break • Exhibition Area**

## Room: A

### Quality and Reliability Assessment – Techniques and Methods for Devices and Systems

*Chairs: Fausto Fantini, Werner Kanert*

Tue-A-15:20
**Power Grid Redundant Path Contribution in System on Chip (SoC) Robustness against Electromigration**
*Boukary Ouattara[1], Lise Doyen[1], David Ney[1], Habib Mehrez[2], Pirouz Bazargan-Sabet[2]*
*[1]STMicroelectronics, France; [2] Laboratory of Computer Sciences, France*

Tue-A-15:40
**Single-parameter model for the post-breakdown conduction characteristics of HoTiOx-based MIM capacitors**
*Enrique Miranda*
*Universitat Autonoma de Barcelona, Spain*

Tue-A-16:00
**Impact of local structural and electrical property of grain boundaries in poly-crystalline HfO2 on reliability of SiOx interfacial layer**
*Shubhakar Kalya[1], Kin Leong Pey[1], Raghavan Nagarajan[1], Michel Bosman[2], Sunil Singh Kushvaha[2], Zhongrui Wang[3], Sean Joseph O'Shea[2]*
*[1]SUTD, Singapore; [2] IMRE, Singapore; [3]NTU, Singapore*

Tue-A-16:20
**Accelerated Degradation data of SiC MOSFETs for Lifetime and Remaining Useful Life Assessment**
*Thomas Santini[1], Sébastien Morand[1], Mitra Fouladirad[2], Luong-Viêt Phung[3], Florent Miller[1], Bruno Foucher[1], Antoine Grall[2], Bruno Allard[3]*
*[1]Airbus Group Innovations, France; [2]Université de Technologie de Troyes, France; [3] Laboratoire Ampère, France*

Tue-A-16:40
**Degradation Behaviour in Upstream/ Downstream Via Test Structures**
*Jörg Kludt[1], Kirsten Weide-Zaage[1], Markus Ackermann[2], Verena Hein[2], Christian Kovács[2]*
*[1]Leibniz Universität Hannover, Germany; [2]X-FAB Semiconductor Foundries AG, Germany*

## Room: B

### Power Devices Reliability Passive & Supercapacitor

*Chairs: Mauro Ciappa, Reinhold Bayerer*

Tue-B-15:20
**Prediction of Supercapacitors Floating Ageing with Surface Electrode Interface based Ageing Law**
*Ronan German[1], Ali Sari[1], Pascal Venet[1], Mohamed Ayadi[2], Olivier Briat[3], Jean-Michel Vinassa[3]*
*[1]Université Lyon , France; [2]IFSTTAR Satory, France; [3]Université de Bordeaux, France*

Tue-B-15:40
**Eliminate Infant Mortality in Metallized Film Capacitors by defect detection**
*Patrick McCluskey, Nga Man Li*
*University of Maryland, United States*

Tue-B-16:00
**Metallized film capacitors ageing law based on capacitance degradation**
*Maawad Makdessi, Ali Sari, Pascal Venet*
*Université Lyon 1, France*

## Room: C

### Reliability & Failure Mechanisms of Organic Devices

*Chairs: Thomas Riedl, Ralf Heiderhoff*

Tue-C-15:20
**Temporal phenomena in organic field-effect transistors through Kelvin-Probe Force Microscopy**
*Christian Melzer[1], Christopher Siol[2], Heinz von Seggern[2]*
*[1]Universität Heidelberg, Germany; [2]Technische Universität Darmstadt, Germany*

Tue-C-15:40
**Neutron Radiation Tolerance of Organic Field Effect Transitors**
*Giuseppe Paterno[1], Valentina Robbiano[1], Victoria Garcia Sakai[2], Franco Cacialli[1]*
*[1]University College London, United Kingdom; [2]ISIS-Neutron and Muon Source, United Kingdom*

Tue-C-16:00
**Stress-Induced Degradation of p- and n-type Organic Thin-Film-Transistors in the ON and OFF States**
*Nicola Wrachien[1], Andrea Cester[1], Gaudenzio Meneghesso[1], Riccardo D'Alpaos[2], Andrea Stefani[2], Guido Turatti[2], Michele Muccini[3]*
*[1]University of Padova, Italy; [2] ETC, Italy; [3] CNR and ETC, Italy*

Tue-C-16:20
**Hybrid VCSEL and DFB organic microlasers**
*Tim Wagner, Andreas Mischok, Markas Sudzius, Robert Brueckner, Vadim G. Lyssenko, Hartmut Froeb, Karl Leo*
*Institut fuer Angewandte Photophysik, TU Dresden, Germany*

**17:00 - 17:30 Coffee Break • Exhibition Area**

**17:30 - 19:00 Poster Session • Exhibition Area**

## Quality and Reliability Assessment – Techniques and Methods for Devices and Systems

Tue-Expo-17:30-P01
**Prognostic Methodology for Remaining Useful Life Estimation of Retention Loss in Nanoscale Resistive Switching Memory**
*Nagarajan Raghavan[1], Daniel Frey[2], Kin Leong Pey[1]*
*[1] Singapore University of Technology and Design, Singapore; [2] Massachusetts Institute of Technology, United States*

Tue-Expo-17:30-P02
**Analytical stress characterization after different chip separation methods**
*Michael Fügl[1], Gunther Mackh[2], Elke Meissner[3], Lothar Frey[3]*
*[1] University Erlangen, Germany; [2] Infineon Technologies AG, Germany; [3] Fraunhofer IISB, Germany*

Tue-Expo-17:30-P03
**Monolithic integrable capacitive humidity sensing method for material characterization of dielectric thin films**
*Andreas Rückerl, Sophia Huppmann, Roland Zeisel, Simeon Katz*
*Osram Opto Semiconductors GmbH, Germany*

Tue-Expo-17:30-P04
**Influence of temperature and dose rate on the degradation of BiCMOS operational amplifiers during total ionizing dose testing**
*Aleksandr S. Petrov, Konstantin I. Tapero, Viktor N. Ulimov*
*Research Institute of Scientific Instruments, Russian Federation*

Tue-Expo-17:30-P05
**State of Health Online Estimation of Energy Storage System using Balancing Circuit**
*Shili Seima, Hijazi Alaa, Venet Pascal*
*Laboratoire AMPERE, France*

Tue-Expo-17:30-P06
**RTN distribution comparison for bulk, FDSOI and FinFETs devices**
*Louis Gerrer[1], Salvatore Amoroso[1], Razaidi Hussin[2], Asen Asenov[3]*
*[1] University of Glasgow - Device Modelling Group, United Kingdom; [2] University of Malaysia, United Kingdom; [3] GoldStandard Simulations, United Kingdom*

Tue-Expo-17:30-P07
**Comparison of in-situ measurement techniques of the solder joint reliability under the thermo-mechanical stresses**
*Ning Duan*
*NXP Semiconductors, Netherlands*

Tue-Expo-17:30-P08
**Vacuum quality evaluation for micro-bolometer thermal imager sensors**
*Michael Elßner*
*Fraunhofer IMS, Germany*

Tue-Expo-17:30-P09
**Assessment of Mechanical Reliability of Surface Mounted Capacitor by an Accelerated Shear Fatigue Test Technique**
*Julien Magnien, Golta Khatibi*
*University of Vienna, Austria*

Tue-Expo-17:30-P10
**µ-Raman spectroscopy for stress analysis in high power silicon devices**
*Thierry Kociniewski[1], Jeff Moussodji[2], Zoubir Khatir[2]*
*[1] UVSQ - GEMaC / IFSTTAR - LTN, France; [2] IFSTTAR - LTN, France*

Tue-Expo-17:30-P11
**Compact model of magnetic tunnel junction with stochastic spin transfer torque switching for reliability analyses**
*You Wang[1], Yue Zhang[1], Erya Deng[1], Jacques-Olivier Klein[1], Lirida Alves De Barros Naviner[2], Weisheng Zhao[1]*
*[1] Univ. Paris-Sud, France; [2] Institut TELECOM, Télécom ParisTech, France*

## Reliability & Failure Mechanisms of Organic Devices

Tue-Expo-17:30-P12
**Air-stable, high current density, solution-processable, amorphous organic rectifying diodes (ORDs) for low-cost fabrication of flexible passive low frequency RFID tags.**
*Indranil Ronnie Bose[1], Kornelius Tetzner[2], Kathrin Borner[1], Karlheinz Bock[1]*
*[1] Fraunhofer EMFT, Germany; [2] TU Berlin, Germany*

Tue-Expo-17:30-P13
**Reliability and operational stability of all-inkjet printed organic transistors**
*Henrique Leonel Gomes[1], Maria Do Carmo Medeiros[2], Fausta Loffredo[3], Riccardo. Miscioscia[3], Fulvia Villani[3], Carme Martínez-Domingo[4], Eloi Ramom[4], Enrico Sowade[5], Kalayan Mitra[5], Ian Mcculloch[6], Jordi Carrabina[4]*
*[1] Universidade do Algarve, Portugal; [2] Universidade de Coimbra, Portugal; [3] ENEA, Portici Research Center, Italy; [4] CAIAC, Universitat Autònoma de Barcelona, Spain; [5] Chemnitz University of Technology, Germany; [6] Department of Chemistry, Imperial College London, United Kingdom*

## Failure Analysis

Tue-Expo-17:30-P14
**SEM-based nanoprobing on 32 and 28 nm CMOS devices – Challenges for Semiconductors Failure Analysis**
*Erik Paul*
*GLOBALFOUNDRIES, Germany*

Tue-Expo-17:30-P15
**Acoustic detection of micro-cracks in small electronic devices**
*Georg Michael Reuther, Reinhard Pufall, Michael Goroll*
*Infineon Technologies AG, Germany*

Tue-Expo-17:30-P16
**High resolution imaging of dopant and depletion layer distributions in SiC power MOSFET using super-higher-order nonlinear dielectric microscopy**
*Norimichi Chinone[1], Takashi Nakamura[2], Yasuo Cho[1]*
*[1] Tohoku Univ., Japan; [2] ROHM Co., Ltd., Japan*

Tue-Expo-17:30-P17
**Quantifying the Limits of Scanning Electron Microscopy for the Metrology of Critical Dimensions of Photoresist Structures in the Nanometer Range**
*Mauro Ciappa[1], Emre Ilguensatiroglu[1], Alexey Illarionov[2]*
*[1] ETH Zurich, Switzerland; [2] Integrated Systems Laboratory, ETH, Switzerland*

Tue-Expo-17:30-P18
**Scanning Spreading Resistance Microscopy for failure analysis of nLDMOS devices with decreased breakdown voltage**
*Stefan Doering[1], Ralf Rudolf[1], Martin Pinkert[1], Hagen Roetz[1], Catejan Wagner[1], Stefan Eckl[1], Marc Strasser[2], Andre Wachowiak[3], Thomas Mikolajick[4]*
*[1] Infineon Technologies Dresden GmbH, Germany; [2] Infineon Technologies AG, Germany; [3] NaMLab GmbH, Germany; [4] TU Dresden, Germany*

Tue-Expo-17:30-P19
**Electromigration in Open TSVs**
*Wolfhard H. Zisser, Hajdin Ceric, Josef Weinbub, Siegfried Selberherr*
*Institute for Microelectronics, TU Wien, Austria*

Tue-Expo-17:30-P20
**Copper dendrites growth in LLT (Lead Lock Tape) embedded in QFP package: physical identification and characterization**
*Claudio Savoia[1], Giuseppe Giuga[1], Fabio Tormen[1], Luca Merlo[2]*
*[1] STMicrolectronics, Italy;*
*[2] University of Milano, Italy*

## Power Devices Reliability

Tue-Expo-17:30-P21
**Joining and package technology for 175°C Tj increasing reliability in automotive applications**
*Peter Dietrich*
*Fuji Electric Europe GmbH, Germany*

Tue-Expo-17:30-P22
**Overload Robust IGBT Design for SSCB Application**
*Ihsan Supono[1], Jesus Urresti[1], Alberto Castellazzi[1], David Flores[2]*
*[1] University of Nottingham, United Kingdom; [2] IMB-CNM, Spain*

Tue-Expo-17:30-P23
**Reliability enhancement by integrated liquid cooling in power IGBT modules for hybrid and electric vehicles**
*Yangang Wang, Steve Jones*
*Dynex Semiconductor ltd, United Kingdom*

Tue-Expo-17:30-P24
**Robust snubber-less power converter design with soft-switching avalanche-rugged Si and SiC Power MOSFETs**
*Francesco Giuliani[1], Dipankar De[1], Nicola Delmonte[2], Alberto Castellazzi[1], Paolo Cova[2]*
*[1] University of Nottingham, United Kingdom; [2] University of Parma, Italy*

Tue-Expo-17:30-P25
**Solder void position and size effects on electro thermal behaviour of MOSFET transistors in forward bias conditions**
*Son-Ha Tran[1], Laurent Dupont[2], Zoubir Khatir[2]*
*[1] VeDeCoM, France; [2] IFSTTAR-LTN, France*

Tue-Expo-17:30-P26
**Turn-off Instabilities in large area 600V IGBTs**
*Carmine Abbate[1], Francesco Iannuzzo[1], Giovanni Busatto[1], Annunziata Sanseverino[1], Francesco Velardi[1], Cesare Ronsisvalle[2], James Victory[2]*
*[1] University of Cassino and Southern Lazio, Italy; [2] Fairchild Semiconductor, Germany*

Tue-Expo-17:30-P27
**Impact of active thermal management on power electronics design**
*Markus Andresen, Marco Liserre*
*Christian-Albrechts-University of Kiel, Germany*

Tue-Expo-17:30-P28
**NBTI Degradation in STI-based LDMOSFETs**
*Yandong He, Ganggang Zhang, Xing Zhang*
*Institute of Microelectronics, Peking University, China*

Tue-Expo-17:30-P29
**Description of Supercapacitor Performance Degradation Rate during Thermal Cycling Under Constant Voltage Ageing Test**
*Mohamed Ayadi[1], Olivier Briat[2], Richard Lallemand[3], Akram Eddahech[4], Ronan German[5], Gerard Coquery[3], Jean-Michel Vinassa[6]*
*[1] Ifsttar-IMS Laboratories, France; [2] Laboratoire IMS CNRS, France; [3] IFSTTAR Versailles Satory, France; [4] IMS Laboratory, France; [5] Université Lyon 1, France; [6] University of Bordeaux, France*

## Chip-Package Interactions and 3D Reliability & Failure Mechanisms

Tue-Expo-17:30-P30
**Study of the UBM to copper interface robustness of solder bumps in flip chip packages**
*Joerg Dreybrodt, Yves Dupraz*
*EM Microelectronic Marin SA, Switzerland*

Tue-Expo-17:30-P31
**A study of through package vias in a glass interposer for multifunctional and miniaturized systems**
*Abderrahim El Amrani, Abdellah Benali, Mohsine Bouya, Mustapha Faqir*
*Université Internationale de Rabat, Morocco*

Tue-Expo-17:30-P32
**Evaluation new Corner Stress Relief Structure Layout for high robust Metallization**
*Verena Hein[1], Kirsten Weide-Zaage[2], Joerg Kludt[2]*
*[1] X-FAB Semiconductor Foundries AG, Germany; [2] University Hannover, Germany*

Tue-Expo-17:30-P33
**Sn Whisker evaluation in 3D micro-bumped structures**
*George Vakanas[1], Joke De Messemaeker[2], Bjorn Vandecasteele[2], Geert Willems[2], Mark Ashworth[3], Geoffrey Wilcox[3], Ingrid De Wolf[2], David Schaubroek[2]*
*[1] Intel assignee to imec (3D), United States; [2] IMEC, Belgium; [3] Loughborough University, United Kingdom*

## Reliability & Failure Mechanisms in Packages and Assembly

Tue-Expo-17:30-P34
**Thermal and Mechanical Effects of Voids within Flip Chip Soldering in LED Packages**
*Yang Liu[1], Stanley Y. Y. Leung[2], Jia Zhao[3], Cell K.Y. Wong[2], Cadmus A. Yuan[4], Guoqi Zhang[5], Fenglian Sun[1], Liangliang Luo[1]*
*[1] Harbin University of Science and Technology, China; [2] Beijing Research Centre, Delft University of Technology, China; [3] State Key Laboratory of Solid State Lighting, China; [4] Institute of Semiconductors, Chinese Academy of Sciences, China; [5] DIMES Center for SSL Technologies, Delft University of Technology, Netherlands*

Tue-Expo-17:30-P35
**Influence of mobile ion in organic material used in semiconductor devices**
*Yik Yee Tan[1], Claudia Keller[2], Kok Seng Teo[1], Sivanyanam Rajamanickam[1]*
*[1] Infineon Technologies, Malaysia; [2] Infineon Technologies, Germany*

Tue-Expo-17:30-P36
**A three-scale approach to the numerical simulation of metallic bonding for MEMS packaging**
*Alberto Corigliano[1], Aldo Ghisi[1], Stefano Mariani[1], Giorgio Allegato[2], Laura Oggioni[2]*
*[1] Politecnico di Milano, Italy; [2] STMicroelectronics, Italy*

Tue-Expo-17:30-P37
**Microstructure of Sn-1Ag-0.5Cu Solder Alloy Bearing Fe Under Salt Spray Test**
*Nor Ilyana Muhd Nordin[1], Suhana Mohd Said[1], Rahizar Ramli[1], Mohd Faizul Mohd Sabri[1], Nurulakmal Mohd Sharif[1], Nik Ahmad Fadzil Nik Mohd Arifin[2], Nik Nurul Syazana Ibrahim[2]*
*[1] University of Malaya, Malaysia; [2] MIMOS, Malaysia*

Tue-Expo-17:30-P38
**Protective Coatings of Electronics under Harsh Thermal Shock**
*Juha Pippola, Tuomas Marttila, Laura Frisk*
*Tampere University of Technology, Finland*

Tue-Expo-17:30-P39
**Evaluating board level solder inter-connects reliability using vibration test methods**
*Yang Liu, Fenglian Sun, Hongwu Zhang, Zhen Zhou*
*Harbin University of Science & Techno-logy, China*

Tue-Expo-17:30-P40
**Reliability of adhesive joined thinned chips on flexible substrates under humid conditions**
*Laura Frisk[1], Kirsi Saarinen-Pulli[2]*
*[1] Tampere university of Technology, Finland; [2] Konecranes, Finland*

## Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics

Tue-Expo-17:30-P41
**Crystallographic-orientation-dependent GIDL currents in Tri-gate MOSFETs under hot carrier stress**
*Jong Tae Park, Jae Hoon Lee*
*Incheon National University, Korea*

Tue-Expo-17:30-P42
**Hot carrier and PBTI induced degra-dation in silicon nanowire gate-all-around SONOS MOSFETs**
*Jong Tae Park[1], Jin Hyung Choi[1], Jin-Woo Han[2], Chon Gun Yu[1]*
*[1] Incheon National University, Korea; [2] Nasa ames research center, United States*

Tue-Expo-17:30-P43
**Energy distribution of positive charges in high-k dielectric**
*Sharifah Fatmadiana Wan Muhamad Hatta[1], Ji Zhigang[2], Jian Zhang[2], Wei Zhang[2], Norhayati Soin[3], B Kaczer[4], S Gendt[4], G Groeseneken[4]*
*[1] University of Malaya, Malaysia; [2] Liver-pool John Moores University, United Kingdom; [3] University Malaya, Malaysia; [4] IMEC, Belgium*

Tue-Expo-17:30-P44
**Defects evolution involving interface dispersion approaches in high-k/ metal-gate deep-submicron CMOS**
*Yasmin Abdul Wahab, Norhayati Soin, Sharifah Fatmadiana Wan Muhammad Hatta*
*University of Malaya, Malaysia*

Tue-Expo-17:30-P45
**Total ionizing dose response of fluorine implanted silicon-on-insulator buried oxide**
*Kenneth Potter[1], Katrina Morgan[1], Chris Shaw[2], Peter Ashburn[1], William Redman-White[1], C.H. de Groot[1]*
*[1] University of Southampton, United Kingdom; [2] AWE Plc, United Kingdom*

Tue-Expo-17:30-P46
**Analysing Aging and Voltage Scaling Impacts under Neutron-induced Soft Error Rate in SRAM-based Field Programmable Gate Arrays**
*Fernanda Kastensmidt[1], Jorge Tonfat[1], Thiago Both[1], Gilson Wirth[1], Paolo Rech[1], Ricardo Reis[1], Pascal Benoit[2], Florent Bruguier Bruguier[2], Lionel Torres[2]*
*[1] UFRGS, Brazil; [2] LIRMM, France*

## Reliability & Failure Mechanisms of Wide Bandgap Devices

Tue-Expo-17:30-P47
**Stability Evaluation of Au-free Ohmic contacts on AlGaN/GaN HEMTs under a Constant Current Stress**
*Tian-Li Wu, Denis Marcon, Steve Stof-fels, Shuzhen You, Brice De Jaeger, Marleen Van Hove, Guido Grosesenken, Stefaan Decoutere*
*IMEC, Belgium*

Tue-Expo-17:30-P48
**Failure signatures on 0.25 µm GaN HEMTs for high-power RF applications**
*Antonio Stocco[1], Stefano Dalcanale[1], Fabiana Rampazzo[1], Matteo Meneghini[1], Gaudenzio Meneghesso[1], Jan Grünen-pütt[2], Benoit Lambert[3], Hervé Blanck[2], Enrico Zanoni[1]*
*[1] Department of Information Engineering, University of Padova, Italy; [2] United Mo-nolithic Semiconductors, Germany; [3] United Monolithic Semiconductors, France*

Tue-Expo-17:30-P49
**Crosstalk in monolithic GaN-on-Silicon power electronic devices**
*Vineet Unni[1], Hiroji Kawai[2], Sankara Narayanan[1]*
*[1] The University of Sheffield, United Kingdom; [2] POWDEC K.K, Japan*

Tue-Expo-17:30-P50
**Influence of different carbon doping on the performance and reliability of InAlN/GaN HEMTs**
*Isabella Rossetto[1], Fabiana Rampazzo[1], Matteo Meneghini[1], Christian Dua[2], Piero Gamarra[2], Raphael Aubry[2], Marie Antoinette Poisson[2], Sylvain L. Delage[2], Gaudenzio Meneghesso[1], Enrico Zanoni[3]*
*[1] University of Padova, Italy; [2] Thales III-V Labs, France; [3] DEI-UNIPD, Italy*

## Reliability & Failure Mechanisms of Photonic and Special Devices

Tue-Expo-17:30-P51
**The effect of gate overlap on the device degradation in IGZO thin film transistors**
*Jong Tae Park, Dae Hyun Kim*
*Incheon National University, Korea*

Tue-Expo-17:30-P52
**Dispersion study of DC and Low Frequency Noise in SiGe:C Hetero-junction Bipolar Transistors used for mm-Wave to Terahertz applications**
*Marcelino Seif[1], Fabien Pascal[1], Bruno Sagnes[1], Alain Hoffmann[1], Sebastien Haendler[2], Pascal Chevalier[2], Daniel Gloria[2]*
*[1] IES - Université Montpellier 2, France; [2] STMicroelectronics Crolles, France*

Tue-Expo-17:30-P53
**The degradation of multi-crystalline silicon solar cells after damp heat tests**
*Wonwook Oh[1], Seongtak Kim[1], Soohyun Bae[1], Nochang Park[2], Yoonmook Kang[1], Haeseok Lee[1], Donghwan Kim[1]*
*[1] Korea university, Korea; [2] KETI, Korea*

Tue-Expo-17:30-P54
**A fast reliability assessment method for Si MEMS based microcantilever beams**
*Peyman Rafiee, Golta Khatibi*
*University of Vienna, Austria*

## Focused Ion Beam and European FIB User Group

Tue-Expo-17:30-P55
**Low temperature FIB cross section: application to indium micro bumps**
*Lionel Dantas De Morais, Sophie Cheval-liez, Stephanie Mouleres*
*SOFRADIR, France*

Room: A

## Failure Analysis

*Chairs: Siegfried Görlich, Rudolf Schlangen*

Wed-A-08:30-**Tutorial**
**Asking The Right Questions (be)for(e) Failure Analysis**
*Peter Jacob, EMPA, Zürich, Switzerland*

Wed-A-10:40
**Signal noise perturbation on automotive mixed-mode semiconductor device generated by graded substrate defect**
*Yann Weber[1], Linda Buffo[1], Béatrice Vanhuffel[1], Nicholas Lee[1], Neal Stirlen[2], Jeff Chen[2], Xiang-Dong Wang[2]*
*[1]Freescale Semiconduteurs, France;*
*[2]Freescale Semiconduteurs, United States*

Wed-A-11:00
**Quantitative Scanning Microwave Microscopy: A calibration flow**
*Thomas Schweinboeck, Soeren Hommel*
*Infineon, Germany*

Wed-A-11:20
**Electro Optical Therahertz Pulse Reflectometry, a non destructive technique to localize defects on various type of package**
*Antoine Reverdy[1], Maxime Marchetti[2], Alessandra Fudoli[3], Vincent Goubier[2], Morgan Cason[3]*
*[1]Sector Technologies, France;*
*[2]ST Microelectronis, France;*
*[3]ST Microelectronis, Italy*

Wed-A-11:40
**Exact 3D Simulation of Scanning Electron Microscopy Images of Semiconductor Devices in the Presence of Electric and Magnetic Fields**
*Mauro Ciappa[1], Alexey Yu. Illarionov[2], Emre Ilguensatiroglu[1]*
*[1] ETH Zurich, Switzerland;*
*[2]Integrated Systems Laboratory, ETH, Switzerland*

Wed-A-12:00
**A comprehensive study of the application of the EOP techniques on bipolar devices**
*Mehdi Mohamed Rebai[1], Frédéric Darracq[2], Philippe Perdu[3], Jean-Paul Guillet[2]*
*[1]MS Laboratory & CNES, France; [2] IMS Laboratory, France; [3]CNES, France*

Room: B

## Power Devices Reliability Electrical & Thermal Analysis, Modelling

*Chairs: Mauro Ciappa, Reinhold Bayerer*

Wed-B-08:30-**Tutorial**
**Drift and reliability mechanisms in GaN based power devices for high voltage switching applications: The current understanding**
*Joachim Würfl, FBH, Berlin, Germany*

Wed-B-10:40
**Impact of gate drive voltage on avalanche robustness of trench IGBTs**
*Michele Riccio[1], Luca Maresca[1], Andrea Irace[1], Giovanni Breglio[1], Yohei Iwahashi[2]*
*[1]Università di Napoli Federico II, Italy;*
*[2]Toyota Motor Corporation, Japan*

Wed-B-11:00
**Thermal-aware design and fault analysis of a DC/DC parallel resonant converter**
*Giuseppe De Falco, Michele Riccio, Giovanni Breglio, Andrea Irace*
*DIETI - Università di Napoli Federico II, Italy*

Wed-B-11:20
**Comparison of Temperature Limits for Trench Silicon IGBT Technologies for Medium Power Applications**
*Xavier Perpiñà[1], Xavier Jordà[1], Javier León[2], Miquel Vellvehi[2], Daniel Antón[3], Sergio Llorente[3]*
*[1]IMB-CNM, Spain; [2] CNM, Spain;*
*[3]BSH, Spain*

Wed-B-11:40
**3-D electrothermal simulation of active cycling on smart power MOSFETs during Short-Circuit and UIS conditions**
*Michele Riccio[1], Vincenzo D'alessandro[1], Andrea Irace[1], Gilles Rostaing[2], Mounira Berkani[2], Stéphane Lefebvre[2], Philippe Dupuy[3]*
*[1]University Federico II, Italy; [2] SATIE, CNAM, CNRS, ENS Cachan, France;*
*[3] FREESCALE, France*

Wed-B-12:00
**Performance drifts of N-MOSFETs under pulsed RF life test**
*Mohamed Gares*
*ISIM, University of Gabes, Tunisia*

Room: C

## Chip-Package Interactions and 3D Reliability & Failure Mechanisms

*Chairs: Ingrid De Wolf*

Wed-C-08:30-**Tutorial**
**Managing the Effects of Mechanical Stress on the Reliability of 3D IC Stacks**
*Ehrenfried Zschech[1], Valeriy Sukharev[2], Riko Radojcic[3]; [1] FhG IZFP, Dresden, GER; [2] Mentor Graphics, Fremont CA, USA; [3] San Diego CA, USA*

Wed-C-10:40
**Reliability Challenges for Barrier/Liner System in High Aspect Ratio Through Silicon Vias**
*Yunlong Li, Stefaan Van Huylenbroeck, Els Van Besien, Xiaoping Shi, Chen Wu, Michele Stucchi, Gerald Beyer, Eric Beyne, Ingrid De Wolf, Kristof Croes*
*IMEC, Belgium*

Wed-C-11:00
**Submicron XCT for failure analysis in advanced packaging**
*Markus Löffler[1], S. Niese[1], J. Wolf[2], Ehrenfried Zschech[3]*
*[1]TU Dresden, Germany; [2] Fraunhofer IZM-ASSID, Germany; [3]TU Dresden and Fraunhofer IKTS-MD, Germany*

Wed-C-11:20
**The effects of etching and deposition on the performance and stress evolution of open through silicon vias**
*Lado Filipovic, Siegfried Selberherr*
*Technische Universität Wien, Austria*

Wed-C-11:40
**Advanced methods for mechanical and structural characterization of nanoscale materials for 3D IC integration**
*Christoph Sander, André Clausner, Martin Gall*
*Fraunhofer IKTS-MD, Germany*

Wed-C-12:00
**Stress Analyses of High Spatial Resolution on TSV and BEoL Structures**
*Dietmar Vogel[1], Ellen Auerswald[1], Juergen Auersperg[1], Parisa Bayat[2], Raul Rodriguez[2], Dietrich Zahn[2], Sven Rzepka[1], Bernd Michel[1]*
*[1]Fraunhofer ENAS, Germany;*
*[2]Technical University Chemnitz, Germany*

10:10 - 10:40 Coffee Break • Exhibition Area

12:20 -13:30 Lunch Break • Exhibition Area

Room: A

## Failure Analysis

*Chairs: Siegfried Görlich, Rudolf Schlangen*

Wed-A-13:30-**Invited**
**Enabling Higher Fault Isolation Resolution through Advanced Optics**
*Derryck T. Reid*
*Heriot-Watt University, United Kingdom*

Wed-A-14:00
**Magnetic Field Imaging for non destructive 3D IC testing**
*Jan Gaudestad, Antonio Orozco*
*Neocera, United States*

Wed-A-14:20
**Pattern image enhancement by extended depth of field**
*Samuel Chef[1], Bastien Billiot[2], Sabir Jacquir[2], Kevin Sanchez[3], Philippe Perdu[3], Stéphane Binczak[2]*
*[1]University of Burgundy & CNES, France; [2]University of Burgundy, France; [3]CNES, France*

Wed-A-14:40
**Backside spectroscopic photon emission microscopy using intensified silicon CCD**
*Arkadiusz Glowacki[1], Christian Boit[1], Philippe Perdu[2], Yoshitaka Iwaki[3]*
*[1]Technische Universität Berlin, Germany; [2]CNES, France; [3]Hamamatsu Photonics, Germany*

Wed-A-15:00
**Fretting corrosion: analysis of the failure mechanism for low voltage drives applications**
*Elena Mengotti[1], Liliana Duarte[1], Juha Pippola[2], Laura Frisk[2]*
*[1]ABB, Switzerland; [2]Tampere University of Technology, Finland*

Room: B

## Power Devices Reliability Power Device Assembly

*Chairs: Mauro Ciappa, Reinhold Bayerer*

Wed-B-13:30-**Invited**
**Lifetime Modeling and Simulation of Power Modules for Hybrid Electrical/ Electrical Vehicles**
*Markus Thoben*
*Infineon, Germany*

Wed-B-14:00
**Study of Thermal Cycling and Temperature Aging on PbSnAg Die Attach Solder Joints for High Power Modules**
*Franc Dugal[1], Mauro Ciappa[2]*
*[1]ABB, Switzerland;*
*[2]ETH Zurich, Switzerland*

Wed-B-14:20
**Improving the FE Simulation of Molded Packages Using Warpage Measurements**
*Saskia Huber[1], Marius van Dijk[2]*
*[1]Fraunhofer, Germany;*
*[2]Fraunhofer IZM, Germany*

Wed-B-14:40
**Reliability of Cu nanoparticle joint for high temperature power electronics**
*Toshitaka Ishizaki[1], Yasushi Yamada[2], Toshikazu Satoh[1]*
*[1]Toyota Central R&D Labs., Inc., Japan;*
*[2] Daido Univeristy, Japan*

Wed-B-15:00
**Dielectric Strength and Thermal Performance of PCB-Embedded Power Electronics**
*Wolfgang Wondrack[1], Richard Randoll[1], Andreas Schletz[2]*
*[1]Daimler, Germany;*
*[2]Fraunhofer IISB, Germany*

Room: C

## Reliability & Failure Mechanisms in Packages and Assembly

*Chairs: Kirsten Weide-Zaage, Heléné Frémont*

Wed-C-13:30-**Invited**
**Reliability of Wafer Level Chip Scale Packages**
*René Rongen*
*NXP Semiconductors, Nijmegen, Netherlands*

Wed-C-14:00
**High temperature degradation of palladium coated copper bond wires**
*Jörg Krinke, Dragica Dragicevic, Susann Leinert, Erik Frieß, Joachim Glück*
*Robert Bosch GmbH, Germany*

Wed-C-14:20
**Interface microstructure effects in Au thermosonic ball bonding contacts by high reliability wire materials**
*Benjamin März[1], Andreas Graff[1], Robert Klengel[1], Matthias Petzold[2]*
*[1]Fraunhofer Institute for Mechanics of Materials Halle, Germany; [2]Fraunhofer IWM Halle, Germany*

Wed-C-14:40
**Reliability of thick Al wire: A study of the effects of wire bonding parameters on thermal cycling degradation rate using non-destructive methodologies**
*Elaheh Arjmand, Pearl Agyakwa, C. Mark Johnson*
*University of Nottingham, United Kingdom*

Wed-C-15:00
**Qualification procedure against moisture for embedded capacitors**
*Helene Fremont[1], Jörg Kludt[2], Massar Wade[1], Kirsten Weide-Zaage[2], Isabelle Bord-Majek[1], Geneviève Duchamp[1]*
*[1]IMS-Bordeaux Université de Bordeaux, France; [2]LFI Gottfried Wilhelm Leibniz Universität Hannover, Germany*

**15:20 - 15:50 Coffee Break • Exhibition Area**

Room: A

## Failure Analysis

*Chairs: Siegfried Görlich, Rudolf Schlangen*

Wed-A-15:50-17:30-**Workshop**

Failure Analysis Workshop
see details on page 11

Room: B

## Power Devices Reliability

*Chairs: Eckhard Wolfgang, Mauro Ciappa*

Wed-B-15:50-17:30-**Workshop**

Power Devices Workshop
see details on page 11

Room: C

## Reliability & Failure Mechanisms in Packages and Assembly

*Chairs: Kirsten Weide-Zaage, Heléné Frémont*

Wed-C-15:50
**High Temperature Reliability of Electrically Conductive Adhesive Attached Temperature Sensors on Flexible Polyimide Substrates**
*Sanna Lahokallio, Janne Kiilunen, Laura Frisk*
*Tampere University of Technology, Finland*

Wed-C-16:10
**A Study on Electrochemical effects in external Capacitor Packages**
*Harald Preu, Jochen Feilmeier, Markus Lang, Norbert Soellner, Jürgen Walter, Walter Mack*
*Infineon Technologies AG, Germany*

**18:30 Bus Transfer with Guided City Tour - Pickup in front of TUB Main Entrance (Straße des 17. Juni 135)**

**19:30 Social Event - Palais at the Kulturbrauerei (Bus Transfer is provided back to TU Berlin)**

Room: A

## Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics

*Chairs: Marise Bafleur, Oliver Aubel*

Thu-A-08:30-**Invited**
**Performance and Reliability Trade-Offs for High-K RRAM**
*Nagarajan Raghavan*
*Singapore University of Technology and Design, Singapore*

Thu-A-09:10
**Optimization of inter-gate-dielectrics in hybrid float gate devices to reduce window instability during memory operations**
*Baojun Tang[1], Weidong Zhang[2], Laurent Breuil[1], Colin Robinson[2], Yunqi Wang[3], Maria Toledano-Luque[1], Geert Van den Bosch[1], Jianfu Zhang[2], Jan Van Houdt[1]*
*[1] IMEC, Belgium; [2] Liverpool John Moores University, United Kingdom; [3] University of Oxford, United Kingdom*

Thu-A-09:30
**Impact of endurance degradation on the programming efficiency and the energy consumption of NOR Flash memories**
*Vincenzo Della Marca, Jeremy Postel-Pellerin, Guillaume Just, Pierre Canet, Jean-Luc Ogier*
*Aix-Marseille University, France*

Thu-A-09:50
**Variability Model for Forming Process in Oxygen Vacancy Modulated High-κ based Resistive Switching Memory Devices**
*Nagarajan Raghavan[1], Michel Bosman[2], Daniel Frey[3], Kin Leong Pey[1]*
*[1] Singapore University of Technology and Design, Singapore; [2] A*STAR Institute of Materials Research and Engineering, Singapore; [3] Massachusetts Institute of Technology, United States*

Room B:

## Reliability & Failure Mechanisms of Wide Bandgap Devices

*Chairs: Hans-Joachim Würfl, Michael Uren*

Thu-B-08:30
**Single Pulse Avalanche Robustness and Repetitive Stress Ageing of SiC power MOSFETs**
*Asad Fayyaz[1], Li Yang[1], Michele Riccio[2], Alberto Castellazzi[1], Andrea Irace[2]*
*[1] University of Nottingham, United Kingdom; [2] University of Naples Federico II, Italy*

Thu-B-08:50
**Effect of gate trench fabrication technology on reliability of AlGaN/GaN heterojunction field effect transistors**
*Sergey Shevchenko, Matthias Schulz, Eldad Bahat-Treidel, Wilfred John, Stephan Freyer, Paul Kurpas, Hans-Joachim Würfl*
*Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Germany*

Thu-B-09:10
**Physical Origin of Current Collapse in Au-free AlGaN/GaN Schottky Barrier Diode**
*Jie Hu, Steve Stoffels, Silvia Lenci, Nicolò Ronchi, Rafael Venegas, Shuzhen You, Benoit Bakeroot, Guido Groeseneken, Stefaan Decoutere*
*IMEC, Belgium*

Thu-B-09:30
**Thermal damage in SiC Schottky diodes induced by SE heavy ions**
*Carmine Abbate[1], Giovanni Busatto[1], Paolo Cova[2], Nicola Delmonte[2], Francesco Giuliani[2], Francesco Iannuzzo[1], Annunziata Sanseverino[1], Francesco Velardi[1]*
*[1] DIEI - University of Cassino and Southern Lazio, Italy; [2] DII - University of Parma, Italy*

Thu-B-09:50
**Temperature effects on the ruggedness of SiC Schottky Diodes under surge current**
*Javier León[1], Xavier Perpiñà[1], Viorel Banu[1], Josep Montserrat[1], Maxime Berthou[2], Miquel Vellvehi[1], Philippe Godignon[1], Xavier Jordà[1]*
*[1] IMB-CNM (CSIC), Spain; [2] Insa-Lyon, France*

Room: C

## Reliability & Failure Mechanisms of Photonic and Special Devices

*Chairs: Frank Altmann, Massimo Vanzi*

Thu-C-08:30-**Invited**
**MEMS Reliability – Current Status and Challenges**
*Mervi Paulasto-Kröckel, Jue Li*
*University Aalto, Finland*

Thu-C-09:00
**ESD on GaN-based LEDs: an analysis based on dynamic electroluminescence measurements and current waveforms**
*Matteo Dal Lago[1], Matteo Meneghini[1], Nicola Trivellin[2], Gaudenzio Meneghesso[1], Enrico Zanoni[1], Marco Barbato[1], Carlo De Santi[1]*
*[1] University of Padova, Italy; [2] LightCube SRL, Italy*

Thu-C-09:20
**Temperature dependent optoelectronic properties of a non-intentionally created cleaved-coupled-cavity laser**
*Heinz-Christoph Neitzert[1], Giovanni Landi[2]*
*[1] Salerno University, Italy; [2] Fernuniversitaet Hagen, Germany*

Thu-C-09:40
**Thermally-activated degradation of InGaN-based laser diodes: effect on threshold current and forward voltage**
*Carlo De Santi[1], Matteo Meneghini[2], Michael Marioli[2], Matteo Buffolo[2], Nicola Trivellin[3], T. Weig[4], K. Holc[4], K. Kohler[4], J. Wagner[4], U. T. Schwarz[4], Gaudenzio Meneghesso[2], Enrico Zanoni[2]*
*[1] Università degli Studi di Padova - Department of Information Engineering, Italy; [2] University of Padova, Italy; [3] LightCube SRL, Italy; [4] Fraunhofer Institute for Applied Solid State Physics IAF, Germany*

Thu-C-10:00
**FIB-induced electro-optical alterations in a DFB InP laser diode**
*Giovanna Mura, Massimo Vanzi, Giulia Marcello*
*DIEE University of Cagliari - Italy, Italy*

**10:20 - 10:50 Coffee Break • Exhibition Area**

Room: A

## Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics ESD/SER

*Chairs: Marise Bafleur, Oliver Aubel*

Thu-A-10:50
**Novel 3D back-to-back diodes ESD protection**
*Bertrand Courivaud[1], Nicolas Nolhier[1], Gilles Ferru[2], Marise Bafleur[1], Fabrice Caignet[1]*
*[1] LAAS-CNRS, France; [2] IPDIA, France*

Thu-A-11:10
**Particle Monte Carlo Modeling of Single-Event Transient Current and Charge Collection in Integrated Circuits**
*Jean-Luc Autran[1], Maximilien Glorieux[2], Daniela Munteanu[3], Sylvain Clerc[2], Gilles Gasiot[2], Philippe Roche[2]*
*[1] Aix-Marseille University, France; [2] STMicroelectronics, France; [3] CNRS, France*

Thu-A-11:30
**Radiation Sensitivity of Junctionless Double-Gate 6T SRAM Cells Investigated by 3-D Numerical Simulation**
*Daniela Munteanu[1], Jean-Luc Autran[2]*
*[1] CNRS-IM2NP, France; [2] Aix-Marseille University, France*

Thu-A-11:50
**Improving the ability of Bulk Built-In Current Sensors to detect Single Event Effects by using triple-well CMOS**
*Jean-Max Dutertre[1], Rodrigo Possamai Bastos[2], Olivier Potin[3], Marie-Lise Flottes[3], Bruno Rouzeyre[3], Giorgio Di Natale[3], Alexandre Sarafianos[4]*
*[1] Ecole des Mines de Saint-Etienne, France; [2] TIMA Lab , France; [3] LIRMM. Univ. Montpellier, France; [4] STMicroelectronics, France*

Thu-A-12:10
**Assessment of Read Disturb Immunity in Conducting Bridge Memory Devices – A Thermodynamic Perspective**
*Nagarajan Raghavan[1], Michel Bosman[2], Kin Leong Pey[1]*
*[1] Singapore University of Technology and Design, Singapore; [2] A*STAR Institute of Materials Research and Engineering, Singapore*

Room: B

## Reliability & Failure Mechanisms of Wide Bandgap Devices

*Chairs: Hans-Joachim Würfl, Michael Uren*

Thu-B-10:50
**Proton induced trapping effect on space compatible GaN HEMTs**
*Antonio Stocco[1], Simone Gerardin[1], Davide Bisi[1], Stefano Dalcanale[1], Fabiana Rampazzo[1], Matteo Meneghini[1], Gaudenzio Meneghesso[1], Jan Grünenpütt[2], Benoit Lambert[3], Hervé Blanck[2], Enrico Zanoni[4]*
*[1] University of Padova, Italy; [2] United Monolithic Semiconductors, Germany; [3] United Monolithic Semiconductors, France; [4] DEI-UNIPD, Italy*

Thu-B-11:10
**Analysis of an ESD failure mechanism on a SiC MESFET**
*Tanguy Phulpin[1], Karine Isoird[1], David Tremouilles[1], Dominique Tournier[2], Philippe Godignon[3]*
*[1] LAAS-CNRS, France; [2] ampere-lab, France; [3] CNM, Spain*

Thu-B-11:30
**Traps localization and analysis in GaN HEMTs**
*Alessandro Chini[1], Fabio Soci[1], Gaudenzio Meneghesso[2], Matteo Meneghini[2], Enrico Zanoni[2]*
*[1] University of Modena and Reggio Emilia, Italy; [2] University of Padova, Italy*

Thu-B-11:50
**Degradation analysis and current collapse imaging in AlGaN/GaN HEMT by electric field induced optical second harmonic generation measurement**
*Takashi Katsuno[1], Takaaki Manaka[2], Tsuyosihi Ishikawa[1], Hiroyuki Ueda[1], Tsutomu Uesugi[1], Mitsumasa Iwamoto[2]*
*[1] Toyota Central R&D Labs., Inc., Japan; [2] Tokyo Institute of Technology, Japan*

Room: C

## Reliability & Failure Mechanisms of Photonic and Special Devices

*Chairs: Frank Altmann, Massimo Vanzi*

Thu-C-10:50
**UV LEDs reliability tests for fluoro-sensing sensor application**
*F. Jose Arques-Orobon[1], Neftali Nuñez[2], Manuel Vazquez[2], Vicente González-Posadas[1]*
*[1] Technical University of Madrid, Spain; [2] Instituto de Energía Solar-Technical University of Madrid, Spain*

Thu-C-11:10
**A study of deposition conditions on charging properties of PECVD silicon nitride films for MEMS capacitive switches**
*Matroni Koutsoureli, Loukas Michalas, Anestis Gantis, George Papaioannou*
*University of Athens, Greece*

Thu-C-11:30
**Automated defect analysis in solar cells using EBIC**
*Grigore Moldovan[1], Shark Lotharukpong[2], Peter Wilshaw[2]*
*[1] Oxford Instruments NanoAnalysis, United Kingdom;*
*[2] University of Oxford, United Kingdom*

Thu-C-11:50
**Conduction Instability of Amorphous InGaZnO Thin-Film Transistors under Constant Drain Current Stress**
*Jung Han Kang, Edward Namkyu Cho, Ilgu Yun*
*Yonsei University, Korea*

12:30 - 13:30 Lunch Break • Exhibition Area

## Room: A

**Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics FEOL**

*Chairs: Marise Bafleur, Oliver Aubel*

Thu-A-13:30
**Comparative Soft Error Evaluation of Logic Cells in FinFET Technology**
*Laurent Artola[1], Guillaume Hubert[1], Massimo Alioto[2]*
*[1]ONERA - The French Aerospace Lab, France; [2]National University of Singapore, Singapore*

Thu-A-13:50
**A Quantitative Study of Phosphorus Implantation Damage on the thick Gate Oxide of the 28nm Node**
*Xinggong Wan[1], Sandhya Chandrashekhar[1], Boris Bayha[2], Martin Trentzsch[2], Torben Balzer[2], Mahesh Siddabathula[2], Oliver Aubel[2]*
*[1]GLOBALFOUNDRIES, United States; [2]GLOBALFOUNDRIES, Germany*

Thu-A-14:10
**Mixture of Negative Bias Temperature Instability and Hot-Carrier driven Threshold Voltage Degradation of 130nm technology p-channel Transistors**
*Gunnar Andreas Rott[1], Karina Rott[1], Hans Reisinger[1], Wolfgang Gustin[1], Tibor Grasser[2]*
*[1]Infineon Technologies AG, Germany; [2]Institute for Microelectronics, Technische Universität Wien, Austria*

Thu-A-14:30
**Predictive evaluation of electrical characteristics of sub-22nm FinFET technologies under device geometry variations**
*Cristina Meinhardt, Alexandra Lackmann Zimpeck, Ricardo Reis*
*UFRGS, Brazil*

## Room: B

**Power Devices Reliability Devices & Processes**

*Chairs: Mauro Ciappa, Reinhold Bayerer*

Thu-B-13:30
**The Influence of Liners with Ti, Ta or Ru Finish on Thin Cu Films**
*David Gross[1], Sabine Haag[1], Martin Schneider-Ramelow[2], Klaus-Dieter Lang[2]*
*[1]Robert Bosch GmbH, Germany; [2]Fraunhofer IZM, Germany*

Thu-B-13:50
**HCS Degradation of 5nm Oxide High-Voltage PLDMOS**
*Christina Olk, Stefano Aresu, Ralf Rudolf, Michael Röhner, Wolfgang Gustin*
*Infineon, Germany*

Thu-B-14:10
**Risk and reliability assessment about a manufacturing issue in a power MOSFET for automotive applications**
*Corinne Bergès, Pierre Soufflet, Abdeslam Jadrani*
*Freescale, France*

Thu-B-14:30
**Structure oriented compact model for advanced trench IGBTs without fitting parameters for extreme condition: part II**
*Junpei Takaishi[1], Syohei Harada[1], Masanori Tsukuda[2], Ichiro Omura[1]*
*[1]Kyushu Institute of Technology, Japan; [2] ICSEAD, Japan*

Thu-B-14:50
**Short-circuit protection for an IGBT with detecting the gate voltage and gate charge**
*Kazunori Hasegawa[1], Hidetaro Yoshida[1], Kota Hamada[1], Masanori Tsukuda[2], Ichiro Omura[1], Kenichi Yamamoto[1]*
*[1]Kyushu Institute of Technology, Japan; [2] The International Centre for the Study of East Asian Development, Japan*

## Room: C

**Chip-Package Interactions and 3D Reliability & Packages and Assembly & Failure Mechanisms**

*Chairs: Ingrid De Wolf, Kirsten Weide-Zaage, Heléné Frémont*

Thu-C-13:30-14:10-**Workshop**

CPI + 3D + Packaging + Harsh Environment Workshop
see details on page 11

**15:10 - 15:30 Coffee Break • Exhibition Area**

**15:30 - 16:00 Closing Ceremony • Room: A**
**Best Paper Award - Marise Bafleur • Best Poster Award - Olaf Wittler**
**Announcement ESREF 2015 - Marise Bafleur, Philippe Perdu**

# Abstracts - Oral Presentations

Tue-A-08:30-**Keynote**
**Organic photovoltaic stability: Designed to last**
*Jan Gilot, Ronn Andriessen*
*Solliance/Holst Centre, Netherlands*

Since the discovery of Organic PhotoVoltaics (OPV) in the early 1990's, a lot of effort was put on further increasing the efficiency and to up-scale the devices to cells and modules. Today, power conversion efficiencies of 10 - 12% have been reported by using different processing approaches as well as different device architectures. Also up-scaling has been demonstrated on R2R coating and printing processes as well as R2R vacuum deposition. However, device, cell and module stability research only started around 2005 to become a serious point of attention for the OPV community. Initiatives like ISOS and round robins tests of OPV devices clearly showed the importance of standardizing test protocols in order to allow for better interlaboratory comparisons. This actually accelerated the progress in the field of understanding device failures as well as of identifying lifetime enhancing strategies for technical and chemical measures.
This presentation will explain, starting from a baseline OPV architecture, how layer-by-layer improvements can enhance both device performance and stability. We present how fundamental understanding of dominating failure mechanisms can guide material and architecture selection. Our insights into the degradation mechanisms stem from combinatorial device testing, systematic variation of ageing conditions as well as detailed analytical investigations. Combination of reliability-driven device design and a proper barrier and encapsulation technology are the foundations of an OPV designed to last.

Tue-A-09:10-**Keynote**
**OLEDs quality and reliability**
*Volker van Elsbergen*
*Philips Research, Aachen, Germany*

Organic light-emitting diodes (OLEDs) are a new and attractive class of solid-state light sources and they are emerging as a compelling candidate to replace conventional lighting systems. OLEDs provide potential for power-efficient large area light sources which will substantially contribute to energy efficient lighting. In addition, they combine revolutionary properties. They are thin and flat, and can be transparent, color-tunable, and flexible, enabling light sources with an unprecedented grade of flexibility in terms of design and application.
This talk will give an introduction to the OLED technology, present today's status of OLED lighting products, and will outline the future of OLED lighting. Special attention will be given to quality aspects, failure mechanisms, and reliability. Topics that will be covered comprise:
- operational lifetime
- uniformity of light emission
- shelf life and encapsulation
- reliability and short circuit behavior
- thermal stability
- instability of charge carrier injection and transport

## Quality and Reliability Assessment – Techniques and Methods for Devices and Systems

Tue-A-10:20-**Invited**
**Robustness Validation - A Physics of Failure Based Approach to Qualification**
*Werner Kanert*
*Infineon, Germany*

Product reliability is crucial to the success of a company. Product qualification today is based on standards that follow a stress-test driven approach, meaning pre-defined stress tests with pre-defined stress conditions. However, reliability requirements have increased, while at the same time both designs of semiconductor components and usage of these components in the applications have increasingly been pushed to the limits. This development raises the question, how far the standard procedures are still suitable for reliability assessment. Robustness Validation is an approach to a failure-mechanism-driven qualification that was primarily initiated by the automotive industry but has a much wider range of applicability. The paper will give an introduction to the basic ideas of Robustness Validation. Some limitations including statistical aspects will also be discussed.

Tue-A-10:50
**A design tool to study the impact of mission-profile on the reliability of SiC-based PV-inverter devices**
*Nicolae Cristian Sintamarean[1], Huai Wang[1], Frede Blaabjerg[1], Peter De Place Rimmen[2]*
*[1]Aalborg University, Denmark;*
*[2]Danfoss Power Electronics A/S, Denmark*

This paper introduces a reliability-oriented design tool for a new generation of grid connected PV-inverters. The proposed design tool consists of a real field mission profile model (for one year operation in USA-Arizona), a PV-panel model, a grid connected PV-inverter model, an Electro-Thermal model and the lifetime model of the power semiconductor devices. A simulation model able to consider one year real field operation conditions (solar irradiance and ambient temperature) is developed. Thus, one year estimation of the converter devices thermal loading distribution is achieved and is further used as an input to a lifetime model. The proposed reliability oriented design tool is used to study the impact of MP and device degradation (aging) in the PV-inverter lifetime. The obtained results indicate that the MP of the field where the PV-inverter is operating has an important impact in the converter lifetime expectation, and it should be considered in the design stage to better optimize the converter design margin. In order to have correct lifetime estimation it is crucial to consider also the device degradation feedback (in the simulation model) which has an impact of 30 % in the precision of the lifetime estimation in the studied case.

Tue-A-11:10
**Copper wire interconnect reliability evaluation using in-situ HTSL tests**
*Amar Mavinkurve, Leon Goumans, Orla O'Halloran, Rene Rongen, Mark-Luke Farrugia*
*NXP Semiconductors, Netherlands*

Extensive work has been done in recent times to understand various failure mechanisms involving the Cu wire interconnect on conventional Al-based bondpads. One of the authors of this work have recently demonstrated the use of a novel Failure Analysis technique to quantify ex-situ Cu-Al ballbond degradation due to inter-metal corrosion. Three different failure mechanisms involving such interconnects have been described in a separate paper. This paper describes the use of in-situ High Temperature Storage Life (HTSL) tests based on a four point resistance method to evaluate Cu wire interconnect reliability. Although the same set up was used in the past to monitor Au-Al ballbond degradation, a different approach needed to be used for this system. Using conventional statistical methods of failure probability distributions and the need to rely on a set failure criterion was not found to be useful in this case. Furthermore, tests usually took very long periods until a sufficient percentage of the population had failed based on the set criterion. A simple physical model was used to quantify ballbond degradation due to the predominant failure mechanism. The method enabled extraction of activation energies for a number of molding compounds and is extremely useful for a faster screening of mold compounds that are suitable for Cu wire.

Tue-A-11:30
**Robust Electromigration Reliability Through Engineering Optimization**
*Wee Loon Ng[1], Kheng Chok Tee[1], Junfeng Liu[1], Yong Chiang Ee[1], Oliver Aubel[2], Chuan Seng Tan[3], Kin Leong Pey[4]*
*[1] GLOBALFOUNDRIES, Singapore; [2] GLOBALFOUNDRIES, Germany; [3] Nanyang Technological University, Singapore; [4] Singapore University of Technology and Design, Singapore*

With complex process integration approach and severe fabrication limitations caused by introduction of new materials and diminishing process margins, there are mounting concerns with the increased failure rate at the early life cycle (e.g. <1 year operation) of product application known as infant mortality failures. A paradigm change in reliability qualification methodology aims to understanding the impact of variation on reliability is required to ensure reliability robustness. Using Electromigration (EM) as an example, this paper described a methodology where the impact of process variation on reliability is studied. A model that predicts the impact of process variation on EM sigma is also proposed which enables variation and its impact on reliability to be quantified. Using this methodology, the critical process parameters impacting reliability could be identified and controlled to ensure reliability robustness.

Tue-A-11:50
**Empirical BEOL-TDDB evaluation based on I(t)-trace analysis**
*Oliver Aubel[1], Armand Beyer[1], Georg Talut[1], Martin Gall[2]*
*[1] GLOBALFOUNDRIES, Germany;*
*[2] Fraunhofer IKTS, Germany*

In this paper we are proposing a comprehensive approach of analyzing I(t)-traces generated during BEOL-TDDB investigations. The relations of the initial leakage, the shape of the I(t)-trace and the voltage dependence of the components are discussed. Clear voltage and area dependence could be found. The TDDB lifetime itself and also the transition point of the two I(t)-trace components is describing the TDDB voltage acceleration very well. Additionally the review of the breakdown charge gives evidence that only one component is responsible for the TDDB breakdown behavior.This empirical evaluation delivers a different view on the I(t)-trace shapes leading to better understanding of its contributions to the TDDB behavior.

Tue-A-13:10
**As-grown donor-like traps in low-k dielectrics and their impact on intrinsic TDDB reliability**
*Baojun Tang[1], Kristof Croes[1], Yohan Barbarin[1], Yunqi Wang[2], Robin Degraeve[1], Yunlong Li[1], Maria Toledano-Luque[1], Thomas Kauerauf[1], Juergen Bommels[1], Zsolt Tokei[1], Ingrid De Wolf[1]*
*[1] IMEC, Belgium;*
*[2] University of Oxford, United Kingdom*

Low-k dielectrics are essential for downscaling of the interconnects for the 20-10nm technologies. A planar capacitor test vehicle was used to investigate the intrinsic time dependent dielectric breakdown (TDDB) reliability of low-k dielectrics and the origin of an observed C-V hysteresis was studied. We hypothesize that the hysteresis is caused by donor-like traps present in the bulk of the low-k and not by electron/hole trapping or mobile charges. It is proposed that porogen/carbon residues are the source of these donor-like traps. Using Ileak vs. time measurements, it was found that the donor-like traps accelerate dielectric degradation due to an enhanced EOX, causing a localized partial breakdown. The intrinsic TDDB reliability of the low-k film was improved by adding a sealing layer as it blocked the donor-like traps discharging.

Tue-A-13:30
**Physics-of-Failure Assessment Methodology for Power Electronic Systems**
*David Squiller[1], Hannes Greve[1], Patrick McCluskey[1], Elena Mengotti[2]*
*[1] The University of Maryland, College Park, United States;*
*[2] ABB Switzerland Ltd., Corporate Research, Switzerland*

Driven by consumer markets and industrial needs, power electronic systems are operating at higher power densities, in smaller packages and in more exotic environments. As these trends continue, ensuring long-term operation in harsher conditions requires accurate reliability prediction models, most viably obtained through Physics-of-Failure (PoF) methodologies. This paper introduces a PoF-based system-level reliability assessment procedure in which the dominant failure mechanisms are identified for each primary subsystem. Procedures are also included describing how these assessment methodologies can be included in the product design phase to enhance overall system reliability.

Tue-A-13:50
**Influence of dicing damages on the thermo-mechanical reliability of bare-chip assemblies**
*Matthias Steiert, Jürgen Wilde*
*University of Freiburg, Germany*

A comprehensive portfolio of methods to avoid chip fracture is shown here. The influences of different dicing techniques to the breaking strength of silicon chips were studied. Due to investigations on the size effect of diced chips it was possible to develop an analytical model which describes the risk of chip fracture

for bare-chip assemblies. The possibility to predict fracture probabilities permits to design packages towards a minimal risk of chip fracture. New processes to remove dicing defects were evaluated. They can contribute to avoid chip fracture totally.

Tue-A-14:10
**Study of EM void nucleation and mechanic relaxation effects**
*Giulio Marti[1], Lucile Arnaud[1], Yves Wouters[2]*
*[1] STMicroelectronics, France; [2] SIMAP, France*

In this paper the void formation during electromigration is characterized with the single standard via (SSV) and the innovative local sense structure (LSS). LSS allows the measurement of small resistance change before the final void formation. This has allowed to define a time nucleation for the void. The SSV has been used to study: side effect in the first phase (i.e. the “plateau”), the time to failure (TTF) and the void growth. The comprehension of all these phenomena will be fundamental for the future of interconnects reliability physics and lifetime prediction.

Tue-A-14:30
**Assessment methodology of the lateral migration component in data retention of 3D SONOS memories**
*Lifang Liu*
*IMEC, Belgium*

A new procedure to assess the impact of lateral charge migration from the overall retention transient is developed. This experimental procedure is designed to be applied on any 3D NAND string, and does not require devices specifically designed; this allows to assess the impact of lateral migration in realistic conditions. The experimental procedure relies on comparing retention loss of a standard sample with a “control sample” not suffering from lateral migration, thanks to a pre-conditioning operation. The preconditioning procedure to obtain the control samples is discussed in detail and demonstrated through measurements and simulations.

Tue-A-15:20
**Power Grid Redundant Path Contribution in System on Chip (SoC) Robustness against Electromigration**
*Boukary Ouattara[1], Lise Doyen[1], David Ney[1], Habib Mehrez[2], Pirouz Bazargan-Sabet[2]*
*[1] STMicroelectronics, France; [2] Laboratory of Computer Sciences, France*

The miniaturisation of integrated circuits leads to reliability issues such as electromigration (EMG). This well known phenomenon is checked at design level by CAD tools. The conventional EMG check methods are based on electrical parameters. However, the wire physical degradation depends also on the interconnection network structure. In order to improve the EMG check methodologies, we propose an accurate method based on failure mechanism and chip power grid configuration. Indeed, the power grid offers redundant paths in case of void in main power supply path. The principle of our method is to take into account the contribution of these redundant paths in power grid lifetime assessment. These effects are validated by silicon ageing tests on structures designed in 28nm FDSOI (Full Depleted Silicon On Insulator). These accelerated tests results have confirmed the lifetime gain due to redundancy. These results provide perspectives for the relaxation of wire current limits and improve the chip design toward EMG

Tue-A-15:40
**Single-parameter model for the post-breakdown conduction characteristics of HoTiOx-based MIM capacitors**
*Enrique Miranda*
*Universitat Autonoma de Barcelona, Spain*

The post-breakdown I-V characteristics of HoTiOx-based metal-insulator-metal structures were investigated. Two models, diode-like and power-law, have been compared with the aim of detecting any possible correlation among the model parameters. We found that the number of parameters involved can be reduced and that in the case of the power-law model a single parameter is solely required to approximate the I-V curves. This property is used to model the observed hysteretic behavior. The connection with the physics of electron transport through atom-sized constrictions is discussed.

Tue-A-16:00
**Impact of local structural and electrical property of grain boundaries in polycrystalline HfO2 on reliability of SiOx interfacial layer**
*Shubhakar Kalya[1], Kin Leong Pey[1], Raghavan Nagarajan[1], Michel Bosman[2], Sunil Singh Kushvaha[2], Zhongrui Wang[3], Sean Joseph O'Shea[2]*
*[1] SUTD, Singapore; [2] IMRE, Singapore; [3] NTU, Singapore*

Study of local structural and electrical property of grain boundaries (GBs) in polycrystalline high-κ (HK) dielectric and its role on reliability of underlying interfacial layer (IL) is important to assess the overall reliability and failure analysis of HK/IL dielectric stacks. A detailed understanding of this study requires characterization of HK/IL dielectrics with nanometer scale resolution. In this work, we present the impact of surface roughness thickness and GBs containing high density of defects, in polycrystalline HfO2 dielectric on the performance of underlying SiOx IL using atomic force microscopy tool and simulation results. Our experimental and simulation results show SiOx IL beneath thinner HfO2 dielectric and GBs experiences enhanced electric field and likely to trigger the breakdown of SiOx IL.

Tue-A-16:20
**Accelerated Degradation data of SiC MOSFETs for Lifetime and Remaining Useful Life Assessment**
*Thomas Santini[1], Sébastien Morand[1], Mitra Fouladirad[2], Luong-Viêt Phung[3], Florent Miller[1], Bruno Foucher[1], Antoine Grall[2], Bruno Allard[3]*
*[1] Airbus Group Innovations, France; [2] Université de Technologie de Troyes, France; [3] Laboratoire Ampère, France*

The phenomenon of Threshold Voltage instability has been reported to be a critical issue for the first generation of commercial SiC MOSFETs. For aeronautic mission profile, the long term reliability of such device has to be estimated prior to any integration. As far as the author knows, this paper proposes one of the first attempts to use a non-homogeneous Gamma process to model the threshold voltage degradation of a commercial SiC MOSFET. Such approach allows evaluating the time to failure as well as it distribution thanks to the proposed Acceleration Degradation Testing methodology. All the data collected during the ageing tests will be used to model an acceleration factor and to extrapolate the time-to-failure in a given application. Ultimately, the use of Gamma process to evaluate the remaining useful life of electronic component is described as a first step toward prognostic of remaining useful life in embedded power electronics.

Tue-A-16:40
**Degradation Behaviour in Upstream/ Downstream Via Test Structures**
*Jörg Kludt[1], Kirsten Weide-Zaage[1], Markus Ackermann[2], Verena Hein[2], Christian Kovács[2]*
*[1] Leibniz Universität Hannover, Germany; [2] X-FAB Semiconductor Foundries AG, Germany*

The miniaturization process of CMOS components creates new challenges for the development of integrated circuits. Especially the connections with a tungsten via between two metal layers can be a problem. Changes in geometry can bear on reliability problems. For a robust metallization design it is necessary to know how big the influence of the tungsten via alignment is effected on the physical behaviour. Investigations have shown that the alignment has a noticeable effect on the reliability and performance of metal structures.

## Focused Ion Beam and European FIB User Group

Tue-B-10:20-**Invited**
**Precise nanofabrication with multiple ion beams for advanced circuit edit**
*Huimeng Wu, David Ferranti, Lewis Stern*
*Carl Zeiss Microscopy, LLC, United States*

Gallium focused ion beam (Ga-FIB) systems have been used historically in the semiconductor industry for circuit edit. Significant efforts have been invested to improve the performance of Ga-FIB. However, as the dimensions of integrated circuits continue to shrink, Ga-FIB induced processes are being driven to their physical limits. A helium ion beam offers high spatial resolution imaging as well as precise ion machining and sub-10 nm nanofabrication capabilities because the probe size can be brought to as small as 0.25 nm. However, it is limited by its relatively low material removal rate. Recently, the new Zeiss Orion-NanoFab microscope provides multiple ion beams (He, Ne and Ga as an option) into one platform and promotes the further studies of He and Ne induced deposition and etching processes to compare with a Ga ion beam. Because of the mass difference between He, Ne and Ga ions, the interactions of ions with sample surface and precursor molecules result in different sputtering rates, implantation and deposition yields. This presentation gives an overview of our current studies using this new platform to deposit or mill nanostructures for circuit edit.

Tue-B-10:50
**Advanced FIB sample preparation techniques for high resolution TEM investigations of HEMT device structures**
*Michél Simon-Najasek[1], Frank Altmann[1], Susanne Hübner[1], Andreas Graff[1], Helmut Jung[2]*
*[1] Fraunhofer Institute for Mechanics of Materials IWM, Germany; [2] United Monolithic Semiconductors GmbH, Germany*

In this paper an advanced sample preparation technique based on Focused Ion Beam (FIB) optimized for the TEM investigation of high electron mobility transistor (HEMT) structures is presented. It is shown that the usage of an innovative in-situ lift-out method combined with X2 window and backside milling techniques as well as online thickness control and end point detection can significantly improve the quality of electron transparent samples required for high resolution TEM investigations. This advanced preparation flow is evaluated and demonstrated at GaN HEMT structures for atomic resolution TEM investigation.

Tue-B-11:10
**Local thickness and composition analysis of TEM lamellas in the FIB**
*Christian Lang[1], Matthew Hiscock[1], Cheryl Hartfield[2], Michael Dawson[2]*
*[1] Oxford Instruments, United Kingdom; [2] Oxford Instruments, United States*

Lamella thickness and the presence of any surface damage layer created during the preparation in the FIB-SEM greatly impact the quality of subsequent analysis of the sample in the TEM. Here we present a new technique that enables measurement of the local thickness and composition of TEM lamellas and discuss its application to the failure analysis of semiconductor devices. The local thickness in different device regions is accurately measured based on the X-ray emission excited by the electron beam in the FIB-SEM and potential applications in characterising redeposition in the FIB-SEM as well as guiding the preparation of high quality lamellas are outlined on Si and III-V semiconductor devices.

Tue-B-11:30
**Efficient and flexible Focused Ion Beam micromachining of Solid Immersion Lenses in various bulk semiconductor materials – an adaptive calibration algorithm**
*Philipp Scholz[1], Norbert Herfurth[1], Michael Sadowski[1], Ted Lundquist[2], Uwe Kerst[1], Christian Boit[1]*
*[1] Technische Universität Berlin, Germany; [2] DCG Systems, United States*

Focused Ion Beam (FIB) micromachining of Solid Immersion Lenses (SILs) in substrate material offers optical analysis solutions for current and future technologies without the limitations of external SIL systems. This work presents an efficient single iteration calibration algorithm. This algorithm enables the implementation of FIB created SILs using a variety of substrate materials, process chemistries and most importantly different SIL shapes to match sample thicknesses. The successful application on silicon and silicon carbide is presented by creating a 50µm wide refractive lens segment with a radius of curvature of 60µm. Laser scanning microscope images of a silicon sample demonstrate the optical benefit with a measured resolution of 274nm.

Tue-B-11:50
**Focused ion beam contact to non-volatile memory cells**
*Clemens Helfmeier[1], Rudolf Schlangen[2], Christian Boit[1]*
*[1] Technische Universität Berlin, Germany; [2] Nvidia, United States*

Electrical characterization of non-volatile memory cells has been performed. A focused ion beam (FIB) contact procedure is presented that allows to contact the floating gate. Calculations and measurement results on an exemplary floating gate memory cell show intact cell structure with limited retention time after FIB modification. The presented procedure allows the measurement and control of the previously unavailable floating gate current and voltage.

## Reliability & Failure Mechanisms of Organic Devices

Tue-C-13:10-**Invited**
**Massive scale OPV manufacture**
*Frederik C. Krebs*
*Technical University of Denmark, Denmark*

To succeed as a technology the organic solar cell must progress from the laboratory and approach real scale in both manufacture and deployment. This talk will describe how OPV is manufactured at high speed and installed at high speed on a large scale. The installation rate of 100 m long polymer solar cell modules can be accomplished in less than 1 minute yielding power outputs of more than 250 watt. The installation rate is much faster than conventional PV with a lower weight. Operation has been running so far outdoors for more than 1.5 years. New failure modes and new opportunities will be described.

Tue-C-13:50
**Transparent conductive gas diffusion barriers**
*Andreas Behrendt, Christian Friedenberger, Tobias Gahlmann, Sara Trost, Andreas Polywka, Patrick Görrn, Thomas Riedl*
*University of Wuppertal, Germany*

Gas diffusion barriers (GDB) which are the same time highly transparent and electrically conductive would substantially simplify the production of organic electronic devices and open avenues to novel applications. In this work we will show that tin-oxide (SnO2) prepared by low-temperature atomic layer deposition (ALD) is an excellent candidate to meet the above requirements. In a combination with environmentally more sensitive thin metal layers, the SnO2 GDB concomitantly functions as a protective layer to form In-free transparent electrodes which are robust even under damp-heat conditions. These novel electrodes can favorably applied in organic solar cells and OLEDs.

Tue-C-14:10
**Comprehensive analysis of the efficiency roll-off in phosphorescent organic light-emitting diodes**
*Sebastian Wehrmeister*
*University of Augsburg, Germany*

Efficiency roll-off in organic light-emitting diodes (OLEDs) as result of high current densities represents a substantial drawback for technical applications. However, since high brightness is a major request for lighting purposes, high current densities are unavoidable. To identify and analyse the impact of quenching processes on the efficiency, time-resolved spectral measurements on a red phosphorescent OLED with Ir(MDQ)2(acac) as emitter have been performed. We probe the excited states lifetime after a short laser pulse on top of the steady-state region of a rectangular electrical pulse [1]. By continuously increasing the current density of the electrical pulse, the non-radiative decay becomes more likely and the excited states lifetime decreases. A comparison of the calculated external quantum efficiency (EQE) based on these data with direct EQE measurements reveals the influence and the origin of quenching processes on the efficiency roll-off of the device.

Tue-C-14:30
**Investigating UV Stability of Polyfluorene Triarlyamine-based Blue Light-emitting Copolymers**
*Nathan Chander[1], Michael Cass[2], Ji-Seon Kim[1]*
*[1] Imperial College London, United Kingdom;*
*[2] Cambridge Display Technology, United Kingdom*

We report on the effect of UV photoexcitation on the optoelectronic properties of blue light-emitting polymers. Raman, UV-visible absorption and photoluminescence spectroscopy have been used to examine their properties. Raman spectroscopy proves to be a novel, yet powerful technique in the investigation of change in conformation and chemical structures. Results show UV excitation causes degradation and leads to reduced emission intensity due to reactions of the phenyl side groups in arylamine units. Furthermore, photoexcited polymer samples showed evidence of cross-linking between fluorene units in different chains.

Tue-C-15:20
**Temporal phenomena in organic field-effect transistors through Kelvin-Probe Force Microscopy**
*Christian Melzer[1], Christopher Siol[2], Heinz von Seggern[2]*
*[1] Universität Heidelberg, Germany;*
*[2] Technische Universität Darmstadt, Germany*

In the present poster, charging and discharging induced device instabilities of pentacene based organic field-effect transistors (OFETs) are discussed on basis of Kelvin-Probe Force Microscopy (KPFM) measurements performed in the vicinity of the charge reversal point. Even for p-type devices, the remnant charging of the transistor channel with electrons in the hole-depletion mode induces a substantial threshold-voltage shift, thus making the device unstable. Further, on basis of these measurements, the electric-field and carrier-density dependence of the hole mobility in the sub-threshold regime of pentacene based OFETs can be determined. While the local carrier density and the electric field are obtained from the local surface potential and its gradient respectively, the local current is measured by dynamic KPFM following the charge-carrier front entering the transistor channel from the source and drain contacts. Thus, a KPFM based transient experiment is performed. The obtained hole mobility is compared to a transport model for disordered organic semiconductors comprising its carrier-density and field dependence.

Tue-C-15:40
**Neutron Radiation Tolerance of Organic Field Effect Transitors**
*Giuseppe Paterno[1], Valentina Robbiano[1], Victoria Garcia Sakai[2], Franco Cacialli[1]*
*[1] University College London, United Kingdom;*
*[2] ISIS-Neutron and Muon Source, United Kingdom*

Flexible and lightweight carbon-based electronic devices such as organic solar cells (OPVs), organic field effect transistors (OFETs) and organic light-emitting diodes (OLEDs) are likely to have significant industrial and social impact in a variety of areas in the near future, owing to the promise of low manufacturing costs, high production throughput and large area applications. For all these reasons organic electronics devices may represent a valid alternative to their inorganic counterparts, especially for aviation and space applications where payload control is crucial. However, before such promising ideas become a reality, it is important to test the devices reliability in a radiation-harsh environment. Here we report a study of the effect of fast neutron irradiation on OFETs, in order to mimic the effect of the cosmic

rays on this class of devices. In this experiment, we monitored the changes in field-effect mobility of two conjugated polymers namely poly (3-hexylthiophene)[P3HT] and poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2 b]thiophene)[PBTTT] before and after fast neutron irradiation. We observed that neutron radiation induces the formation of defects in the polymer chains (i.e chains scission and oxidation), and this effect is less pronounced in PBTTT. In addition, we found that the decrease of mobility caused by the formation of these defects is counterbalanced by a "radiation-induced annealing effect", which leads to an increase of the field mobility in P3HT as-cast devices and all the PBTTT-based OFETs. In any case, despite the exposure to such a high flux of energetic neutrons ($7.8 \bullet 10^8$ $cm^{-2}$ neutrons with energy >10 MeV) the devices remained functional and, in some cases, we observed an improvement of the field-effect mobility.

Tue-C-16:00
**Stress-Induced Degradation of p- and n-type Organic Thin-Film-Transistors in the ON and OFF States**
*Nicola Wrachien[1], Andrea Cester[1], Gaudenzio Meneghesso[1], Riccardo D'Alpaos[2], Andrea Stefani[2], Guido Turatti[2], Michele Muccini[3]*
*[1] University of Padova, Italy; [2] ETC, Italy; [3] CNR and ETC, Italy*

In this work we analyzed the effect of different stress configurations on p- and n-type organic thin-film-transistors, to emulate the various operating conditions in a real application. Devices showed the largest degradation when they are stressed in the ON condition, because of the uniform charge injection and defect generation in the whole channel area. Charge trapping kinetics and mobility degradation was also strongly dependent on the semiconductor type, suggesting a key-role of the semiconductor on the device reliability.

Tue-C-16:20
**Hybrid VCSEL and DFB organic microlasers**
*Tim Wagner, Andreas Mischok, Markas Sudzius, Robert Brueckner, Vadim G. Lyssenko, Hartmut Froeb, Karl Leo*
*Institut fuer Angewandte Photophysik, TU Dresden, Germany*

We characterize organic vertical-cavity surface emitting lasers, distributed-feedback lasers and their hybrid systems using optical spectroscopy techniques. The corresponding lasing thresholds, output powers, confinement factors etc. are compared and discussed. We demonstrated, that different resonant modes can be coherently coupled to one specific mode which will eventually lase. To achieve this, we have produced a hybrid device which uses Bragg scattering as a coupling mechanism between vertical and lateral modes.

## Failure Analysis

Wed-A-10:40
**Signal noise perturbation on automotive mixed-mode semiconductor device generated by graded substrate defect**
*Yann Weber[1], Linda Buffo[1], Béatrice Vanhuffel[1], Nicholas Lee[1], Neal Stirlen[2], Jeff Chen[2], Xiang-Dong Wang[2]*
*[1] Freescale Semiconduteurs, France;*
*[2] Freescale Semiconduteurs, United States*

The semiconductor technologies evolution allows greatly reducing noise impact on products and many structures have been created to reduce its effect. However, this paper presents the apparition of a noise issue during the production of a mixed-mode device dedicated to automotive applications. The research investigations concerned the fact that failure was not detected in production but at customer level; therefore, it was determinant to understand the root cause of this failure mode to drive corrective actions in order to secure customer. The challenge was to analyse noise in Failure Analysis (FA) without fault spatial localization results. Indeed, Infrared (IR) EMission MIcroscopy (EMMI) or Thermal Laser Stimulation (TLS) were unable to provide any defective area in the product. The lack of failing device identification required to combine electrical and design analysis in order to define hypothesis on the failure origin. It is then possible to drive physical investigations by different approaches, using physical cross-section, SIMS and SCM analysis. Finally, the obtained complementary results will be discussed and an explanation of the failure mechanism will be presented as the root cause issue, allowing defining the defective step in production process.

Wed-A-11:00
**Quantitative Scanning Microwave Microscopy: A calibration flow**
*Thomas Schweinboeck, Soeren Hommel*
*Infineon, Germany*

A procedure for doping concentration calibration is presented using Scanning Microwave Microscopy (SMM) measurements of a purpose-built calibration sample comprising a wide range of doping concentrations of both n- and p-type implants at the sample surface. A transmission line model that takes into account the physical elements forming the evaluated network including modelling the tip-sample-interaction is used to evaluate the criticality of parameters affecting the measured signal. Using a vertical DMOS sample a showcase flow for quantification is exercised and the attainable degree of accuracy is discussed.

Wed-A-11:20
**Electro Optical Therahertz Pulse Reflectometry, a non destructive technique to localize defects on various type of package**
*Antoine Reverdy[1], Maxime Marchetti[2], Alessandra Fudoli[3], Vincent Goubier[2], Morgan Cason[3]*
*[1] Sector Technologies, France; [2] ST Microelectronis, France; [3] ST Microelectronis, Italy*

Localizing defects (and, particularly, open defects) at package level is becoming a real challenge for Failure Analysis Laboratories due to package diversity and complexity. One of the well known approaches to address this set of problems within the device is the Time Domain Reflectometry (TDR). The main limitation of this technique is the lack of resolution and sensitivity. Electro Optical Terahertz Pulse Reflectometry (EOTPR) is overcoming these limitations by using a photoconductive terahertz pulse generation and detection technology, resulting in a system with: (i) high measurement bandwidth, (ii) extremely low time base jitter, and (iii) high time base resolution and range with greater sensitivity. In this paper we will present some case studies on various types of devices on which EOTPR approach provided interesting results.

Wed-A-11:40
**Exact 3D Simulation of Scanning Electron Microscopy Images of Semiconductor Devices in the Presence of Electric and Magnetic Fields**
*Mauro Ciappa[1], Alexey Yu. Illarionov[2], Emre Ilguensatiroglu[1]*
*[1] ETH Zurich, Switzerland;*
*[2] Integrated Systems Laboratory, ETH, Switzerland*

Simulations of Scanning Electron Microscopy images of semiconductor devices in the presence of electric fields are usually too simplistic, since they just rely on approximated solutions of the Poisson equation. In this paper, the 3D Poisson equation is solved in a TCAD environment, which accounts for realistic boundary conditions, as well as for complex physical effects like the formation of space charge regions in semiconductors and the polarization of dielectrics. The calculated solution is then passed to a Monte Carlo code that implements a new electron tracking engine optimized for speed, stability, and accuracy. After introducing the new tracking engine, three simulation examples are presented dealing with the presence of an extraction field, self-charging of the irradiated sample, and potential contrast in a biased silicon junction.

Wed-A-12:00
**A comprehensive study of the application of the EOP techniques on bipolar devices**
*Mehdi Mohamed Rebai[1], Frédéric Darracq[2], Philippe Perdu[3], Jean-Paul Guillet[2]*
*[1] MS Laboratory & CNES, France; [2] IMS Laboratory, France; [3] CNES, France*

In addition to Emission Microscopy, Electro-Optical Probing (EOP) technique has shown its efficiency in the world of failure analysis since the last decades and its ability to measure waveforms on various devices. The different physical parameters that affect and modify the reflected laser probing beam through active silicon components are just beginning to be well known. All the physical and environmental parameters contribute to the modulation of the reflected laser probing beam onto structures under test. However, the origins of EOP signals from bipolar transistors junctions used in a lot of analog devices are not well known and not that much described in the literature.

In this paper we present backside EOP signal measurements from bipolar devices. We compare these measurements on a failed transistor and on a reference transistor and we interpret the results according to a model previously developed for silicon devices (MOS and Bipolar).

Wed-A-13:30-**Invited**
**Enabling Higher Fault Isolation Resolution through Advanced Optics**
*Derryck T. Reid*
*Heriot-Watt University, United Kingdom*

Solid-immersion lenses (SILs) play an essential role in enabling high-resolution backside optical imaging and probing of CMOS circuits. Here, we review the core concepts of SIL imaging, distinguishing between the cases of hemispherical and aplanatic SILs and summarising the performance enhancements available in each case. Approaches to further extending the resolution by engineering the polarisation state and / or the intensity distribution across the pupil of the SIL backing objective are discussed, specifically the potential benefits from using radial polarisation and annular illumination. We then discuss the new failure analysis technique of two-photon laser-assisted device alteration LADA (2pLADA), which uses 1280-nm femtosecond pulses to inject photocarriers by two-photon absorption into a highly localised region within the circuit. The results presented will compare the performance of this new embodiment with the original implementation of LADA using CW 1064-nm lasers. Specifically, we show how by using a synchronized pulsed laser, logic transition waveforms can be acquired that can be used to measure propagation delays of the critical path signals. The ability to synchronize the laser pulse with the internal circuit signals is shown to result in improved localization isolation of the LADA sites.

Wed-A-14:00
**Magnetic Field Imaging for non destructive 3D IC testing**
*Jan Gaudestad, Antonio Orozco*
*Neocera, United States*

Due to magnetic fields ability to penetrate through all materials used by the semiconductor industry, a unique ability not found in any other techniques, it has become an important technique for detecting shorts, leakages and opens in multi stacked Through Silicon Via samples. We show in this paper how magnetic field imaging is being used to image the current in a TSV stacked silicon device with a new 3D analysis algorithm of the distance from the top of the stacked device to the current path.

Wed-A-14:20
**Pattern image enhancement by extended depth of field**
*Samuel Chef[1], Bastien Billiot[2], Sabir Jacquir[2], Kevin Sanchez[3], Philippe Perdu[3], Stéphane Binczak[2]*
*[1] University of Burgundy & CNES, France; [2] University of Burgundy, France; [3] CNES, France*

Most optical defect localization techniques such as dynamic laser stimulation or photon emission microscopy require a pattern image. The main purpose is to navigate onto the device but it also enables the analyst to vizualize where is located the monitored activity by superimposition. The defect localization work flow usually starts at low or medium magnification. At these scales several factors can lead to a lack of orthogonality of the sample with the optical axis of the system. Therefore, images can be locally out of focus. In this paper, a method based on depth of field extension is suggested to correct the pattern image.

Wed-A-14:40
**Backside spectroscopic photon emission microscopy using intensified silicon CCD**
*Arkadiusz Glowacki[1], Christian Boit[1], Philippe Perdu[2], Yoshitaka Iwaki[3]*
*[1]Technische Universität Berlin, Germany; [2]CNES, France; [3]Hamamatsu Photonics, Germany*

A typical solution for backside analysis of photon emissions from semiconductor integrated circuits is the InGaAs detector. It takes advantage of the transparency of the silicon material to wavelengths within its spectral sensitivity regime. However, it has been recently demonstrated that light spectral information extraction is more reliable when using silicon CCDs assisted by proper backside bulk Si thinning of the device. In this paper we demonstrate further improvement of the photon emission spectrum acquisition using the solid-state intensified silicon CCD. Using such solution it is possible to significantly reduce the analysis time, expand the detectable spectral regime as well as improve the spectral wavelength resolution.

Wed-A-15:00
**Fretting corrosion: analysis of the failure mechanism for low voltage drives applications**
*Elena Mengotti[1], Liliana Duarte[1], Juha Pippola[2], Laura Frisk[2]*
*[1]ABB, Switzerland; [2]Tampere University of Technology, Finland*

In many power electronics products, such as low voltage drives, the mechanical and electrical connection between PCBAs having different functionality is obtained though board-to-board connectors. A common failure mechanism for these components part is fretting corrosion. This failure mechanism results from mechanical micro-motion of the two parts with respect to each other and causes a wear damage at the asperities of the contact surface resulting in an increase of the resistance between the two parts and which finally triggers various device failure. Failures that are due to a missed communication may have a different effect on the total product depending on the circuit diagram of the two boards. In this paper microstructure and chemical investigation were performed at the junction part of the connectors. We also investigate the changes on chemical-composition at the contact zone of the connectors as new and after product level reliability testing which includes stressors like humidity, temperature, temperature cycling and vibration. SEM-EDX showed micro mechanical fractures of the plating material for the sample where an increase in the ohmic resistive measurement was observed before imaging.

## Power Devices Reliability

Tue-B-15:20
**Prediction of Supercapacitors Floating Ageing with Surface Electrode Interface based Ageing Law**
*Ronan German[1], Ali Sari[1], Pascal Venet[1], Mohamed Ayadi[2], Olivier Briat[3], Jean-Michel Vinassa[3]*
*[1]Université Lyon , France; [2] IFSTTAR Satory, France; [3]Université de Bordeaux, France*

Supercapacitors (SC) are power devices used as transitory energy sources for peak power applications such as braking energy recovering in hybrid transports. They are subject to electrochemical ageing processes which affect their performances and reliability. Consequently, the main influence factors on SC ageing kinetic are temperature and voltage. Some ageing law based on experiment results have already been produced (for instance the Eyring law) but are not precisely related to physical considerations. In this article, we propose to use an ageing law which links ageing kinetic with the growth of an interface layer between the electrodes surface and electrolyte, called here SEI (Solid Electrode Interface) layer. In order to have a representative sample, 81 commercial supercapacitors coming from 3 different manufacturers will be tested through floating ageing tests at different voltage and temperature constraints. All presented components are manufactured with the most widespread SC technology (double layer SC using activated carbon for electrode and acetonitrile). The fitting of SC experimental ageing results and SEI ageing law is achieved. Then the effect of temperature and voltage on SEI ageing law parameters is performed.

Tue-B-15:40
**Eliminate Infant Mortality in Metallized Film Capacitors by defect detection**
*Patrick McCluskey, Nga Man Li*
*University of Maryland, United States*

Metallized film capacitors are known for their self-healing property in which weak electrical defects would not cause a catastrophic short circuit and continue to work with small partial discharge (PD) current and a slight drop of capacitance. If defects exist in a large quantity or in critical dimensions and shapes, this effect will become non trivial and can cause early failure of the capacitor. Burning-in is a widely adopted way of eliminating infant mortality of components but it has one major disadvantage - consumes usable lifetime. This paper focuses on identifying defects introduced to the wound metallized film during manufacture using Non-Destructive Analysis (NDA). Defect parameters and common failure accelerating factors, i.e. temperature and effective voltage were related using experiment and Finite Element Analysis (FEA). Lifetime of defective capacitors could then be estimated by an empirical model. From the relationship developed for defect parameters and capacitor lifetime, we aim to screen out potential early failing capacitors by defect detection with NDA.

Tue-B-16:00
**Metallized film capacitors ageing law based on capacitance degradation**
*Maawad Makdessi, Ali Sari, Pascal Venet*
*Université Lyon 1, France*

In view of their potential for high dielectric breakdown strengths, low dissipation factors and good dielectric stability over a wide range of frequencies and temperature, metallized film capacitors are very used in power electronics applications. Nevertheless, capacitors failure occurring on board can have catastrophic consequences on a human and/or financial scale; a good acquaintance of their deterioration over time would contribute in the improvement of the availability of the whole system by performing a predictive maintenance on the component. This operation requires the knowledge of the capacitor ageing law and their failure mechanisms associated to the application. Capacitance loss can be mainly attributed to the self-healing process occurring in metallized film capacitors when used under high steady electrical and thermal stresses. In this paper, an original capacitance ageing law is proposed based on the identification of voltage and temperature degradation kinetics from three experimental ageing tests performed at different voltage and temperature constraints. 34 capacitors provided from different manufacturer using polyester film as dielectric have been studied and compared to validate the proposed law.

Wed-B-10:40
**Impact of gate drive voltage on avalanche robustness of trench IGBTs**
*Michele Riccio[1], Luca Maresca[1], Andrea Irace[1], Giovanni Breglio[1], Yohei Iwahashi[2]*
*[1] Università di Napoli Federico II, Italy; [2] Toyota Motor Corporation, Japan*

In recent years many studies have been carried out to assess the avalanche robustness of new IGBT designs. Experimental evidences and numerical simulations have pointed the attention toward the shape of the forward blocking I-V curve. Particularly, the presence of a Negative Differential Resistance (NDR) branch can be responsible of not-uniform current conduction and a reduced avalanche energy capability. In this work, the impact of the gate drive voltage on Trench-IGBTs avalanche capability is deeply analysed by means of TCAD simulations and IR thermal measurements during Unclamped Inductive Switching (UIS) test on a 1.2kV - 200A device. The effect of the gate biasing, during the blocking-state, on the breakdown voltage of the device active area is investigated as the main cause of the interplay between the IGBT cells and the termination. As a result, an increased avalanche capability is proven for negative gate bias and a theoretical explanation of the involved phenomena is provided.

Wed-B-11:00
**Thermal-aware design and fault analysis of a DC/DC parallel resonant converter**
*Giuseppe De Falco, Michele Riccio, Giovanni Breglio, Andrea Irace*
*DIETI - Università di Napoli Federico II, Italy*

In this paper a 3-D electrothermal (ET) analysis of a DC-DC parallel resonant converter (PRC) for constant current (CC) application is presented. A full 3-D electrothermal simulation approach is proposed at application level to provide a support for the design stage and to analyse possible fault condition s inside the active devices. Simulations and measurements have been performed on a 100 W - 2 A prototype of a PRC-CC circuit with 80 kHz nominal switching frequency. In particular, in the reported case study, the analysis has been focused on the full-bridge section of the circuit in order to prove the effect of the soft switching operation, introduced by the resonant technique, and consider the effect of possible fault conditions. To this purpose an unexpected short-circuit condition on a power MOSFET composing the H-bridge is considered, to evaluate the ET circuit behaviour and the time-to-failure of the power section. Considerations are carried out in terms of minimum requirements of protection circuits which must be fulfilled in order to avoid catastrophic system failure. The paper first gives a brief introduction of the simulation environment, evidencing the proposed approach for steady-state and transient analysis. Afterwards, a description of the analysed circuit, explaining the key features and the working principle, is given. Finally the simulations results and the experimental measurements are presented.

Wed-B-11:20
**Comparison of Temperature Limits for Trench Silicon IGBT Technologies for Medium Power Applications**
*Xavier Perpiñà[1], Xavier Jordà[1], Javier León[2], Miquel Vellvehi[2], Daniel Antón[3], Sergio Llorente[3]*
*[1] IMB-CNM, Spain; [2] CNM, Spain; [3] BSH, Spain*

This work focuses on determining the switching limits in temperature for Reverse Conducting IGBTs and compares them to "conventional" IGBTs (based on trench technologies) in 600V-50 A application scenario. After, their leakage current under blocking state is tested at several working temperatures. In fact, we focused on study of the leakage current that limits blocking safe operating area with temperature, determining the maximum temperature at which component fails. After ensuring the thermal limits for their operation to avoid the failure, overcurrent tests have been performed, our study being focused on studying the overcurrent induced failures due to thermal effects using short circuit tests adapted to our needs. As a result, we observe that RC-IGBTs integrating the free-wheeling diode show higher performances than the other components manufactured without incorporating such a structure internally.

Wed-B-11:40
**3-D electrothermal simulation of active cycling on smart power MOSFETs during Short-Circuit and UIS conditions**
*Michele Riccio[1], Vincenzo D'alessandro[1], Andrea Irace[1], Gilles Rostaing[2], Mounira Berkani[2], Stéphane Lefebvre[2], Philippe Dupuy[3]*
*[1] University Federico II, Italy; [2] SATIE, CNAM, CNRS, ENS Cachan, France; [3] FREESCALE, France*

Active cycling of power devices operated in harsh conditions causes high power dissipation, resulting in critical electrothermal and thermo-mechanical effects that can lead to catastrophic failures. This paper analyzes the ageing-induced degradation of the chip metallization and its impact on the device robustness during short-circuit (SC) and unclamped inductive switching (UIS) tests. A 3-D electrothermal simulator relying in a full circuit representation of the whole device and exploiting the finite difference method to describe the heat propagation is used to predict the behavior of a power MOSFET affected by various ageing levels. It is found that ageing can jeopardize the robustness of the transistor when subject to SC conditions due to the exacerbated de-biasing effect on the gate-source voltage distribution; conversely, this mechanism does not arise under UIS avalanching conditions. This allows explaining the difference in time-to-failure experimentally observed for transistors subject to SC and UIS tests and dissipating the same energy.

Wed-B-12:00
**Performance drifts of N-MOSFETs under pulsed RF life test**
*Mohamed Gares*
*ISIM, University of Gabes, Tunisia*

This paper presents a reliability life test bench specifically dedicated to high RF power devices for lifetime tests under pulse conditions. The monitoring of RF power, drain, gate voltages and currents under various pulses and temperatures conditions are investigated. A 3000 hours pulsed RF life test has been conducted on a dedicated RF S-band test bench in operating modes. The investigation findings of degradations of critical electrical parameters derived from the data treatment after this accelerated ageing tests are presented. Numerous duty cycles are applied in order to stress Lateral-Diffused Metal–Oxide-Semiconductor (LDMOS). It shows with tracking of a set of RF parameters (Pout, Gain and Drain Efficiency: DE) that the dominant degradation phenomenon is linked to hot carriers generated interface states (traps) and trapped electrons. Which results in a build up of negative charge at Si/SiO2 interface and the main cause appear with incidence on RF power devices. Physical simulation software (Silvaco-Atlas) has been used to locate and confirm these phenomena.

Wed-B-13:30-**Invited**
**Lifetime Modeling and Simulation of Power Modules for Hybrid Electrical / Electrical Vehicles**
*Markus Thoben*
*Infineon, Germany*

In hybrid electrical vehicles (HEV) and electric vehicles (EV) power semiconductors, packaged in a module, are used. Packaging technologies are suffering several wear out mechanisms, that are typically induced by thermal or power cycling. The type of wear out mechanism is affected by the connection technology but also by the load type. In the design of the inverter the mission profile simulation of the power module is an important step to ensure operation of the power module over the complete vehicle lifetime. Influences of application parameters are presented. Physics of failure based FEM simulation can help to develop appropriate lifetime models which are basis for the mission profile simulation. Available Power Module technology achieves the lifetime requirement for Hybrid Electric Vehicles/Electric Vehicles, if the described method is applied in the design phase of the inverter.

Wed-B-14:00
**Study of Thermal Cycling and Temperature Aging on PbSnAg Die Attach Solder Joints for High Power Modules**
*Franc Dugal[1], Mauro Ciappa[2]*
*[1] ABB, Switzerland; [2] ETH Zurich, Switzerland*

An experimental analysis is presented of the degradation of PbSnAg die attach solder joints in high-power IGBT modules submitted to cycling and static temperature aging. The investigation focuses on the characterization of the microstructure of the solder alloy and on the formation of intermetallic phases at the interfaces. After microsectioning, degraded solders are compared to virgin devices by different analytical techniques, including Scanning Electron Microscopy, Energy Dispersive X-ray Analysis, X-ray imaging, and Scanning Acoustic Microscopy.

Wed-B-14:20
**Improving the FE Simulation of Molded Packages Using Warpage Measurements**
*Saskia Huber[1], Marius van Dijk[2]*
*[1] Fraunhofer, Germany; [2] Fraunhofer IZM, Germany*

Due to the constant development of new components in microsystem technology the possibility to guarantee the reliability and lifetime of these components is essential. An efficient method for this purpose is Finite Element (FE) modeling. In order to shorten lengthy and expensive lifetime tests, FE simulations become more and more necessary. To obtain suitable FE models, multitude of material and technical component characteristics are needed. However, due to the rapid development of new materials, the characteristics are often insufficient or even unknown. Therefore additional measurements of the material or the complete system are necessary. Which material data is required depends first and foremost on the component and its usage.
In this paper the importance of temperature dependent topographic measurements for the simulation model of a package design (Smart Power Module) will be demonstrated. The warpage of a whole package was measured at different temperatures in order to obtain unknown material behavior like the chemical shrinkage. Therefore the Shadow Moiré Measurement Method was utilized. This work will focus on how to obtain experimental data of two different molding compounds (MC) in several stages of post curing as well as implementing the results in a FE simulation model.

Wed-B-14:40
**Reliability of Cu nanoparticle joint for high temperature power electronics**
*Toshitaka Ishizaki[1], Yasushi Yamada[2], Toshikazu Satoh[1]*
*[1] Toyota Central R&D Labs., Inc., Japan; [2] Daido Univeristy, Japan*

Power cycle reliability of Cu nanoparticle joint has been studied for high temperature operation of power devices. Al2O3 heater chips and Cu-65wt%Mo baseplates were joined by Cu nanoparticles and Sn-0.7Cu and power cycle tests of 65ºC/200ºC and 65ºC/250ºC were carried out on the joints. The Cu nanoparticles were prepared by reducing Cu carbonate in ethylene glycol with dodecanoic acid + dodecyl amine (C12) and decanoic acid and decyl amine (C10) as capping agents. A power cycle test of 65ºC/200ºC did not inflict severe damage on the Cu nanoparticle joints so that there were not many cracks formed after 3000 cycles. Vertical cracks were formed in the C12 Cu nanoparticle joint after 3000 cycles of 65ºC/250ºC test, however the maximum temperature during the power cycle test did not change at all because vertical cracks did not have an effect on preventing heat flow. On the contrary, lateral cracks were completely formed in the Sn-0.7Cu soldered joint after 200 cycles of 65ºC/200ºC test and in the C10 Cu nanoparticle joint after 360 cycles of 65ºC/250ºC test. In these experiments, the maximum temperatures were rapidly increased because heat conduction was prevented across the formed lateral cracks.

Wed-B-15:00
**Dielectric Strength and Thermal Performance of PCB-Embedded Power Electronics**
*Wolfgang Wondrack[1], Richard Randoll[1], Andreas Schletz[2]*
*[1] Daimler, Germany; [2] Fraunhofer IISB, Germany*

Advantages of embedded power electronics compared to classical DCB soldered and bonded modules are smaller size, less weight, and cost savings [2]. In addition, the low parasitic inductance provided by the embedded technology offers the potential to better utilize the maximum chip voltages. Heat-spreading in the thick copper plate inside the printed circuit board improves the thermal performance. At the same time, combination with silver sintering for the die attach, higher lifetimes compared with standard DCB (direct copper bonding) assemblies may be reached. Potential risks of this new approach are lifetime limitations, and restricted dielectric strength and thermal performance of the module. In order to evaluate the embedding technology for power devices, test samples were designed and fabricated. In order to evaluate these risks, the thermal performance and the thermomechanical strain in these samples were simulated and compared with measured values. Temperature-dependent partial discharge tests have been conducted.

Thu-B-13:30
**The Influence of Liners with Ti, Ta or Ru Finish on Thin Cu Films**
*David Gross[1], Sabine Haag[1], Martin Schneider-Ramelow[2], Klaus-Dieter Lang[2]*
*[1] Robert Bosch GmbH, Germany; [2] Fraunhofer IZM, Germany*

The influence of the different liner material stacks Ti-N/Ti, Ta-N/Ta and Ta-N/Ru on the microstructure of 1 µm thick sputtered Cu films is examined prior to and after annealing. It is shown that the liner has an impact on the orientation distribution of the Cu grains and seriously affects the defect density in the Cu films. The relationship to the measured Cu resistivity is considered which strongly depends on the microstrain.

Thu-B-13:50
**HCS Degradation of 5nm Oxide High-Voltage PLDMOS**
*Christina Olk, Stefano Aresu, Ralf Rudolf, Michael Röhner, Wolfgang Gustin*
*Infineon, Germany*

Hot carrier (HC) injection, inducing drain and gate leakage current increase in 5nm oxide p-channel LDMOS transistors, is investigated. Devices with two different drain implants are studied. At low gate voltage (VGS) and high drain voltage (VDS), reduction of the ON-resistance (RON) is observed. At stress times at which RON almost reaches its constant level, an increase of the drain leakage in OFF state (VDS=-60V, VGS=0V) is observed. Longer stress time leads to increased gate leakage and in some cases oxide breakdown. In contrast to what was reported for devices with 25nm gate oxide thickness, the threshold voltage of 5nm gate oxide PLDMOS transistors does not drift. The experimental data can be fully explained by hot carrier injection and the oxide damage can be explained by two different and competing degradation mechanisms. By combining experimental data and TCAD simulations we are further capable to locate the hot spot of maximum oxide damage in the accumulation (Acc) region of the PLDMOS.

Thu-B-14:10
**Risk and reliability assessment about a manufacturing issue in a power MOSFET for automotive applications**
*Corinne Bergès, Pierre Soufflet, Abdeslam Jadrani*
*Freescale, France*

In the automotive semiconductor industry, risk assessments are requested by customers on quality incidents that happen in the assembly line or in field. More rarely, in a die business context, such a study is requested about a defect observed during the optical inspection performed by the customers on the known good dice after assembly. This article deals with the case of pin holes in the top metal surface of a MOSFET component. The risk assessment is addressing detection, occurrence and severity of the defect: this implies process and failure analysis. Also, reliability has been carried out, by completing accelerated and typical stress tests.

Thu-B-14:30
**Structure oriented compact model for advanced trench IGBTs without fitting parameters for extreme condition: part II**
*Junpei Takaishi[1], Syohei Harada[1], Masanori Tsukuda[2], Ichiro Omura[1]*
*[1] Kyushu Institute of Technology, Japan; [2] ICSEAD, Japan*

Compact model for expressing turn-off waveform for advanced trench gate IGBTs is proposed even under high current density condition. The model is analytically formulated only with device structure parameters so that no fitting parameters are required. The validity of the model is confirmed with TCAD simulation for 1.2 kV class IGBTs. The proposed turn-off model is sufficiently accurate to calculate trade-off curve between turn-off loss and forward voltage drop under extremely-high current conduction, so that the model can be used for system design with the advanced trench gate IGBTs.

Thu-B-14:50
**Short-circuit protection for an IGBT with detecting the gate voltage and gate charge**
*Kazunori Hasegawa[1], Hidetaro Yoshida[1], Kota Hamada[1], Masanori Tsukuda[2], Ichiro Omura[1], Kenichi Yamamoto[1]*
*[1] Kyushu Institute of Technology, Japan; [2] The International Centre for the Study of East Asian Development, Japan*

This paper proposes a new short-circuit protection method for an IGBT. The proposed method is characterized by detecting not only gate charge but also gate voltage of the IGBT. This results in a shorter protection time, compared to the previous method that detects only the gate charge. A real-time monitoring system using an FPGA and A/D converters is used for the proposed protection method. Experimental results verify that the proposed method achieves a protection time of 390 ns, which is reduced by 68% compared to the previous method.

## Chip-Package Interactions and 3D Reliability & Failure Mechanisms

Wed-C-10:40
**Reliability Challenges for Barrier/Liner System in High Aspect Ratio Through Silicon Vias**
*Yunlong Li, Stefaan Van Huylenbroeck, Els Van Besien, Xiaoping Shi, Chen Wu, Michele Stucchi, Gerald Beyer, Eric Beyne, Ingrid De Wolf, Kristof Croes*
*IMEC, Belgium*

The reliability results for barrier/liner systems in different high aspect ratio (5×50µm) through silicon vias (TSV) are summarized and compared. Quite a few factors can influence the TSV barrier/liner reliability performance, including the TSV trench etch process, the oxide liner material/thickness, etc. The challenges for more advanced TSV technology nodes (e.g. 3×50µm) are also discussed and possible solutions are recommended.

Wed-C-11:00
**Submicron XCT for failure analysis in advanced packaging**
*Markus Löffler[1], S. Niese[1], J. Wolf[2], Ehrenfried Zschech[3]*
*[1]TU Dresden, Germany; [2] Fraunhofer IZM-ASSID, Germany;*
*[3]TU Dresden and Fraunhofer IKTS-MD, Germany*

In order to embed more functionality and performance into the same design space, 3D IC integration technology is one of the routes towards further miniaturization of ICs and consequently, printed circuit boards. 3D TSV (through silicon via) stacking of wafers or dies requires die-to-die interconnections to conduct electricity and heat. Typically micro bump contacts with solder (e.g. AgSn) and Cu TSV are used. Process and quality control of these advanced packaging processes and the resulting 3D products is challenging, but a necessity to avoid costly device failures due to packaging faults. We employed a lab-source microfocus X-ray computed tomography system to demonstrate the capability of non-destructive detection and characterization of such die-to-die interconnections with features in the micron range. Structural characteristics and flaws, such as electrical shorts, voids, filling faults, or composition features could be reliably identified. We demonstrate the use of submicron X-ray computed tomography for non-destructive process development, process monitoring and failure analysis in 3D TSVs stacks on a packaged test chip with dimensions 10 × 10 × 0.9 mm³ that consists of six chip layers with TSVs and microbumps as well as AgSn solder.

Wed-C-11:20
**The effects of etching and deposition on the performance and stress evolution of open through silicon vias**
*Lado Filipovic, Siegfried Selberherr*
*Technische Universität Wien, Austria*

The effects of silicon etching using the Bosch process and LPCVD oxide deposition on the performance of open TSVs are analyzed through simulation. Using an in-house process simulator, a structure is generated which contains scalloped sidewalls as a result of the Bosch etch process. During the LPCVD deposition step, oxide is expected to be thinner at the trench bottom when compared to the top; however, additional localized thinning is observed around each scallop. The scalloped structure is compared to a structure where the etching step is not performed, but rather a flat trench profile is assumed. Both structures are imported into a finite element tool in order to analyze the effects of processing on device performance. The scalloped structure is shown to have an increased resistance and capacitance when compared to the flat TSV. Additionally, the scalloped TSV does not perform as well at high frequencies, where the signal loss is shown to increase. However, the scallops allow the TSV to respond better to an applied stress. This is due to the scallops' enhanced range of motion and displacement, meaning they can compensate for the stress along the entire sidewall and not only on the TSV top, as in the flat structure.

Wed-C-11:40
**Advanced methods for mechanical and structural characterization of nanoscale materials for 3D IC integration**
*Christoph Sander, André Clausner, Martin Gall*
*Fraunhofer IKTS-MD, Germany*

Managing the emerging internal mechanical stress in chips particularly if they are 3D stacked is a key task to maintain performance and reliability of microelectronic products. Hence, a strong need of a physics-based simulation methodology/flow emerges. This physics-based simulation, however, requires materials parameters with high accuracy. A full-chip analysis can then be performed, balancing the need for local resolution and computing time. The key for an efficient simulation of a 3D stacked IC is a comprehensive database with material properties for multiple scales for the affected materials. Therefore, effective "composite-type" materials data for several regions of interest are needed. Advanced techniques to measure FEA- and design-relevant properties such as adhesion properties, local and effective Young's modulus, and effective CTE values are presented.

Wed-C-12:00
**Stress Analyses of High Spatial Resolution on TSV and BEoL Structures**
*Dietmar Vogel[1], Ellen Auerswald[1], Juergen Auersperg[1],*
*Parisa Bayat[2], Raul Rodriguez[2], Dietrich Zahn[2], Sven Rzepka[1],*
*Bernd Michel[1]*
*[1]Fraunhofer ENAS, Germany;*
*[2]Technical University Chemnitz, Germany*

Knowledge and control of local stress development in BEoL stacks and nearby TSVs in advanced 3D integrated devices is a key to their thermo-mechanical reliability. The paper presents a combined simulation / measurement approach to evaluate stresses generated in the result of the TSV and BEoL stack manufacturing and 3D bonding processes. Stress measurement methods of high spatial resolution capability (microRaman and FIB based stress release techniques) are used to obtain stress data from real components as manufactured. Finite element analysis (FEA) allows a more accurate interpretation of measurements results as well as a subsequent comprehensive analysis of failure behaviour. The paper gives an introduction to the applied local stress measurement on advanced multi-layer systems and 3D integration components referring to the state-of-art capabilities and limitations. The need of experimental stress data generation is illustrated on FEA examples. Illustration is given for FEA applications on 3D IC integration components currently lacking appropriate residual stress input for an assumed initial state.

## Reliability & Failure Mechanisms in Packages and Assembly

Wed-C-13:30-**Invited**
**Reliability of Wafer Level Chip Scale Packages**
*René Rongen*
*NXP Semiconductors, Nijmegen, Netherlands*

This paper describes applied reliability for semiconductor components in Wafer Level Chip Scale Packages (CSP). To develop and qualify reliable products, the failure mechanism driven approach is to be followed instead of the stress test driven one. This will be explained by elaborating on two failure mode cases assess in WL-CSP: cracks in the passivation layer and top metal of the die/silicon and electromigration in the solder joints. A new TMCL test method is described that covers the direct (thermo) mechanical interaction between PCB and the die/design via the solder joint. In addition, the relevance of Finite Element Modeling to understand the origin of failure modes is shown which allows for optimizing designs and materials. Finally, the concept of life time prediction, starting from application use descriptions and mission profiles, is introduced. Reliability testing, modeling and life time prediction/ reliability statistics are combined in one framework to accommodate for the creation of application specific highly reliable components.

Wed-C-14:00
**High temperature degradation of palladium coated copper bond wires**
*Jörg Krinke, Dragica Dragicevic, Susann Leinert, Erik Frieß, Joachim Glück*
*Robert Bosch GmbH, Germany*

High temperature storage lifetime tests of palladium coated copper bond wires (pcc-wires) beyond 1000h@150°C lead to an increased number of broken stitches during wire bond pull test. In this article we show that there is an intrinsic degradation of pcc-wires: assumed defects in the Pd layer allow a temperature driven diffusion of Cu to the Pd surface reacting to CuO on the wire surface. Whole Cu grains of the wire core are dissolved in this way, weakening the bond wire strength to very low values. The degradation mechanism of pcc-wires is found in both cases, in molded packages and at non-molded wires from the spool. We present the results after temperature storage at 150°C, 175°C, 200°C, and 250°C up to 5000h.

Wed-C-14:20
**Interface microstructure effects in Au thermosonic ball bonding contacts by high reliability wire materials**
*Benjamin März[1], Andreas Graff[1], Robert Klengel[1], Matthias Petzold[2]*
*[1] Fraunhofer Institute for Mechanics of Materials Halle, Germany;*
*[2] Fraunhofer IWM Halle, Germany*

Palladium-doped and (Cu, Pt)-doped high reliability gold wires were used to form wire bond interconnects on aluminum IC metallization. By isothermal annealing of wire bond samples the formation of intermetallic Au-Al phases was stimulated. SEM/EBSD investigations of the phase regions exhibited significantly slower isothermal growth rates compared to a reference gold wire. Correlating TEM, STEM-EDXS and nanobeam diffraction analyses revealed that Pd is preferentially incorporated into the Al3Au8 intermetallic forming a new stable phase but additionally can obviously form a new Pd-rich ternary intermetallic. In comparison, Cu dopants are also accumulated into a new Al-Au-Cu phase while Pt is rather found agglomerating within grain boundaries and interfaces. These results suggest a qualitative diffusion barrier model that allows discussing how wire doping can affect the bond contact microstructure, thus increasing the lifetime of bond contacts.

Wed-C-14:40
**Reliability of thick Al wire: A study of the effects of wire bonding parameters on thermal cycling degradation rate using non-destructive methodologies**
*Elaheh Arjmand, Pearl Agyakwa, C. Mark Johnson*
*University of Nottingham, United Kingdom*

The effect of bonding parameters on the reliability of thick Al wire bond is investigated. Five bonding parameters (time, ultrasonic power, begin-force, end-force and touch-down sensor steps) were varied with five levels, producing 25 different designs. The bond signals of the ultrasonic generator were collected during bonding in order to obtain prior quality information of bonded wires. 3D x-ray tomography was then used to evaluate bond degradation during passive thermal cycling between -55 °C and 125 °C. Tomography datasets were obtained from the as-bonded condition and during cycling. Initial results clearly show the effect of ultrasonic power on wire bond attached area. Furthermore, they show the importance of appropriate begin- and end-force for achieving well attached and or reliable bonds. Analysis of the virtual cross-sections indicates a correlation between the bond signal (i.e. the initial bond quality) and wire bond damage/degradation rate. An improved understanding of the wire bonding process was achieved by observing the effect of different bonding parameters on the ultrasonic generator signal and degradation rate under thermal cycling.

Wed-C-15:00
**Qualification procedure against moisture for embedded capacitors**
*Helene Fremont[1], Jörg Kludt[2], Massar Wade[1], Kirsten Weide-Zaage[2], Isabelle Bord-Majek[1], Geneviève Duchamp[1]*
*[1] IMS-Bordeaux Université de Bordeaux, France;*
*[2] LFI Gottfried Wilhelm Leibniz Universität Hannover, Germany*

Embedding passives in PCB permit to gain in integration density, while enhancing electromagnetic compatibility performances. The choice of the dielectric is a fundamental for large frequency band stability in embedded capacitor values. However, these materials are prone to water absorption, which can lead to functional parameter degradations and additional stresses at the interfaces. This paper presents experimental capacitors embedded in FR-4, and finite elements simulations of moisture absorption with different dielectrics. Technological choice, as well as qualification procedure can be improved thanks to the simulation results.

Wed-C-15:50
**High Temperature Reliability of Electrically Conductive Adhesive Attached Temperature Sensors on Flexible Polyimide Substrates**
*Sanna Lahokallio, Janne Kiilunen, Laura Frisk*
*Tampere University of Technology, Finland*

The attachment and packaging of temperature sensors may be challenging due to their structure and materials. Sensing requires a structure which is open to the environment and the materials often differ from those used in silicon-based electronics. Thus, traditional attachment techniques and materials such as soldering may be inappropriate. Polymer-based electrically conductive adhesives (ECA) provide an alternative. The operating environment of a sensor may, however, be very demanding which may be problematic for polymer ECAs. Very little research is available on the use of ECAs in challenging conditions, thus restricting their use in many applications. In this study the behaviour of temperature sensors attached with ECAs onto flexible polyimide substrates was tested in thermal storage tests at 200°C. More than 1,000 hours of testing without failures was conducted on the ECA sensor structures. Good high temperature reliability therefore seems to be possible with ECA flip chip structure. However, the PI substrate was observed to be critical for reliability. An adhesive layer used in the PI substrate reacted at the test temperature. Consequently, severe oxidation of the copper pads and reaction with other materials was seen to destroy the interconnection and cause failures.

Wed-C-16:10
**A Study on Electrochemical effects in external Capacitor Packages**
*Harald Preu, Jochen Feilmeier, Markus Lang, Norbert Soellner, Jürgen Walter, Walter Mack*
*Infineon Technologies AG, Germany*

Semiconductor device are often driven in combination with external capacitors to improve the EMI (= electromagnetic interference) performance. Several package types exist where a capacitor is attached to the IC in an external moulding compound package. In many applications, the final product module is exposed to a harsh environment with variable temperatures and in combination with increased humidity and ionic contaminations. These conditions are a challenge for the reliability of the device, especially if moisture and ions are able to penetrate the package and initiate the formation of conductive paths.
This paper presents examples of the analysis of modules which were tested in applications together with reliability experiments with the purpose to understand the respective failure modes. Appropriate sample preparation, sensitive analytical methods like micro-x-ray fluorescence spectroscopy (µXRF), ToF-SIMS, SEM/EDX, x-ray-microscopy as well as micro computed x-ray-tomography (µCT) have been applied to identify the root causes of the electrical failures.
As a main conclusion of these investigations, we found that electrolytes can easily penetrate the typically by module manufacturers used thermoplastic overmold materials. This can lead to either reversible electrical failures which can be eliminated by drying or irreversible electrical failures because of material migration. The actual failure mode depends on mechanical and climate conditions inside the module which could not be simulated up to now under laboratory but only under application conditions.

## Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics

Thu-A-08:30-**Invited**
**Performance and Reliability Trade-Offs for High-K RRAM**
*Nagarajan Raghavan*

*Singapore University of Technology and Design, Singapore*
Resistive random access memories (RRAM) have shown tremendous potential in replacing Flash technology for future non-volatile data storage device applications in just about a couple of years from now. Although RRAM has various advantages in terms of simple design, high density integration and CMOS compatible process flow, it has its own intrinsic constraints in terms of variability and reliability, just as is the case for any other technology. While performance and reliability are both key metrics for any new product or technology design initiative, the critical aspect to investigate is the trade-off involved in improving them, as the measures implemented to boost performance do not necessarily have a positive impact on its reliability (lifetime). Optimization of the RRAM design for commercial applications requires a clear understanding and acknowledgment of these performance – reliability trade-offs. This study presents a qualitative perspective to identifying and understanding these trade-offs and probing the various sources of variability in high-κ RRAM.

Thu-A-09:10
**Optimization of inter-gate-dielectrics in hybrid float gate devices to reduce window instability during memory operations**
*Baojun Tang[1], Weidong Zhang[2], Laurent Breuil[1], Colin Robinson[2], Yunqi Wang[3], Maria Toledano-Luque[1], Geert Van den Bosch[1], Jianfu Zhang[2], Jan Van Houdt[1]*
*[1] IMEC, Belgium; [2] Liverpool John Moores University, United Kingdom; [3] University of Oxford, United Kingdom*

High-k dielectric stacks have been used in the 20 nm generation of floating gate (FG) flash memory cells. However, electron trapping in high-k materials remains a major concern for further development of FG technology. The hybrid FG (HFG) device with high-k inter-gate-dielectric (IGD) is a promising candidate with advantages of larger windows and less cell-to-cell interference, in which the poly floating gate is replaced by an n-poly/p-metal bi-layer structure. In this paper, to continue our previous work, the window instability in HFG with engineered IGD stacks during memory operations has been extensively studied. The results show that the HFG cell with the HAH (HaH) IGD structure provides not only the largest window but also the least instability, making it a suitable candidate beyond the 1x nm flash technology node.

Thu-A-09:30
**Impact of endurance degradation on the programming efficiency and the energy consumption of NOR Flash memories**
*Vincenzo Della Marca, Jeremy Postel-Pellerin, Guillaume Just, Pierre Canet, Jean-Luc Ogier*
*Aix-Marseille University, France*

In this paper the impact of the endurance degradation on the programming window and the energy consumption of Flash floating gate memories is investigated. Using a new technique of measurement we characterized the evolution of dynamic drain current during the channel hot electron injection in the course of cycling. We define the programming efficiency as a new figure of merit and we demonstrate why this decreases along the endu-

rance experiments. Moreover we demonstrated that the efficiency optimization varies with the cell degradation. Finally, our experimental protocol enables the understanding of the role of defects generation on the programming efficiency of NOR Flash memories.

Thu-A-09:50
**Variability Model for Forming Process in Oxygen Vacancy Modulated High-κ based Resistive Switching Memory Devices**
*Nagarajan Raghavan[1], Michel Bosman[2], Daniel Frey[3], Kin Leong Pey[1]*
*[1] Singapore University of Technology and Design, Singapore; [2] A*STAR Institute of Materials Research and Engineering, Singapore; [3] Massachusetts Institute of Technology, United States*

Forming is one of the key phenomenon that governs the subsequent switchability in high-κ based resistive random access memory (RRAM) devices. The variability of subsequent switching events, shape and size of filament, reliability of the non-volatile memory device in terms of endurance and retention, ultra-low power operation of the memory array all depend on the forming process in one way or the other. As a result, controllability of forming and reduction of the forming voltage is an important design activity in the RRAM technology development process. In this study, we shall analyze the various factors that affect the forming distribution from a simulation perspective using the Kinetic Monte Carlo (KMC) based formulation of the vacancy defect evolution process in the dielectric. The impact of high-κ microstructure (grain boundaries), metal-oxide interface roughness, deposition process induced defect distribution as well as role of multi-layer dielectric films on the forming time and spread will be investigated in detail. The results of the study provide guidelines to further reliability design initiatives in tightening the forming distribution.

Thu-A-10:50
**Novel 3D back-to-back diodes ESD protection**
*Bertrand Courivaud[1], Nicolas Nolhier[1], Gilles Ferru[2], Marise Bafleur[1], Fabrice Caignet[1]*
*[1] LAAS-CNRS, France; [2] IPDIA, France*

A 3D technology is used to design ESD protection devices. These planar bidirectional components, based on back-to-back diodes, are dedicated to first stage, external ESD protection. The main trick consists in using deep trenches, usually employed to perform capacitors, to design 3D diode. These devices present an amazing behaviour when they are submitted at cumulative ESD stress. However there is a specific holes configuration that should improve cumulative ESD stress robustness.

Thu-A-11:10
**Particle Monte Carlo Modeling of Single-Event Transient Current and Charge Collection in Integrated Circuits**
*Jean-Luc Autran[1], Maximilien Glorieux[2], Daniela Munteanu[3], Sylvain Clerc[2], Gilles Gasiot[2], Philippe Roche[2]*
*[1] Aix-Marseille University, France; [2] STMicroelectronics, France; [3] CNRS, France*

This work describes a new computational approach for modelling the radiation-induced transient current and charge collection at circuit-level. Our methodology is based on a random-walk process that takes into account both diffusion and drift of radiation-induced minority carriers in a non-constant electric field both in space and time. The model has been successfully coupled with SPICE for circuit solving and feedback on the charge-collection process. It is illustrated here for a junction impacted by an ionizing particle and embedded in a CMOS inverter.

Thu-A-11:30
**Radiation Sensitivity of Junctionless Double-Gate 6T SRAM Cells Investigated by 3-D Numerical Simulation**
*Daniela Munteanu[1], Jean-Luc Autran[2]*
*[1] CNRS-IM2NP, France; [2] Aix-Marseille University, France*

The Junctionless Double-Gate (JL-DGFET) technology is potentially interesting for future ultra-scaled devices, due to the simplified technological process and reduced leakage currents. In this work, we investigate, for the first time, the sensitivity to radiation of 6T SRAM cells built up of JL-DGFETs. A detailed comparison with SRAMs based on inversion-mode devices (FDSOI and IM-DGFET) is performed. Our simulations indicate that JL-DGFET SRAMs are naturally more immune to radiation than FDSOI SRAMs, but more sensitive than IM-DGFET SRAMs.

Thu-A-11:50
**Improving the ability of Bulk Built-In Current Sensors to detect Single Event Effects by using triple-well CMOS**
*Jean-Max Dutertre[1], Rodrigo Possamai Bastos[2], Olivier Potin[3], Marie-Lise Flottes[3], Bruno Rouzeyre[3], Giorgio Di Natale[3], Alexandre Sarafianos[4]*
*[1] Ecole des Mines de Saint-Etienne, France; [2] TIMA Lab , France; [3] LIRMM. Univ. Montpellier, France; [4] STMicroelectronics, France*

Bulk Built-In Current Sensors (BBICSs) were introduced to detect the anomalous transient currents induced in the bulk of integrated circuits when hit by ionizing particles. To date, the experimental testing of only one BBICS architecture was reported in the scientific bibliography. It reports an unexpected weakness in its ability to monitor NMOS transistors. Based on experimental measures, we propose an explanation of this weakness and also the use of triple-well CMOS to offset it. Further, we introduce a new BBICS architecture well suited for triple-well that offers high detection sensitivity and low area overhead.

Thu-A-12:10
**Assessment of Read Disturb Immunity in Conducting Bridge Memory Devices – A Thermodynamic Perspective**
*Nagarajan Raghavan[1], Michel Bosman[2], Kin Leong Pey[1]*
*[1] Singapore University of Technology and Design, Singapore; [2] A*STAR Institute of Materials Research and Engineering, Singapore*

Conducting bridge random access memory (CBRAM) devices operate on the basis of repeated nucleation and rupture of the metallic filament during the SET and RESET transitions. One of the critical reliability metrics for any non-volatile memory (NVM) is read disturb immunity, which refers to the ability of the device to keep the filament stable and unperturbed during the reading phase. While read disturb has been analyzed in detail for OxRAM which works based on the principle of oxygen vacancy generation and oxygen ion drift / diffusion, the susceptibility of CBRAM to read disturb events has not been analyzed in-depth. We make use of electrical test data, first order basic thermal model and fundamental thermodynamics to assess the stability of the CBRAM filament in both the high resistance state (HRS) as well as low resistance state (LRS). Our analysis reveals that the HRS retention is very good, while LRS retention can be quite poor for the CBRAM stack.

Thu-A-13:30
**Comparative Soft Error Evaluation of Logic Cells in FinFET Technology**
*Laurent Artola[1], Guillaume Hubert[1], Massimo Alioto[2]*
*[1]ONERA - The French Aerospace Lab, France;*
*[2]National University of Singapore, Singapore*

This work presents a comparative soft error evaluation of logic gates in bulk FinFET technology from 65- down to 32-nm technology generations. Single Event Transients induced by radiations are modeled with the MUSCA SEP3 tool, which explicitly accounts for the layout and the electrical properties of transistors. Good agreement between the calculated transient current, and TCAD mixed-mode simulations is demonstrated. This work allows for estimating the SER of such logic gates for ground applications, as well as for understanding the impact of voltage and drive strength through analysis of the sensitivity to soft errors.

Thu-A-13:50
**A Quantitative Study of Phosphorus Implantation Damage on the thick Gate Oxide of the 28nm Node**
*Xinggong Wan[1], Sandhya Chandrashekhar[1], Boris Bayha[2], Martin Trentzsch[2], Torben Balzer[2], Mahesh Siddabathula[2], Oliver Aubel[2]*
*[1]GLOBALFOUNDRIES, United States;*
*[2]GLOBALFOUNDRIES, Germany*

The tilted Phosphorous implantation has for a long time been adopted to form the lightly doped drain (LDD). For the first time, we report the implantation damage due to this on the thick gate oxide of the NMOSFET devices for 28nm technology. During the Time Dependent Dielectric Breakdown (TDDB) test, the breakdown time of the thick gate oxide of NMOSFET was found to be a function of implantation energy and dosage. In this work, an empirical model was established to characterize the implantation induced gate oxide lifetime reduction, which was correlated to the effective oxide thickness reduction. Our results showed that a careful implantation scheme needs to be chosen to balance the reliability requirements and the device performance for the scaled 28nm process and beyond.

Thu-A-14:10
**Mixture of Negative Bias Temperature Instability and Hot-Carrier driven Threshold Voltage Degradation of 130nm technology p-channel Transistors**
*Gunnar Andreas Rott[1], Karina Rott[1], Hans Reisinger[1], Wolfgang Gustin[1], Tibor Grasser[2]*
*[1]Infineon Technologies AG, Germany; [2]Institute for Microelectronics, Technische Universität Wien, Austria*

We present measurement results in form of threshold voltage drift plots, recovery traces and continuous capture emission time maps (CET maps) including Negative Bias Temperature Instability (NBTI) and Hot-Carrier driven Degradation (HCD). The measurements were performed on a 130nm MOS Transistor technology which is used for automotive and analog applications and has a nominal voltage of 1.5V. Devices of l = 100nm, w = 10µm have been stressed using a 2-dimensional parameter space of gate and drain voltage combinations at elevated temperature (125°C). The chosen stress conditions include the homogeneous (Vds = 0) and inhomogeneous (Vds << Vnom) NBTI case, the pure HCD (Vgs < Vnom) case as well as the mixture of NBTI and HCD. The results clearly show that for increasing Vds > Vnom NBTI recovery becomes less severe and mainly the permanent degradation due to HCD endures after the end of stress. Furthermore there is a drift minimum of NBTI observable for a specic Vds. Using CET maps it is quite evident that for high stress times the probability density of emission becomes very small whereas for shorter stress times there is a recoverable component notable.

Thu-A-14:30
**Predictive evaluation of electrical characteristics of sub-22nm FinFET technologies under device geometry variations**
*Cristina Meinhardt, Alexandra Lackmann Zimpeck, Ricardo Reis UFRGS, Brazil*

This work evaluates the impact on ION and IOFF currents of variations in process parameters for a set of predictive FinFET technologies from 20nm to 7nm. The main contribution of the present study is to identify relevant behavioural standards with respect to the use of FinFET technology in digital designs. It is no longer enough to focus only on the threshold voltage fluctuations in the development of projects and EDA tools considering the FinFET technology. It is necessary that EDA tools and designers evaluate all electrical characteristics.

## Reliability & Failure Mechanisms of Wide Bandgap Devices

Thu-B-08:30
**Single Pulse Avalanche Robustness and Repetitive Stress Ageing of SiC power MOSFETs**
*Asad Fayyaz[1], Li Yang[1], Michele Riccio[2], Alberto Castellazzi[1], Andrea Irace[2]*
*[1]University of Nottingham, United Kingdom; [2]University of Naples Federico II, Italy*

This paper presents an extensive electro-thermal characterisation of latest generation SiCPower MOSFETs under unclamped inductive switching conditions. Tests are carried out to thoroughly understand the single pulse avalanche ruggedness limits of commercially SiC MOSFETs and assess their aging under repetitive stress conditions. Both a functional and a structural characterisation of the transistors is presented, with the aim of informing future device technology development for robust and reliable power system development.

Thu-B-08:50
**Effect of gate trench fabrication technology on reliability of AlGaN/GaN heterojunction field effect transistors**
*Sergey Shevchenko, Matthias Schulz, Eldad Bahat-Treidel, Wilfred John, Stephan Freyer, Paul Kurpas, Hans-Joachim Würfl Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Germany*

A comparison of reliability by means of mean-time-to-failure (MTTF) determined from three-temperature accelerated life time tests for two groups of AlGaN/GaN hetero-junction field effect transistors is presented. The two groups differ by gate trench fabrication technology, namely by RF bias and power levels used for the reactive ion etching of gate trenches in a SiNx layer. The extrapolated MTTF at Tchannel = 150 °C was found to be ~2.6e8 h and ~2.6e5 h for transistors with gate trenches etched using RF power/bias 30 W/100 V and 15 W/30 V, respectively. The experimental results are explained based on the outcomes of simulations performed using Silvaco-“Atlas” 2D semiconductor device simulator. The simulations revealed higher electric field at the corner of the gate on a drain side and increased electron concentration in the vicinity of gate for the group of transistors processed with lowered RF power/bias. We conclude that the electric field and amount of electrons stipulated reliability degradation.

Thu-B-09:10
**Physical Origin of Current Collapse in Au-free AlGaN/GaN Schottky Barrier Diode**
*Jie Hu, Steve Stoffels, Silvia Lenci, Nicolò Ronchi, Rafael Venegas, Shuzhen You, Benoit Bakeroot, Guido Groeseneken, Stefaan Decoutere*
*IMEC, Belgium*

Dynamic characterization (Pulsed I-V) on Au-free AlGaN/GaN Schottky Barrier Diodes (SBDs) has been performed to evaluate the impact of a negative quiescent bias on the forward characteristic. Results show an increase of on-resistance when more negative quiescent biases are applied, and a sudden current collapse phenomenon when the quiescent bias exceeds -175 V. Furthermore, the measurements show a common signature: the total current collapse is the result of the trapping phenomena occurring around the Schottky contact corner. In this paper, a TCAD model with two discrete donor states has been defined, to aim in the understanding of the role of surface donor states and explaining the observed behavior of AlGaN/GaN SBDs from this dynamic measurement. We propose that trapping at deep energy levels, existing at the Si3N4/AlGaN interface, is responsible for the gradual current reduction observed for negative quiescent biases up to Anode-to-Cathode voltage (VAC) of -175 V. The electron filling of the shallower traps with high density at energy level located 0.3 eV below the conduction band starts at higher reverse bias, resulting in a strong Fermi-level pinning, which can be the cause of sudden current collapse.

Thu-B-09:30
**Thermal damage in SiC Schottky diodes induced by SE heavy ions**
*Carmine Abbate[1], Giovanni Busatto[1], Paolo Cova[2], Nicola Delmonte[2], Francesco Giuliani[2], Francesco Iannuzzo[1], Annunziata Sanseverino[1], Francesco Velardi[1]*
*[1]DIEI - University of Cassino and Southern Lazio, Italy;*
*[2]DII - University of Parma, Italy;*

The failure of SiC Schottky diodes due to the impact of high energy heavy ions is investigated by means of electro-thermal and thermal finite element simulations. In particular, 3D ATLAS simulation of a small portion of the diode structure is used for computing the dissipated power density which is subsequently used as input for the thermal COMSOL simulation of the complete system including chip and packaging. Results show that, as a consequence of the ion penetrating through the device, the temperature at the Schottky barrier becomes bigger than the SiC melting point for a time large enough to cause permanent damages to the SiC lattice. Simulation results are in good agreement with experiments presented in the literature.

Thu-B-09:50
**Temperature effects on the ruggedness of SiC Schottky Diodes under surge current**
*Javier León[1], Xavier Perpiñà[1], Viorel Banu[1], Josep Montserrat[1], Maxime Berthou[2], Miquel Vellvehi[1], Philippe Godignon[1], Xavier Jordà[1]*
*[1]IMB-CNM (CSIC), Spain; [2] Insa-Lyon, France*

This work analyzes the effects of temperature on the destruction of 1.2 kV 10A silicon carbide (SiC) tungsten-based Schottky Barrier diodes (W-SBD's) under surge current tests. First, W-SBD's were aged and tested up to failure under surge current pulses, showing no ageing at 40 A amplitudes and a surge current capability of 64 A and 59 A when they are tested at room temperature (RT) and 200ºC, respectively. Then, they were inspected by IR Lock in thermography and Small Signal Modulation for Thermal Analysis (SIMTA) technique, all they showing physical failure signatures at the active area periphery. Scanning Electron Microscope inspections after Focused Ion Beam millings at these locations revealed that metal degradation due to field stopper bipolar activation was the failure mechanism. At RT, the samples showed lighter degradation (electromigration and thermomigration, contact reconstruction), while at 200ºC, the metal contact was also sputtered off at the periphery. This correlates with the peripheral bipolar current density enhancement (bipolar activation voltage reduction) with temperature. These results are extensible to Junction Barrier Schottky diodes, as they present the same structure leading them to fail: Schottky and bipolar diodes parallel connected. Considering this, new solutions were proposed to enhance the W-SBD's ruggedness under overloading conditions.

Thu-B-10:50
**Proton induced trapping effect on space compatible GaN HEMTs**
*Antonio Stocco[1], Simone Gerardin[1], Davide Bisi[1], Stefano Dalcanale[1], Fabiana Rampazzo[1], Matteo Meneghini[1], Gaudenzio Meneghesso[1], Jan Grünenpütt[2], Benoit Lambert[3], Hervé Blanck[2], Enrico Zanoni[4]*
*[1]University of Padova, Italy; [2] United Monolithic Semiconductors, Germany; [3] United Monolithic Semiconductors, France;*
*[4]DEI-UNIPD, Italy*

In order to assess the space compatibility of GaN-HEMT technology, radiation hardness tests are an essential requirement. In this field, Gallium Nitride exhibits excellent robustness with respect to radiation and GaN-based devices are providing very promising results for most of the typical space configurations. Nevertheless, in presence of high total ionizing dose or of very high fluence levels, displacement damage takes place reducing the device performances from the static to the dynamic point of view. This paper shows how the combination of radiation hardness tests and the improvement of deep level analysis allows to quantify the DC and pulsed performance decrease induced by proton irradiation tests on a technology designed for the space applications, highlighting some signatures useful for an early detection of the displacement damage. Results provide a consistent demonstration of (i) threshold voltage positive shift and (ii) trapping effect enhancement correlated with the proton irradiation fluences.

Thu-B-11:10
**Analysis of an ESD failure mechanism on a SiC MESFET**
*Tanguy Phulpin[1], Karine Isoird[1], David Tremouilles[1], Dominique Tournier[2], Philippe Godignon[3]*
*[1] LAAS-CNRS, France; [2] ampere-lab, France; [3] CNM, Spain*

Efficient energy management become more and more crucial with increasing energy resource scarcity. Power electronic will play a major role in this field and thus require innovations like using wide band gap semiconductor to build power devices. SiC, GaN, diamond based device are currently more or less mature and will sooner or later require investigations on their reliability to allow their wide adoption. In this work we investigate on a SiC-MESFET ElectroStatic-Discharge (ESD) robustness. Surprisingly the ESD robustness is rather low and found to be related to both current non-uniformity and a quite unexpected parasitic NPN bipolar transistor triggering. The outcome of this study allows to propose a simple solution to improve ESD robustness of such devices.

Thu-B-11:30
**Traps localization and analysis in GaN HEMTs**
*Alessandro Chini[1], Fabio Soci[1], Gaudenzio Meneghesso[2], Matteo Meneghini[2], Enrico Zanoni[2]*
*[1] University of Modena and Reggio Emilia, Italy; [2] University of Padova, Italy*

A simple experimental technique aimed at the spatial localization of the dominant trap states involved in drain current dispersion in GaN HEMTs will be presented. By analyzing the dependence of current dispersion from the gate voltage base-line (VGbl) used in double pulse I-V measurements it is possible to observe a different trend of said dispersion when caused by buffer or barrier/surface traps. Devices whose dynamic characteristics are mainly affected by buffer traps are showing the largest dispersion when VGbl approaches the device threshold voltage (VTH) while a reduction in dispersion is observed when VGbl is lowered below VTH. On the other hand, when dynamic characteristics are mainly affected by barrier/surface traps, the opposite trend is observed, i.e. dispersion increases when VGbl is lowered below VTH. Numerical simulations supporting the proposed measurement technique and traps characterization in Fe-doped buffer devices will also be presented.

Thu-B-11:50
**Degradation analysis and current collapse imaging in AlGaN/GaN HEMT by electric field induced optical second harmonic generation measurement**
*Takashi Katsuno[1], Takaaki Manaka[2], Tsuyosihi Ishikawa[1], Hiroyuki Ueda[1], Tsutomu Uesugi[1], Mitsumasa Iwamoto[2]*
*[1] Toyota Central R&D Labs., Inc., Japan; [2] Tokyo Institute of Technology, Japan*

By using electric-field-induced optical second-harmonic generation (EFISHG) measurement, we analyzed degradation of AlGaN/GaN high electron mobility transistor (HEMT) devices, and imaged the current collapse. Strong second-harmonic (SH) signals activated at the gate edge with small shaped-feature traces under high drain stress voltage (300 V) application identified the degradation of the HEMT devices. The EFISHG also imaged trapped carriers at the on-state of the device, which lead to the current collapse. Immediately after (e.g. 1 us) the completion of drain-stress voltage application in the off-state, the SH signals appeared at the gate side of the drain electrode. This signal location well supports the well-known virtual gate model of current collapse.

## Reliability & Failure Mechanisms of Photonic and Special Devices

Thu-C-08:30-**Invited**
**MEMS Reliability – Current Status and Challenges**
*Mervi Paulasto-Kröckel, Jue Li*
*University Aalto, Finland*

With the rapid MEMS market growth, MEMS reliability has become ever more important especially in automotive, aerospace and medical applications where high reliability performance under harsh field conditions is expected. MEMS reliability needs to be considered at the early design phases of MEMS elements, electronics, packaging, and microfabrication processes. Malfunctions or failures of MEMS devices are not limited to the failures of MEMS elements such as stiction, fracture, friction and wear. There are critical reliability challenges arising from 3D or 2.5D system integration and packaging of MEMS devices. Key integration technologies like silicon-on-insulator (SOI), through silicon via (TSV), through glass via (TGV), and hermetic bonding have a significant influence on MEMS reliability. The reliability is also highly affected by the selection of materials and microfabrication techniques since most of the failures are located at the interfaces and interconnections where materials' microstructure plays an essential role.
In regard to reliability testing and failure analysis, there is a lack of testing standards for MEMS devices. New test vehicles, health monitoring systems, microstructural analysis, and failure analysis techniques deserve to be highlighted in order to detect failures as well as distinguish typical failure mechanisms. In addition, MEMS reliability modeling is a challenging multiphysics and multiscale problem. Novel simulation tools for predicting microstructure evolution at microscale or mesoscale needs to be developed in order to give a better understanding of the microstructure related failure mechanisms.

Thu-C-09:00
**ESD on GaN-based LEDs: an analysis based on dynamic electroluminescence measurements and current waveforms**
*Matteo Dal Lago[1], Matteo Meneghini[1], Nicola Trivellin[2], Gaudenzio Meneghesso[1], Enrico Zanoni[1], Marco Barbato[1], Carlo De Santi[1]*
*[1] University of Padova, Italy; [2] LightCube SRL, Italy*

This work presents an extensive study on the effects of Electrostatic Discharges (ESD) on state-of-the-art GaN based LEDs, based on optical and electrical measurements carried out during the ESD events. ESD events were simulated through a Transmission Line Pulser (TLP) which generates voltage pulses with a duration of 100ns and increasing amplitude: during each pulse, spatially-resolved electroluminescence measurements were carried out through an high speed EMCCD camera. These measurements allowed to identify the chip region where the discharge is localized and the change in the damaged area induced by consecutive ESD events. Also the current and voltage waveforms at the LED terminal were monitored during the tests; this analysis provided important information about modifications the impedance of the devices. The analysis was carried out on different type commercially available low-power GaN-based LEDs with several differences in the manufacturing technology. Thanks to these tests we have identified two different failure behaviours during a destructive ESD event, clearly related to the different defects in the semiconductor lattice and to structure of the chip.

Thu-C-09:20
**Temperature dependent optoelectronic properties of a non-intentionally created cleaved-coupled-cavity laser**
*Heinz-Christoph Neitzert[1], Giovanni Landi[2]*
*[1] Salerno University, Italy; [2] Fernuniversitaet Hagen, Germany*

A 1300 nm InGaAsP laser diode, degraded after the application of high voltage ESD pulses in forward direction, showed after degradation a strong longitudinal mode suppression, resulting in a single mode emission spectrum identical to the one of a cleaved-coupled-cavity laser. The room temperature threshold current after ESD induced degradation increased by about 50 % and the differential quantum efficiency dropped substantially. However, even after degradation in a wide temperature range stable single mode laser operation been achieved.

Thu-C-09:40
**Thermally-activated degradation of InGaN-based laser diodes: effect on threshold current and forward voltage**
*Carlo De Santi[1], Matteo Meneghini[2], Michael Marioli[2], Matteo Buffolo[2], Nicola Trivellin[3], T. Weig[4], K. Holc[4], K. Kohler[4], J. Wagner[4], U. T. Schwarz[4], Gaudenzio Meneghesso[2], Enrico Zanoni[2]*
*[1] Università degli Studi di Padova - Department of Information Engineering, Italy; [2] University of Padova, Italy;*
*[3] LightCube SRL, Italy; [4] Fraunhofer Institute for Applied Solid State Physics IAF, Germany*

This paper presents a study of the effects of high temperature stress on the electro-optical characteristics of violet InGaN-based laser diodes. The results indicate that: (i) when submitted to constant current stress (with relatively high junction temperatures), devices show a significant increase in threshold current (Ith), related to the increase in non-radiative recombination; micro-cathodoluminescence measurements indicate that the area affected by degradation is wider than the ridge; (ii) the results of purely-thermal stress test indicate that the exposure to high temperature may induce an increase in threshold current; (iii) during the first part of the stress, this mechanism is well correlated with the variation of the forward voltage, suggesting a degradation in the properties (conductivity, acceptor doping) of the p-type material; for longer stress times, a further Ith increase is detected, with a linear dependence on time.

Thu-C-10:00
**FIB-induced electro-optical alterations in a DFB InP laser diode**
*Giovanna Mura, Massimo Vanzi, Giulia Marcello*
*DIEE University of Cagliari - Italy, Italy*

A recent experiment used FIB to induce local modification in a single-mode edge emitting laser operating at 1310 nm, and led to a method for estimating gain parameters. In this experiment, the final FIB modification introduced large variation in electrical characteristics that were not analysed in detail, and even seemed to contradict the basic laser model that the experiment itself aimed to confirm. This paper focuses on this puzzling point, and solves it with a circuital hypothesis, a circuit simulation and a direct inspection by XEBIC.

Thu-C-10:50
**UV LEDs reliability tests for fluoro-sensing sensor application**
*F. Jose Arques-Orobon[1], Neftali Nuñez[2], Manuel Vazquez[2], Vicente González-Posadas[1]*
*[1] Technical University of Madrid, Spain;*
*[2] Instituto de Energía Solar-Technical University of Madrid, Spain*

The use of UV HB-LEDs for fluoro-sensing applications, as detection of substances in water is proposed for replace previous light sources. Developing devices to continuous environmental analysis requires that the used light sources must be robust, economic, and capable to operate correctly for long periods of time during 24h/day. UV HB-LEDs have improvement over old light sources but need an analysis of reliability for this type of applications. In this paper a reliability analysis of two types of new commercial 3W UV HB-LEDs has been developed, in two different working conditions: continuous and cycled working of 1 minute 30sON/30sOFF. Two sets of eleven LEDs at three accelerated temperature are tested. After 1500h of test at 60ºC, 75ºC and 90ºC, we have not observed catastrophic failures, only LEDs luminosity degradation. The degradation is larger for LEDs working at continuous current than LEDs working at cycled current in all tests

Thu-C-11:10
**A study of deposition conditions on charging properties of PECVD silicon nitride films for MEMS capacitive switches**
*Matroni Koutsoureli, Loukas Michalas, Anestis Gantis, George Papaioannou*
*University of Athens, Greece*

The present paper aims to provide a better insight to the electrical characteristics of silicon nitride films that have been deposited with PECVD method under different conditions. The effect of film thickness, substrate temperature and the frequency that produces the plasma in PECVD method on the dielectric charging phenomenon in silicon nitride films has been investigated with the aid of Thermally Stimulated Depolarization Currents (TSDC) and Kelvin Probe (KP) techniques. The results indicate that the decrease of film thickness and substrate temperature as well as the deposition at high frequency plasma (13.56 MHz) seems to produce silicon nitride films that are less prone to dielectric charging and thus better candidates for MEMS capacitive switches.

Thu-C-11:30
**Automated defect analysis in solar cells using EBIC**
*Grigore Moldovan[1], Shark Lotharukpong[2], Peter Wilshaw[2]*
*[1]Oxford Instruments NanoAnalysis, United Kingdom;*
*[2]University of Oxford, United Kingdom*

Electron Beam Induced Current (EBIC) characterisation is unique in its ability to provide quantitative high-resolution imaging of electrical defects in solar cells. In particular, EBIC makes it possible to image electrical activity of single dislocations in a Focussed Ion Beam (FIB) Scanning Electron Microscope (SEM), to cut and lift-out a micro-specimen containing a particular dislocation, and then transfer for further structural or chemical analysis. As typical solar cell material presents a complex array of defects, it is important to observe statistical variations within a sample and select the key sites for analysis. This paper describes a method for automated defect identification and characterisation, and shows an application to mc-Si solar cells wafers selected from different heights along the manufactured ingot. Information presented here includes the experimental setup for data acquisition, the basic algorithms used for identification and extraction of dislocation contrast. Analysis on solar cell wafers show the EBIC contrast of dislocations to decrease from 0.12 at the bottom of the ingot to 0.08 at the top of the ingot.

Thu-C-11:50
**Conduction Instability of Amorphous InGaZnO Thin-Film Transistors under Constant Drain Current Stress**
*Jung Han Kang, Edward Namkyu Cho, Ilgu Yun*
*Yonsei University, Korea*

Conduction characteristics of amorphous InGaZnO thin-film transistors were investigated by applying constant drain current with gate bias (VGS) modulation. Constant drain current in the off-current (Ioff) level from the transfer characteristic was applied to the drain electrode and the measured drain voltage with the gate bias sweep. The normalized channel conductance (Gd) characteristics were extracted from transfer characteristics and the gate bias modulated drain voltage characteristics with constant drain current stress were compared with the characteristics. The drain voltage induced by the constant drain current stress showed simultaneous transition from off-state with generation current dominant region with increasing drain bias (VDS) to the turn-on state. The high electric field at the drain electrode edge was observed at the threshold voltage (VTH), which can affect the instability characteristics of TFTs.

# Abstracts - Poster Presentations

## Quality and Reliability Assessment – Techniques and Methods for Devices and Systems

Tue-Expo-17:30-P01
**Prognostic Methodology for Remaining Useful Life Estimation of Retention Loss in Nanoscale Resistive Switching Memory**
*Nagarajan Raghavan[1], Daniel Frey[2], Kin Leong Pey[1]*
*[1] Singapore University of Technology and Design, Singapore; [2] Massachusetts Institute of Technology, United States*

Noise is a key indicator of the physical phenomenon underlying device operation, defect density and degradation trends. The analysis of noise in the frequency domain and the exponent (value of slope, α on logarithmic scale) of the power spectral density (PSD) can provide useful insight on the operating and failure mechanism of any device / system. We shall use this noise as a prognostic indicator to detect the instant at which the retention loss of a non-volatile memory device begins to occur. A qualitative perspective to prognostic management of a resistive random access memory (RRAM) device is provided in this work. Our method of detecting retention loss involves the unique observation of a slope of α = 3/2, which arises due to diffusion or ionic migration phenomenon.

Tue-Expo-17:30-P02
**Analytical stress characterization after different chip separation methods**
*Michael Fügl[1], Gunther Mackh[2], Elke Meissner[3], Lothar Frey[3]*
*[1] University Erlangen, Germany; [2] Infineon Technologies AG, Germany; [3] Fraunhofer IISB, Germany*

Synchrotron white beam X-ray topography (SXRT) and photoelastic stress measurements were used to characterize resulting strain fields after mechanical dicing and laser grooving of bare silicon wafers. The distribution and propagation of the strain fields can be characterized by the both methods. In contrast to mechanical dicing, the laser grooving process creates an inhomogeneous strain field. The influenced area is three times larger compared to mechanical dicing. The effect of the dicing procedure on the resulting mechanical fracture strength of the silicon chips was investigated by 3-point bending tests. The fracture strength of samples with an additional laser grooving process was significantly reduced under tensile load. The fracture pattern of the samples indicated that the strain field generated by the separation process causes initial points for µ-cracks propagation under mechanical load. This analysis can help to optimize dicing processes in order to attain a better reliability of chips with regard to process yields.

Tue-Expo-17:30-P03
**Monolithic integrable capacitive humidity sensing method for material characterization of dielectric thin films**
*Andreas Rückerl, Sophia Huppmann, Roland Zeisel, Simeon Katz*
*Osram Opto Semiconductors GmbH, Germany*

A monolithic integrable capacitive humidity sensing method to determine water vapor transmission rates of dielectric thin films is presented. The capacitive sensor, being used to detect transmission of water vapor, and the dielectric thin film to be tested can be processed subsequently with standard semiconductor technology. First measurements yield a reliable value of the well investigated dielectric PECVD-SiO2 (~ 1,6 $*10^{-2}$ +/- 0,7 $*10^{-2}$ g/($m^2$*d) for 330nm at 124°C). The working principle of the sensor, its drawbacks and improvements are discussed and put in reference with other methods.

Tue-Expo-17:30-P04
**Influence of temperature and dose rate on the degradation of BiCMOS operational amplifiers during total ionizing dose testing**
*Aleksandr S. Petrov, Konstantin I. Tapero, Viktor N. Ulimov*
*Research Institute of Scientific Instruments, Russian Federation*

The degradation of BiCMOS operational amplifiers TLV2451CP under the gamma-irradiation is studied for different dose rates and temperatures during irradiation. It is shown that studied devices are sensitive to both enhanced low dose rate sensitivity and time-dependent effects. Evidently the main reason for degradation of studied devices is build-up of the interface traps. Obtained results show possibility to develop an approach for total ionizing dose testing of BiCMOS devices considering low dose rate effects.

Tue-Expo-17:30-P05
**State of Health Online Estimation of Energy Storage System using Balancing Circuit**
*Shili Seima, Hijazi Alaa, Venet Pascal*
*Laboratoire AMPERE, France*

In this paper, an original technique for monitoring the state of health of energy storage systems is presented. The proposed approach is based on estimating the instantaneous internal parameter of each storage system element with a fast control of the balancing circuit present at the terminal of each element. The swift control of the balancing circuit could be applied at any storage system state (charge or discharge or rest) and have no incidence. This instantaneous internal parameter that is estimated is the Equivalent Series Resistance (ESR) which represents the ageing of the element. Then by the control of the balancing circuit, monitoring the ageing and then predicting the failure of the cell is possible.
The experiment is performed first using simulation with realistic storage system models in order to demonstrate and validate the effectiveness and the accuracy of the proposed technique. The experimental results presented covers storage system such us supercapacitor but could be also applied to battery.

Tue-Expo-17:30-P06
**RTN distribution comparison for bulk, FDSOI and FinFETs devices**
*Louis Gerrer[1], Salvatore Amoroso[1], Razaidi Hussin[2], Asen Asenov[3]*
*[1] University of Glasgow - Device Modelling Group, United Kingdom; [2] University of Malaysia, United Kingdom; [3] GoldStandard Simulations, United Kingdom*

In this paper we investigate the sensitivity of RTN noise spectra to Statistical Variability alone and in combination with variability in the traps properties, such as trap level and trap activation energy. By means of 3D statistical simulation, we demonstrate the latter to be mostly responsible for noise density spectra dispersion, due to its large impact on the RTN characteristic time. As a result FinFETs devices are shown to be slightly more sensitive to RTN than FDSOI devices. In comparison bulk MOSFETs are strongly disadvantaged by the statistical variability associated with high channel dopping.

Tue-Expo-17:30-P07
**Comparison of in-situ measurement techniques of the solder joint reliability under the thermo-mechanical stresses**
*Ning Duan*
*NXP Semiconductors, Netherlands*

Thermo Mechanical Cycle Lifetime (TMCL) test is a widely used test methodology for evaluating the reliability of solder joints in the microelectronics industry. The commonly used measurement techniques to monitor the solder joint failures during the TMCL test are either event detector or data logger. In this study, TMCL test has been carried out on the same devices in parallel with both measurement techniques. The pros and cons of both techniques are compared. It is observed that the solder joint reliability results on the investigated samples by both techniques are comparable. Event detector can catch short intermittent events, while the data logger is able to capture the details of the solder joint degradation process. In applications for which performance is dependent on the transmission of signals with a frequency of several hundred megahertz or more, the event detector technique shall be used. In such cases the data logger technique may overestimate product lifetime. On the other hand, for some applications where the performance is less susceptible to intermittent solder joint interconnect interruption but more to the increase of the solder joint resistance, the data logger shall be used. In such cases the event detector technique may underestimate product lifetime. In conclusion depending on the end application of the device, the most suitable technique can be selected.

Tue-Expo-17:30-P08
**Vacuum quality evaluation for microbolometer thermal imager sensors**
*Michael Elßner*
*Fraunhofer IMS, Germany*

This paper presents an innovative and effective method of measuring the internal vacuum quality of uncooled microbolometer thermal imager sensors where the bolometer sensor elements their self are used for the vacuum measurement. A feasible thermal calculation model using an extended Fourier's Law is shown that is integrated in thermal FEM simulations. Experimental results correlating with FEM simulations prove the feasibility of this method. A measuring range to pressures as low as 5*10-3 mbar was achieved that fully covers the needed range were the internal package pressure is leading to performance losses of the IRFPA. The vacuum quality evaluations supported by developed temperature stabilization show a high repetitive accuracy with a remaining mean failure of 0.2%. Without the need to integrate additional pressure sensors this method is cost and place saving as well as fast and highly accurate and can be used for stationary test systems as well as in mobile infrared camera systems.

Tue-Expo-17:30-P09
**Assessment of Mechanical Reliability of Surface Mounted Capacitor by an Accelerated Shear Fatigue Test Technique**
*Julien Magnien, Golta Khatibi*
*University of Vienna, Austria*

In this study mechanical reliability of Sn3.5Ag0.75Cusolder joints in SMD capacitors has been investigated. Tensile response of the solder joint with respect to thicknesses and aging conditions was studied by using Cu/SnAgCu/Cu model samples. Isothermal lifetime curves of SMD devices subjected to high strain vibrational loading was obtained by using an ultrasonic fatigue testing set-up. Mechanical reliability and the failure modes of solder joints in the SMD capacitors were found to be highly dependent on the microstructure of the solder and the intermetallic compound layer and the testing temperature. Testing at elevated temperature resulted in a clear change of crack path and fracture mode of the solder joints.

Tue-Expo-17:30-P10
**µ-Raman spectroscopy for stress analysis in high power silicon devices**
*Thierry Kociniewski[1], Jeff Moussodji[2], Zoubir Khatir[2]*
*[1] UVSQ - GEMaC / IFSTTAR - LTN, France;*
*[2] IFSTTAR - LTN, France*

Micron-scale characterization of strain is essential for physic failure studies in power devices. We report the use of Raman spectroscopy to measure mechanical stresses in silicon power devices with spatial resolutions down to 1 µm. µ-Raman measurements were realized on diode and Insulated Gate Bipolar Transistor (IGBT) cross section forward biased in order to map internal strain distributions. Temperature and stress contributions on Raman diffusion were deconvoluted fitting Full Width at Half Maximun (FWHM) and position of the stokes peak. For the first time, it was possible to quantify experimentally mechanical stress evolution during operation. These results give experimental data on thermo-mechanical coupling in power devices and could be able to support numerical models.

Tue-Expo-17:30-P11
**Compact model of magnetic tunnel junction with stochastic spin transfer torque switching for reliability analyses**
*You Wang[1], Yue Zhang[1], Erya Deng[1], Jacques-Olivier Klein[1], Lirida Alves De Barros Naviner[2], Weisheng Zhao[1]*
*[1] Univ. Paris-Sud, France; [2] Institut TELECOM, Télécom ParisTech, France*

Spin transfer torque magnetic tunnel junction (STT MTJ) is considered as a promising candidate for non-volatile memories thanks to its low power, high speed and easy integration with CMOS process. However, it has been demonstrated intrinsically stochastic. This phenomenon leads to the frequent occurrence of switching errors, which results in considerable reliability issues of hybrid CMOS/MTJ circuits. This paper proposes a compact model of MTJ with STT stochastic behavior, in which technical variations and temperature evaluation are properly integrated. Moreover, the phenomenon of dielectric breakdown of MgO barrier which determines the lifetime of MTJ is also taken into consideration. Its accurate performances allow a more realistic reliability analysis involving the influences of ambient environment and technical process.

## Reliability & Failure Mechanisms of Organic Devices

Tue-Expo-17:30-P12
**Air-stable, high current density, solution-processable, amorphous organic rectifying diodes (ORDs) for low-cost fabrication of flexible passive low frequency RFID tags.**
*Indranil Ronnie Bose[1], Kornelius Tetzner[2], Kathrin Borner[1], Karlheinz Bock[1]*
*[1] Fraunhofer EMFT, Germany; [2] TU Berlin, Germany*

We report on long-term air-stable ORDs on flexible substrates based on a solution deposited amorphous organic semiconductor (OSC) material, consisting of a co-polymer of arylamine and a fused aromatic species, reaching charge-carrier mobilities of μ=0.05 cm²/Vs (space charge limited current region) and current densities of up to 100 A/cm² at 10 V levels with rectification ratios of 104 operating in the 10 KHz range. The ORDs exhibit a high degree of air-stability without any passivation with extremely good reproducibility. ORDs were fabricated on polyethylene naphtalate (PEN) foils in a vertical sandwich structure with gold and aluminium as the injecting and blocking electrodes respectively via evaporation with the OSC spin-coated in between (Type1). To improve device performance of the ORDs, poly(ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) was microdispensed as a hole-injection layer (HIL) (Type2). The results for Type1-diodes show a really narrow spread of the diode characteristics, whereas for Type2 diodes the spread is slightly more but still acceptable. These ORDs prove themselves better than conventional Pentacene diodes both in terms of reliability / repeatability of the diode performance and air-stability without an encapsulation layer, and goes towards the enabling of a viable and reliable low-cost fabrication method of RFID-tags using organic semiconductors.

Tue-Expo-17:30-P13
**Reliability and operational stability of all-inkjet printed organic transistors**
*Henrique Leonel Gomes[1], Maria Do Carmo Medeiros[2], Fausta Loffredo[3], Riccardo. Miscioscia[3], Fulvia Villani[3], Carme Martínez-Domingo[4], Eloi Ramom[4], Enrico Sowade[5], Kalayan Mitra[5], Ian Mcculloch[6], Jordi Carrabina[4]*
*[1] Universidade do Algarve, Portugal; [2] Universidade de Coimbra, Portugal; [3] ENEA, Portici Research Center, Italy; [4] CAIAC, Universitat Autònoma de Barcelona, Spain; [5] Chemnitz University of Technology, Germany; [6] Department of Chemistry, Imperial College London, United Kingdom*

This work reports on the improved operational stability of inkjet printed transistors. The dielectric and the organic semiconductor as well as surface treatments were optimized to minimize the density of traps causing gate-bias stress and carrier injection limitations from the metal contacts. State-of-the-art all inkjet printed transistors using poly-4-vinylphenol as dielectric layer and FS0027, a formulation in tetralin based on a triarylamine semiconducting polymer were fabricated with a figure of merit for the operational stability (τo=105 s) [1] as good as the values reported for transistors processed using vacuum sublimed organic semiconductors. Electron trap density on the dielectric surface was primed using electro-optical measurements. Electrons photogenerated in the semiconductor region escape geminate recombination (under a appropriate bias) and drift to the semicondutor/dielectric interface where they neutralize deep-trapped holes. The fast trap neutralization process, allow us to measure the ideal transistor characteristics (trap-free transistors) and compare them with the behavior of transistors with the traps filled. Furthermore, the selective filling of traps provides a valuable tool to study how traps cause non-ideal transistor characteristics, namely non-linear transfer curves. The electrical characteristics of the transistors were also measured in a broad temperature range [120 -350 K]. It is show that the temperature dependence of the current for a trap-empty transistor shows an anomalous behavior and different form a trap-filled transistor. This work was carried out under the FP7 project Technology & Design Kits for Printed Electronics (TDK4PE).
[1] S. G. J. Mathijssen et. al. Advanced Materials, vol. 19 (2007) 2785.

## Failure Analysis

Tue-Expo-17:30-P14
**SEM-based nanoprobing on 32 and 28 nm CMOS devices – Challenges for Semiconductors Failure Analysis**
*Erik Paul*
*GLOBALFOUNDRIES, Germany*

This paper presents an effective device-level failure analysis (FA) method which uses a high-resolution low-kV Scanning Electron Microscope (SEM) in combination with an integrated state-of-the-art nanomanipulator to locate and characterize single defects in failing CMOS devices. The presented case studies utilize several FA-techniques in combination with SEM-based nanoprobing for nanometer node technologies and demonstrate how these methods are used to investigate the root cause of IC device failures. The methodology represents a highly-efficient physical failure analysis flow for 28nm and larger technology nodes.

Tue-Expo-17:30-P15
**Acoustic detection of micro-cracks in small electronic devices**
*Georg Michael Reuther, Reinhard Pufall, Michael Goroll*
*Infineon Technologies AG, Germany*

We demonstrate the feasibility of in-situ acoustic detection of micro-cracks in small electronic devices. Applying precisely controlled damage to test vehicles using a nanoindenter, we record brittle fracture of thin layers by means of an ultra-sound piezo sensor, which is able to detect micro-cracks in the moment they emerge. In particular, this method does not require further preparation effort that may induce additional stress to a sample or modify it physically, inhibiting unambiguous failure analysis. With regard to applicability and limitations, we put acoustic emission into context with other standard experimental procedures for crack characterization in micro-electronic structures.

Tue-Expo-17:30-P16
**High resolution imaging of dopant and depletion layer distributions in SiC power MOSFET using super-higher-order nonlinear dielectric microscopy**
*Norimichi Chinone[1], Takashi Nakamura[2], Yasuo Cho[1]*
*[1] Tohoku Univ., Japan; [2] ROHM Co., Ltd., Japan*

Evaluation techniques for semiconductor devices are keys for device development with low cost and short period. Especially, dopant and depletion layer distribution in device is critical for electrical property of the device and is needed to be evaluated. Super-higher-order nonlinear dielectric microscopy (SHO-SNDM) is one of the promising techniques for semiconductor device evaluation. We developed method for imaging detailed dopant distribution and depletion layer in semiconductor device using SHO-SNDM. As a demonstration, cross-section of a SiC power semiconductor device was measured by this method and detailed dopant distribution and depletion layer distribution were imaged.

Tue-Expo-17:30-P17
**Quantifying the Limits of Scanning Electron Microscopy for the Metrology of Critical Dimensions of Photoresist Structures in the Nanometer Range**
*Mauro Ciappa[1], Emre Ilguensatiroglu[1], Alexey Illarionov[2]*
*[1] ETH Zurich, Switzerland; [2] Integrated Systems Laboratory, ETH, Switzerland*

Statistical fluctuations of the critical dimensions in the Front-End-of-Line represent a challenge for the yield and reliability of CMOS technologies in the sub-22nm nodes. This implies the use of advanced characterization techniques with resolution capabilities in the sub-nanometer range. In this paper, the ability of scanning electron microscopy to achieve the required level of uncertainty is investigated by Monte Carlo simulation. Examples based on the model library approach are shown, which deal with the extraction of the critical dimensions in photoresist lines and contact holes with line edge roughness.

Tue-Expo-17:30-P18
**Scanning Spreading Resistance Microscopy for failure analysis of nLDMOS devices with decreased breakdown voltage**
*Stefan Doering[1], Ralf Rudolf[1], Martin Pinkert[1], Hagen Roetz[1], Catejan Wagner[1], Stefan Eckl[1], Marc Strasser[2], Andre Wachowiak[3], Thomas Mikolajick[4]*
*[1] Infineon Technologies Dresden GmbH, Germany; [2] Infineon Technologies AG, Germany; [3] NaMLab GmbH, Germany; [4] TU Dresden, Germany*

Scanning Spreading Resistance Microscopy (SSRM) is applied to investigate failing nLDMOS devices. The fail devices exhibit a lowered break down voltage (BVDSS) in the electrical tests. For the purpose of comparison, additionally two pass devices are visualized using SSRM. It is shown that the pass devices exhibit similar characteristics regarding the different doping areas, proving the comparability of the measurement results. In contrast, the fail device shows a degradation of the drift zone and significantly different spreading resistance values for the deep body. As simulation shows, the hypothesis of a missing drift zone implant alone explains the electrically observed lowered breakdown voltage. Based on the SSRM results a second hypothesis is proposed, based on an increased net doping of the deep body. This second hypothesis fits both, the electrical data and the observed SSRM results. SSRM enables the proving/disproving of different hypotheses causing the same electrical fail behaviour. In this work SSRM proves its applicability for implant related failure analysis cases.

Tue-Expo-17:30-P19
**Electromigration in Open TSVs**
*Wolfhard H. Zisser, Hajdin Ceric, Josef Weinbub, Siegfried Selberherr*
*Institute for Microelectronics, TU Wien, Austria*

Through silicon vias (TSVs) are the components in three-dimensional integrated circuits, which are responsible for the vertical connection inside the dies. In this work we present studies about the reliability of open TSVs against electromigration (EM). A two-step approach is followed. In the first step the stress development of a void free structure is analyzed by means of simulation to find the locations where voids due to stress are most probably nucleated. In the second step, voids are placed in the TSV and their evolution is traced including the increase of resistance. The resistance raises more than linear in time and shows an abrupt open circuit failure. These results are in good agreement with results of time accelerated electromigration tests.

Tue-Expo-17:30-P20
**Copper dendrites growth in LLT (Lead Lock Tape) embedded in QFP package: physical identification and characterization**
*Claudio Savoia[1], Giuseppe Giuga[1], Fabio Tormen[1], Luca Merlo[2]*
*[1] STMicrolectronics, Italy; [2] University of Milano, Italy*

A non-destructive method to identify copper dendrites in packaged devices has been developed using X rays 3D tomography. The method shows the dendrites grows in the lead locking tape glue layer A recipe has been developed to validate the 3D results, saving the defect evidence. It requires laser ablation to define the area under inspection, chemical etching and treatment by water and LLT plastic film removal to uncover the glue layer. Dendrites are better visible by dark field optical microscopy.

## Power Devices Reliability

Tue-Expo-17:30-P21
**Joining and package technology for 175°C Tj increasing reliability in automotive applications**
*Peter Dietrich*
*Fuji Electric Europe GmbH, Germany*

For the task of improving the reliability and robustness of power electronic semiconductor devices, the main focus is on packaging and joining technology. The improvement is made necessary by various applications which require higher active and passive temperature cycles capability. For example: Automotive applications require a minimum life time of 15 years, wind power 25 and traction applications, 30 to 40 years and longer. Furthermore, higher reliability is demanded of new semiconductor technology, because maximum junction temperatures will, sooner or later, exceed currently recognised limits. In the near future, silicon devices will reach a maximum junction temperature of up to 200°C. And the new wideband-gap devices have the potential to exceed even this limit. That's why a new package and joining technology is mandatory. There are new developments in the pipeline: For the die contact, planar wire technology and copper based bond wires can be expected in the long term. This new technology is based on new material science and PCB process techniques. As a robust joining method, sinter or diffusion solder will be in use soon. But on the semiconductor module level, further action can be taken now, or in the near future, to increase reliability significantly. This paper presents improvements, based on material science, which are already available and can be used now, or in the near future.

Tue-Expo-17:30-P22
**Overload Robust IGBT Design for SSCB Application**
*Ihsan Supono[1], Jesus Urresti[1], Alberto Castellazzi[1], David Flores[2]*
*[1] University of Nottingham, United Kingdom; [2] IMB-CNM, Spain*

This paper presents an optimized non-punch-through IGBT device design for use in solid-state circuit breaker applications. For this particular application, of steadily increasing relevance and interest, it is paramount to minimize the conduction losses without compromising voltage blocking capability, while ensuring adequate overcurrent turn-off and short-circuit withstand capability. Starting from a standard design for switching applications, the results presented show that the optimized device offers a reduction in conduction losses of 13%, without compromise on voltage blocking capability. An original design solution is implemented to further ensure short-circuit capability and overload turn-off at maximum ambient temperature and twice the nominal rated current.

Tue-Expo-17:30-P23
**Reliability enhancement by integrated liquid cooling in power IGBT modules for hybrid and electric vehicles**
*Yangang Wang, Steve Jones*
*Dynex Semiconductor ltd, United Kingdom*

IGBT modules in power-train system of hybrid and electric vehicles (HEV/EV) are working in harsh environment that requires very high reliability. In this work, reliability enhancement by integrated liquid cooling structure in HEV/EV IGBT module is investigated. The thermal resistance of junction to heat sink can be reduced more than 50% by direct liquid cooling as eliminating thermal grease layer, so both active and passive temperature swings decrease significantly which will enhance module reliability and lifetime. The lifetime of modules with conventional and integrated liquid cooling structures are estimated under mission of standard driving cycles, and we found that lifetime is prolonged obviously by direct cooling pin-fin base plate. In addition, the integrated liquid cooling IGBT module makes power system simple and reliable.

Tue-Expo-17:30-P24
**Robust snubber-less power converter design with soft-switching avalanche-rugged Si and SiC Power MOSFETs**
*Francesco Giuliani[1], Dipankar De[1], Nicola Delmonte[2], Alberto Castellazzi[1], Paolo Cova[2]*
*[1] University of Nottingham, United Kingdom; [2] University of Parma, Italy*

A number of harsh-environment high-reliability applications are undergoing substantial electrification. The converters operating in such systems need to be designed to meet both stringent performance and reliability requirements. Semiconductor devices are central elements of power converters and key enablers of performance and reliability. This paper focuses on a dc-dc converter for novel avionic applications and considers both new semiconductor technologies and the application of design techniques to ensure, at the same time, that robustness is maximised and stress levels minimised.

Tue-Expo-17:30-P25
**Solder void position and size effects on electro thermal behaviour of MOSFET transistors in forward bias conditions**
*Son-Ha Tran[1], Laurent Dupont[2], Zoubir Khatir[2]*
*[1] VeDeCoM, France; [2] IFSTTAR-LTN, France*

This research aims to enhance the understanding on position and size effects on the electro thermal behaviour of low voltage power MOSFET transistors in forward bias condition. The numerical simulations are based on a fractional design of experiments (DoE). The performance of a finite elements model is discussed by comparing thermal and electrical measurements to results of finite elements simulation on a module of free void and voided solder. The void in the model is afterwards parameterized on position and size, according to the fractional DoE of the study. The combined functions issued from the parametric simulations and the DoE show the main impact of void size on temperature of the device and on the surface temperature of the bonding wires. From the numerical viewpoint, the most impacting position of void depends highly on the void size. The redistribution of current density and temperature on MOSFET chip and bonding wires due to solder void is also observed. A future experimental study in respect to the same DoE is expected in prospect, in order to fulfil the complementarity for this approach.

Tue-Expo-17:30-P26
**Turn-off Instabilities in large area 600V IGBTs**
*Carmine Abbate[1], Francesco Iannuzzo[1], Giovanni Busatto[1], Annunziata Sanseverino[1], Francesco Velardi[1], Cesare Ronsisvalle[2], James Victory[2]*
*[1] University of Cassino and Southern Lazio, Italy; [2] Fairchild Semiconductor, Germany*

In this paper, an experimental study is proposed to investigate the failure effects in IGBT large-area devices due to hard gate driving strategies. Thanks to simulations, a large overcurrent is predicted in few cells and corresponds to a large spike in the gate voltage during collector voltage transient, which is able to trigger the device instability.
An interpretation of the phenomenon is given that attributes such spike to a strong current unbalancing on the large area device, leading itself to a latch-up failure.

Tue-Expo-17:30-P27
**Impact of active thermal management on power electronics design**
*Markus Andresen, Marco Liserre*
*Christian-Albrechts-University of Kiel, Germany*

Power electronic system design is typically constrained by the thermal limitation so by the overall losses and the peak current. To stay within the maximum current, reached only during transients, the system is typically overrated. Active thermal management is used to control the maximum temperature and the temperature swing to reduce failures that are mostly caused by them. In this paper it is proposed to use the active thermal management to reduce the switching losses or to move them to less stressed devices, during transients, such as a module can reach an higher current, without violating thermal constraints, and the need of overdesign can be reduced. Hence an optimal and cost effective design of power electronics system is achieved.

Tue-Expo-17:30-P28
**NBTI Degradation in STI-based LDMOSFETs**
*Yandong He, Ganggang Zhang, Xing Zhang*
*Institute of Microelectronics, Peking University, China*

NBTI degradation in STI-based LDMOSFETs has been investigated by multi-region DCIV spectroscopy(MR-DCIV), a non-destructive and sensitive method to probe the interface states on channel, accumulation and STI region. A unified MR-DCIV current model was proposed based on its independency to the forward bias and temperature. Under the same negative gate stress condition, MR-DCIV current degradation was compared for nLDMOSFET and pLDMOSFET. Much larger MR-DCIV current shift was observed at channel and accumulation region with thin gate oxide thickness, indicating interface states generation at related regions. Our results show that more significant degradation for multi-finger device was consistent with NBTI degradation mechanism. High voltage device design with thermal management consideration is of crucial importance to guaranteeing the device performance and reliability.

Tue-Expo-17:30-P29
**Description of Supercapacitor Performance Degradation Rate during Thermal Cycling Under Constant Voltage Ageing Test**
*Mohamed Ayadi[1], Olivier Briat[2], Richard Lallemand[3], Akram Eddahech[4], Ronan German[5], Gerard Coquery[3], Jean-Michel Vinassa[6]*
*[1] Ifsttar-IMS Laboratories, France; [2] Laboratoire IMS CNRS, France; [3] IFSTTAR Versailles Satory, France; [4] IMS Laboratory, France; [5] Université Lyon 1, France; [6] University of Bordeaux, France*

Great research effort is currently devoted towards enhancing performance and operating time of electrical vehicle (EV). Classic storage element in EV consists of accumulators, which allow a relatively high autonomy. However, the power capability of these devices can be considered as insufficient. Supercapacitors (SC) are a new promising storage system used in EV to minimize this lack thanks to their high power capability. One of the ageing cause for SCs for this application is the day/night cycling, that's why we study the impact of thermal cycling on SC performances in this paper. In this article, and in order to have a descriptive sample, impacts of three thermal cycling ageing test conditions are compared with obtained results coming from simple calendar ageing tests at constant temperature and voltage. The comparison is based on physics modelling parameters evolution in the Constant Phase Element (CPE) and Multi-Pore (MP) models. These parameters are calculated based on experimental measurements during calendar ageing tests up to 14000 h and 6000 h, 10000 h for thermal cycling tests. Finally, the study of modelling parameters highlights changes in the internal physical structure for both ageing tests.

## Chip-Package Interactions and 3D Reliability & Failure Mechanisms

Tue-Expo-17:30-P30
**Study of the UBM to copper interface robustness of solder bumps in flip chip packages**
*Joerg Dreybrodt, Yves Dupraz*
*EM Microelectronic Marin SA, Switzerland*

Shear tests on SnAg solder bumps were performed with a reduced height to the surface for a high shear force on the under bump metallurgy (UBM) to redistribution layer (RDL) copper interface. By this the failure mechanism of UBM-RDL delamination after stress tests simulating several assembly reflows could be reproduced. A design of experiment was done with corner wafers at worst case conditions for topography and interface clean. TEM cross sections confirmed nano scale carbon residues in the interface when reducing the clean efficiency. This results in a mechanically weakened interface with a present electrical contact. The shear test with reduced height is a more severe test beyond the JEDEC test to verify the bump robustness. This is important when existing bump technologies are used for flip chip package solutions with increased solder reflow requirements.

Tue-Expo-17:30-P31
**A study of through package vias in a glass interposer for multifunctional and miniaturized systems**
*Abderrahim El Amrani, Abdellah Benali, Mohsine Bouya, Mustapha Faqir*
*Université Internationale de Rabat, Morocco*

Glass interposer with through package vias is a promising 3D-IC packaging technology that is expected to be used widely in near future thanks to its numerous benefits. This technique is still developed in research laboratories because of its low yield compared to the Through Silicon Vias which is used in industrial scale. In this work, our progress regarding fabrication of the glass interposer with 3D vertical interconnects will be shown. In this study, samples are fabricated using different techniques; determine failures and defects that have effects on the interposer reliability and functionality. By reviewing the process we tried to eliminate or reduce these weaknesses. Then, we showed the results and discuss the physical and electrical differences between the samples fabricated with old and new processes.

Tue-Expo-17:30-P32
**Evaluation new Corner Stress Relief Structure Layout for high robust Metallization**
*Verena Hein[1], Kirsten Weide-Zaage[2], Joerg Kludt[2]*
*[1] X-FAB Semiconductor Foundries AG, Germany; [2] University Hannover, Germany*

For high robust metallization it is necessary to solve different problems related to migration mechanisms and thermo-mechanical stress in the material. Extended operating conditions and challenging assembling processes influence stress behaviour in chip corners. Typically the corner area of the chip is excluded for use. For higher stress load the forbidden area increases. But effort for demanding mission profiles of a product should not cumulate in increasing chip size. Corner stress relief structures lower the influence of high thermo-mechanical stress. This approach helps to better chip-package interaction. A high functional corner stress relief structure allows the customers a more efficient chip design. In this work a new corner stress relief structure layout is presented and a structure for evaluation the effectiveness of that layout for a thick metal process is shown.

Tue-Expo-17:30-P33
**Sn Whisker evaluation in 3D microbumped structures**
*George Vakanas[1], Joke De Messemaeker[2], Bjorn Vandecasteele[2], Geert Willems[2], Mark Ashworth[3], Geoffrey Wilcox[3], Ingrid De Wolf[2], David Schaubroek[2]*
*[1] Intel assignee to imec (3D), United States; [2] IMEC, Belgium; [3] Loughborough University, United Kingdom*

Sn whiskering remains a reliability concern in electronic applications. Despite research on growth mechanisms and mitigation strategies, no predictive theory is in place. Literature data are available for Cu/Sn-based films and coatings as well as for board-level and flip-chip solder bumps but data are scarce for scaled-down solder volumes. The current work investigates whiskers in isolated geometries for 3D solder-capped Cu microbumps with >2 orders of magnitude smaller solder volumes. To the best of the authors' knowledge, this is the first time Sn whisker growth is reported in isolated solder volumes (e.g. ~ 8mmicron side cube). Whiskers propensity was evaluated per JEDEC industrial specifications in 5/3.5mmicron thick Cu/Sn films and 15mmicron diameter electroplated solder-capped (Sn, SnAg, SnCu) Cu microbumps (as-plated vs. reflowed). Selected Sn whiskers and whisker-like features were analyzed and identified experimentally with SEM, EDX and FIB. First-order, what-if calculations are carried out to quantify trends of Sn whisker growth with further microbump scaling and impact of alternative microbump materials. Future research recommendations are outlined to mitigate manufacturing risks by controlling queue times between bumping and stacking.

## Reliability & Failure Mechanisms in Packages and Assembly

Tue-Expo-17:30-P34
**Thermal and Mechanical Effects of Voids within Flip Chip Soldering in LED Packages**
*Yang Liu[1], Stanley Y. Y. Leung[2], Jia Zhao[3], Cell K.Y. Wong[2], Cadmus A. Yuan[4], Guoqi Zhang[5], Fenglian Sun[1], Liangliang Luo[1]*
*[1] Harbin University of Science and Technology, China; [2] Beijing Research Centre, Delft University of Technology, China; [3] State Key Laboratory of Solid State Lighting, China; [4] Institute of Semiconductors, Chinese Academy of Sciences, China; [5] DIMES Center for SSL Technologies, Delft University of Technology, Netherlands*

This paper investigated the effect of void ratio in the solder layer upon the shear strength and thermal property of DA3547 packages by SAC soldering technology. X-ray observation and shear test revealed that the increase of solder paste volume would significantly decrease the ratio of voids in the solder layer and thus improved the shear strength of the packages. On the other hands, packages with lower void ratio showed lower junction temperature based on the results of IR test and Finite element simulation. However, the temperature difference due to the effect void ratio presented a dependent relationship with the input power. For the DA3547 packages studied in this research, voids show limited influence on the junction temperature under 50mA, the typical current recommended by Cree.

Tue-Expo-17:30-P35
**Influence of mobile ion in organic material used in semiconductor devices**
*Yik Yee Tan[1], Claudia Keller[2], Kok Seng Teo[1], Sivanyanam Rajamanickam[1]*
*[1] Infineon Technologies, Malaysia; [2] Infineon Technologies, Germany*

Kapton tape is often used for co-planarity of inner metal lead frame parts in the packaging of semiconductor components. It is made of organic material known as high temperature insulating tape. In this paper, the increment of leakage current in a packaged component that is caused by a Kapton tape was studied. The leakage measurement on Kapton tape was done using simple testing instruments such as source meter, micro prober and temperature controlled hot plate. The different leakage current characteristics were investigated on high temperature, test duration and length of the Kapton tape. According to the measured leakage current on various dependencies, it is suggested the leakage is due to mobile ion in Kapton tape. Various analysis techniques were able to identify the mobile ion was Sodium ions in the glue of the Kapton tape. Based on the observation, a model explaining the Sodium mobile ions failure mechanism in the Kapton tape was established. The deployment of leakage test can be applied to test incoming lead frame material. The test set up did not require expensive tester equipment and manufactured devices. It could also be transferred as new outgoing quality check mainly for lead frame suppliers.

Tue-Expo-17:30-P36
**A three-scale approach to the numerical simulation of metallic bonding for MEMS packaging**
*Alberto Corigliano[1], Aldo Ghisi[1], Stefano Mariani[1], Giorgio Allegato[2], Laura Oggioni[2]*
*[1] Politecnico di Milano, Italy; [2] STMicroelectronics, Italy*

In this work we present a numerical, multi-scale approach to estimate the strength of a wafer-to-wafer metallic thermo-compression bonding. Following a multi-scale, top-down approach, the mechanical problem is handled at three different length scales. Taking into account control variables such as temperature, overall applied force over the wafer and contact surface roughness, it is shown that the proposed approach is able to provide an estimate of the sealing properties, especially in terms of bonding strength.

Tue-Expo-17:30-P37
**Microstructure of Sn-1Ag-0.5Cu Solder Alloy Bearing Fe Under Salt Spray Test**
*Nor Ilyana Muhd Nordin[1], Suhana Mohd Said[1], Rahizar Ramli[1], Mohd Faizul Mohd Sabri[1], Nurulakmal Mohd Sharif[1], Nik Ahmad Fadzil Nik Mohd Arifin[2], Nik Nurul Syazana Ibrahim[2]*
*[1] University of Malaya, Malaysia; [2] MIMOS, Malaysia*

Understanding the behavior of lead-free solder alloys within a high humidity environment is a serious topic in the deployment of products in various electronics applications. The work reported herein investigates this specific impact on Sn-1.0Ag-0.5Cu-0.5Fe solder alloy. Specimens were treated with 5% NaCl salt spray. All specimens showed strong resistance to corrosion. Microstructural deformations after the test were analyzed using Scanning Electron Microscopy/Energy Dispersive X-Ray Spectroscopy (SEM/EDX). Concerns were at the localized corroded area, as this would cause significant degradation at the solder joints. The mechanisms leading to these disadvantageous results as well as the microstructural evolution and correlation with the intrinsic properties of the solder alloy are discussed.

Tue-Expo-17:30-P38
**Protective Coatings of Electronics under Harsh Thermal Shock**
*Juha Pippola, Tuomas Marttila, Laura Frisk*
*Tampere University of Technology, Finland*

Industrial electronics commonly encounter harsh environmental conditions during their operational life time. The most adverse conditions for the electronics are considered to be elevated temperature, temperature changes, humidity, and contaminants. To protect the electronics from such conditions protective casting and coating materials can be used. The variety of protective materials is wide. However, the knowledge of material behaviour in harsh environments and their effect on electronics reliability in industrial products has been studied only very little. Moreover, the changes in material parameters under various conditions are mainly unknown. In this paper the behaviour of the protective coating and casting materials are studied under thermal shock test. Conditions of the test used were relatively harsh with extreme temperatures of -40°C and +125°C. Temperature change time was approximately two minutes. Samples used in the study were commercial electronics devices designed for harsh conditions. The protective materials studied included silicone based conformal coating, polyurethane based casting material, and silicone based casting material. Moreover, comparison test without any protective materials was conducted. Results from the study show that conformal coating and polyurethane based casting material decreased the device times to failures. However, silicone based coating seemed to slightly increase the reliability of the devices.

Tue-Expo-17:30-P39
**Evaluating board level solder interconnects reliability using vibration test methods**
*Yang Liu, Fenglian Sun, Hongwu Zhang, Zhen Zhou*
*Harbin University of Science & Technology, China*

In this paper, three types of accelerated test methods based on vibration loading are conducted and compared for board level mechanical reliability evaluation. A high speed strain data acquisition system was built up to collected PCB response during swept sine vibration tests. The eigenfrequency is obtained with FFT (Fast Fourier Transform) of strain data of largest PCB vibration amplitude. The first method is fixed frequency sine vibration at eigenfrequency. The second method is swept sine vibration with narrow-band frequency. The third method is random vibration with narrow-band frequency. The PCB responds are collected and compared. The failure process was monitored and characterized. Results show that the vibrating amplitude is highly dependent upon the frequency ratio. Due to the variation of PCB eigenfrequency, the fixed frequency vibration may miss the largest amplitude loading. The other vibration method within a narrow-band frequency could eliminate the influence the boards' factors. And both swept sine and random vibration could produce large amplitude vibration of the board. The differences of these methods are the loading density and repetitions. The failure processes of the three types of test methods are similar. Four failure stages are found from collected failure data. Weibull plot results show the characteristic life of the solder interconnects are verified with loading repetition evaluation.

Tue-Expo-17:30-P40
**Reliability of adhesive joined thinned chips on flexible substrates under humid conditions**
*Laura Frisk[1], Kirsi Saarinen-Pulli[2]*
*[1] Tampere university of Technology, Finland; [2] Konecranes, Finland*

Thinned chips are an interesting option for reducing the thickness of an electronics package. In addition to the reduced size, thinned chips are flexible and can dissipate more heat than thicker ones. Joining of the thinned chips can be done using several different techniques. Of these, anisotropic conductive adhesives (ACA) are an interesting option as they have several advantages such as low bonding temperature and capability for high density. The reliability of ACA flip chip joints under thermal cycling conditions has been found to increase when thinned chips are used. However, the effect of humidity has not been fully explored. In this study the reliability of thinned chips under humid conditions was investigated using thin flexible substrates. Seven test lots were assembled with thinned chips using two different ACA films and liquid crystal polymer (LCP), polyimide (PI), and thin FR-4 substrates. A high humidity and high temperature test was used to study the reliability of the interconnections. Marked differences between the substrates were seen during the test. Additionally, bonding pressure was found to be critical factor for reliability.

## Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics

Tue-Expo-17:30-P41
**Crystallographic-orientation-dependent GIDL currents in Tri-gate MOSFETs under hot carrier stress**
*Jong Tae Park, Jae Hoon Lee*
*Incheon National University, Korea*

The GIDL currents in Tri-gate MOSFETs for different crystal orientations and fin widths under hot carrier stress were examined systematically by comparing the experiments and a theoretical GIDL current model. The extracted values of model parameters provide a consistent explanation for the orientation dependence of GIDL currents in Tri-gate MOSFETs. After hot carrier stress, the large variation in values of a model parameter in non-rotated device provides a consistent explanation for a higher density of dangling bonds on (110) surfaces in Tri-gate MOSFETs. With considering hot carrier effects on the GIDL current and the drain current degradation,one can more reduce fin widths by fabricating multiple gate devices in rotated wafer.

Tue-Expo-17:30-P42
**Hot carrier and PBTI induced degradation in silicon nanowire gate-all-around SONOS MOSFETs**
*Jong Tae Park[1], Jin Hyung Choi[1], Jin-Woo Han[2], Chon Gun Yu[1]*
*[1] Incheon National University, Korea; [2] Nasa ames research center, United States*

Hot carrier and PBTI induced device degradation in nanowire gate-all-around SONOS MOSFETs with a width of 10nm and a height of 10nm have been studied with different widths and operating temperatures. The experimental data show that PBTI and hot carrier degradation are more significant in narrow devices. The possible mechanism for enhanced hot carrier degradation for narrow devices and high stress temperatures is discussed. From the comparison of hot carrier and PBTI degradation as a function of widths, the dominant component for the drain current degradation has been discussed.

Tue-Expo-17:30-P43
**Energy distribution of positive charges in high-k dielectric**
*Sharifah Fatmadiana Wan Muhamad Hatta[1], Ji Zhigang[2], Jian Zhang[2], Wei Zhang[2], Norhayati Soin[3], B Kaczer[4], S Gendt[4], G Groeseneken[4]*
*[1] University of Malaya, Malaysia; [2] Liverpool John Moores University, United Kingdom; [3] University Malaya, Malaysia; [4] IMEC, Belgium*

A probing technique to obtain the energy distribution of positive charges in high-k/SiON gate stack dielectrics, both within and beyond the substrate bandgap, has been proposed. The energy distribution of different high-k/SiON stacks has been investigated and attention has been paid to their differences from the single SiON layer devices. The results obtained from the technique demonstrate the existence of different types of positive charges whereby each type dominates different energy regions. It is observed that the positive charges in high-k/SiON stacks are dominated by the as-grown hole traps below the valence band and the cyclic positive charges within the bandgap. The increase in the cyclic positive charges in thinner high-k devices suggests higher NBTI for future CMOS technologies. It is also observed from the energy profile that the metal gate can impact the NBTI substantially. The energy profile obtained from this technique clearly indicates that process optimization is essential for minimizing NBTI in high-k gate stacks.

Tue-Expo-17:30-P44
**Defects evolution involving interface dispersion approaches in high-k/metal-gate deep-submicron CMOS**
*Yasmin Abdul Wahab, Norhayati Soin, Sharifah Fatmadiana Wan Muhammad Hatta*
*University of Malaya, Malaysia*

The importance of this paper is to propose a technique to demonstrate energy evolution of amorphous oxides defects involving a property of interface depth dispersion to significantly assess their impacts on circuits thru numerical approaches. This study provides its capability for highlighting different positively charged defects within and beyond the silicon bandgap. The defects vary significantly with energy level as well as in evolution of the E' centers and the interface states densities. The defects in E' centers below fermi energy are neutral and unstable, which significantly mount spike above thermal equilibrium during stressing and driven from valence band energy to above conduction band energy in fast recovery stage. A correlation of the time dependency for the charged trap concentration, interfacial density and the drain current is observed with current degradation due to the trap accumulation. The analysis shows a strong sensitivity to positive bias activation of the dopant thus been considered for the evaluation of the device performance.

Tue-Expo-17:30-P45
**Total ionizing dose response of fluorine implanted silicon-on-insulator buried oxide**
*Kenneth Potter[1], Katrina Morgan[1], Chris Shaw[2], Peter Ashburn[1], William Redman-White[1], C.H. de Groot[1]*
*[1] University of Southampton, United Kingdom; [2] AWE Plc, United Kingdom*

A comparison is made of the behaviour of silicon on insulator buried oxides and wet thermal oxides before and after fluorine implantation and irradiation. Before irradiation, the electrical characteristics of the thermal oxide and buried oxide are significantly different. The fluorine implantation in the smart-cut buried oxide results in a large negative threshold shift due to the trapping of positive charges. These charges are associated with positively charged fluorine ions on implantation and are trapped at pre-existing trap sites, particularly at the bonding interface, and at additional defects caused by the ion implantation damage. This shift is absent in the wet thermal oxide. After Co60 irradiation up to 500 Krad (Si), the negative flatband and threshold voltage shift in the fluorine implanted buried oxide is larger than in the unimplanted buried oxide indicating that any potential positive effect of fluorine on the passivation of interface states is more than offset by the additional trapping sites created during implantation. These results demonstrate that in the design of a transistor utmost care must be taken to prevent any fluorine being implanted into the buried oxide.

Tue-Expo-17:30-P46
**Analysing Aging and Voltage Scaling Impacts under Neutron-induced Soft Error Rate in SRAM-based Field Programmable Gate Arrays**
*Fernanda Kastensmidt[1], Jorge Tonfat[1], Thiago Both[1], Gilson Wirth[1], Paolo Rech[1], Ricardo Reis[1], Pascal Benoit[2], Florent Bruguier Bruguier[2], Lionel Torres[2]*
*[1] UFRGS, Brazil; [2] LIRMM, France*

This work investigates the effects of aging and voltage scaling in neutron-induced bit-flip in SRAM-based FPGAs. Experimental results show that aging and voltage scaling can increase in at least two times the susceptibility of SRAM-based FPGAs to Soft Error Rate (SER). These results are innovative, because they combine three real effects that occur in programmable circuits operating at ground-level applications. In addition, a model at electrical simulation for aging, soft error and different voltages was described to investigate the effects observed at the practical neutron irradiation experiment. Results can guide designers to predict soft error effects during the lifetime of devices operating in different power voltage supply mode.

## Reliability & Failure Mechanisms of Wide Bandgap Devices

Tue-Expo-17:30-P47
**Stability Evaluation of Au-free Ohmic contacts on AlGaN/GaN HEMTs under a Constant Current Stress**
*Tian-Li Wu, Denis Marcon, Steve Stoffels, Shuzhen You, Brice De Jaeger, Marleen Van Hove, Guido Grosesenken, Stefaan Decoutere*
*IMEC, Belgium*

The reliability of Au-free Ohmic contacts has been evaluated under a constant current stress (500mA/mm) in a high temperature environment (150°C, 175°C, and 200°C). Two ohmic contact schemes with different Ti/Al ratio (5nm/100nm and 10nm/100nm) have been tested. The results showed that the degradation of the resistance (Rincrease) is accelerated at a higher temperature condition. Moreover, Rincrease has a square root dependence with the time. This indicates that a diffusion process could be responsible for the observed degradation. This has been confirmed by means of physical failure analysis (FIB/TEM) performed on a highly degraded device: an apparent roughness of the interface between TiN and the Ohmic metal layer was observed. On top of this, Nitrogen out-diffusion from TiN into the ohmic metal was observed in the EDS/EELS analysis, suggesting that a material diffusion phenomenon might play a role. In addition, we observed that devices with a lower initial contact resistance (Rc) showed a less degradation with respect to devices with a larger initial Rc. This suggests that obtaining lower Rc is beneficial not only for the performance but also for the reliability.

Tue-Expo-17:30-P48
**Failure signatures on 0.25 µm GaN HEMTs for high-power RF applications**
*Antonio Stocco[1], Stefano Dalcanale[1], Fabiana Rampazzo[1], Matteo Meneghini[1], Gaudenzio Meneghesso[1], Jan Grünenpütt[2], Benoit Lambert[3], Hervé Blanck[2], Enrico Zanoni[1]*
*[1] Department of Information Engineering, University of Padova, Italy; [2] United Monolithic Semiconductors, Germany;*
*[3] United Monolithic Semiconductors, France*

GaN HEMTs for high-frequency operation are now exhibiting outstanding results in both RF performances and long-term stability, but at the moment there is not a unique indication of which failure mechanism affects the device performance in long-time scale, nor a proved technique which allows to identify the best failure accelerating factor useful for a consistent life-time extraction. In this topic, the paper tries to point-out the efficacy of short-term tests on the investigation of failure modes on two generations of AlGaN/GaN 0.25 µm gate-length HEMT transistors, highlighting the failure signatures corresponding to the early appearance of the failure modes typical of this technology: (i) a first mode correlated with a limited performance degradation marked by a left threshold voltage shift, and (ii) a second much more degrading failure mode, driven by a right threshold voltage shift. As a result, this simple preliminary investigation gives a consistent evaluation of the really improved reliability behaviour of the new HEMT technology, which shows excellent robustness from high-field to extremely high-power bias conditions, pushing out the more damaging failure mechanism from the typical operating conditions.

Tue-Expo-17:30-P49
**Crosstalk in monolithic GaN-on-Silicon power electronic devices**
*Vineet Unni[1], Hiroji Kawai[2], Sankara Narayanan[1]*
*[1] The University of Sheffield, United Kingdom;*
*[2] POWDEC K.K, Japan*

We report the presence of “crosstalk” in monolithic GaN-on-Silicon power diodes through a simple and systematic methodology of electrical measurements. The findings would be beneficial to the performance assessment of monolithically integrated power electronic circuits based on a GaN-on-Silicon technology platform. The methodology consists of evaluating the impact on the device electrical characteristics by inducing a perturbation bias on the electrode of an isolated device in the vicinity. It has been observed that the behaviour is primarily responsive to a perturbation bias of negative polarity and effectively manifests itself as reduced forward conductivity in devices. The impact of biasing an electrode of a neighbouring isolated device under floating substrate conditions and the impact of only biasing the Silicon substrate appear to be equivalent, indicating that the former behaviour may be due to the capacitively induced potential of the otherwise electrically unbiased/floating Silicon substrate. Grounding the Silicon substrate appears to mitigate the impact of the crosstalk effects under static conditions. Basic structural details of the devices under evaluation and preliminary results of the study have been reported in this paper.

Tue-Expo-17:30-P50
**Influence of different carbon doping on the performance and reliability of InAlN/GaN HEMTs**
*Isabella Rossetto[1], Fabiana Rampazzo[1], Matteo Meneghini[1], Christian Dua[2], Piero Gamarra[2], Raphael Aubry[2], Marie Antoinette Poisson[2], Sylvain L. Delage[2], Gaudenzio Meneghesso[1], Enrico Zanoni[3]*
*[1] University of Padova, Italy; [2] Thales III-V Labs, France;*
*[3] DEI-UNIPD, Italy*

This paper studies the impact of carbon buffer compensation on the performance, trapping and reliability of InAlN/GaN HEMTs. The analysis was carried out on two series of devices with different carbon doping levels in the GaN buffer layer. Preliminary DC characterization revealed a very slight difference in drain current measured in high power dissipation conditions and a variation of the maximum transconductance measured in saturation zone. No significant difference is shown in DC leakage drain current and threshold voltage value. However carbon doping was found to have a strong impact on the trapping characteristics: pulsed evaluation demonstrated that the devices show a significant current collapse, well correlated to the dynamical shift in threshold voltage; moreover, drain current transient investigation revealed two main traps (T2, T1) with activation energy of 0.89eV and 1.05eV, respectively. A more detailed analysis suggests that trap T2 is located in the buffer layer, its concentration is correlated with carbon doping and it behaves as a line defect. Finally the investigation of reliability demonstrates that the use of high carbon doping does not significantly influence the robustness of the devices with respect to DC OFF-state stress.

## Reliability & Failure Mechanisms of Photonic and Special Devices

Tue-Expo-17:30-P51
**The effect of gate overlap on the device degradation in IGZO thin film transistors**
*Jong Tae Park, Dae Hyun Kim*
*Incheon National University, Korea*

The effect of gate overlap on the device degradation in IGZO TFTs treated by H2 and Ar plasma was experimentally investigated after positive and negative biases stress and hot carrier stress. After positive and negative biases stress, the decrease of the threshold voltage shifts with increase of the gate overlaps may be attributed to the carrier diffusion from the n- extended source and drain regions to the intrinsic channel region. The hot carrier induced threshold voltage shifts were increased with increase of the gate overlap due to the reduction of effective channel length.

Tue-Expo-17:30-P52
**Dispersion study of DC and Low Frequency Noise in SiGe:C Heterojunction Bipolar Transistors used for mm-Wave to Terahertz applications**
*Marcelino Seif[1], Fabien Pascal[1], Bruno Sagnes[1], Alain Hoffmann[1], Sebastien Haendler[2], Pascal Chevalier[2], Daniel Gloria[2]*
*[1] IES - Université Montpellier 2, France; [2] STMicroelectronics Crolles, France*

This work presents an investigation of DC and low frequency noise dispersion in 0.13 µm SiGe:C BiCMOS heterojunction bipolar transistors (HBTs) used for mm-Wave to Terahertz application. Therefore DC and Low Frequency noise measurements have been performed over a half wafer containing a large number of transistors. A statistical 1/f noise compact model is presented as well as a study of the repartition of generation-recombination components. The main low frequency noise sources are found to be homogenously distributed in the intrinsic base-emitter junction. The mean 1/f noise level, evaluated by the figure of merit KBmean, is equal to 6 10-10 µm2.

Tue-Expo-17:30-P53
**The degradation of multi-crystalline silicon solar cells after damp heat tests**
*Wonwook Oh[1], Seongtak Kim[1], Soohyun Bae[1], Nochang Park[2], Yoonmook Kang[1], Haeseok Lee[1], Donghwan Kim[1]*
*[1] Korea university, Korea; [2] KETI, Korea*

Lower performance of multi-crystalline silicon solar cells is usually observed after long-term damp heat test at 85°C/85% relative humidity. Performance degradation is known to result from the loss in fill factor (FF) due to high series resistance. The causes of the increase in the series resistance are the reduction of the photovoltaic (PV) ribbon in the solder joint and the oxidation of surface on the front Ag finger by high thermal and moisture stress. Additionally, severe degradation by FF loss after damp heat originated from the contact resistance between Si and Ag fingers. Ag crystallites on Si wafer and bulk Ag at the edge of the Ag finger were partially oxidized and could not play a role in the current path of photo-generated electrons.

Tue-Expo-17:30-P54
**A fast reliability assessment method for Si MEMS based microcantilever beams**
*Peyman Rafiee, Golta Khatibi*
*University of Vienna, Austria*

In the present study the effect of size and locations of the defects and the loading types on vibrational response and robustness of MEMS Si single crystalline microcantilever beams was investigated. A new vibrational based testing method was developed in order to study the reliability of Si beams and to obtain lifetime curves in a short duration of time.
Si microcantilever beams with a proof mass and different notch sizes were subjected to two types of vibrational loads including constant loading at the resonant frequency and sweep excitation covering the first two resonant frequencies.
Constant vibrational loading at resonant frequency was applied to obtain the reliability data for the beams in terms of stress amplitude versus time to fracture. In comparison with constant frequency conditions, loading of the specimens by using a fast frequency sweep and the same amount of input excitation energy resulted in a clear reduction of the lifetime of the beams. It was found that the time to fracture was highly dependent on the size of the notches, type of the loading and pre-loading conditions.
Finite element analysis was utilized to find the most critical location of the specimen where the induced notch results in the highest stress concentration and also to calculate the stress under which fracture occurs.

## Focused Ion Beam and European FIB User Group

Tue-Expo-17:30-P55
**Low temperature FIB cross section: application to indium micro bumps**
*Lionel Dantas De Morais, Sophie Chevalliez, Stephanie Mouleres*
*SOFRADIR, France*

This paper presents the interest of low temperature FIB cross section on indium micro bump. Experimental setup and results which demonstrate the interest of cooling the sample are detailed. We will explain the artefacts observed during FIB milling at room temperature. The Ga ions interact with indium to create locally an eutectic alloy, with melting point below room temperature. Inside the vacuum chamber, this eutectic alloys sublimates quickly and voids appear in the cross section. Cooling the sample with cryogenic stage enables to perform “clean” cross section without these artefacts.

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Pascal, Venet: Tue-Expo-17:30-P05
Paterno, Giuseppe: Tue-C-15:40
Paul, Erik: Tue-Expo-17:30-P14
Paulasto-Kröckel, Mervi: Thu-C-08:30-Invited
Perdu, Philippe: Wed-A-12:00, Wed-A-14:20, Wed-A-14:40
Perpiñà, Xavier: Thu-B-09:50, Wed-B-11:20
Petrov, Aleksandr S.: Tue-Expo-17:30-P04
Petzold, Matthias: Wed-C-14:20
Pey, Kin Leong: Thu-A-09:50, Thu-A-12:10, Tue-A-11:30, Tue-A-16:00, Tue-Expo-17:30-P01
Phulpin, Tanguy: Thu-B-11:10
Phung, Luong-Viêt: Tue-A-16:20
Pinkert, Martin: Tue-Expo-17:30-P18
Pippola, Juha: Tue-Expo-17:30-P38, Wed-A-15:00
Poisson, Marie Antoinette: Tue-Expo-17:30-P50
Polywka, Andreas: Tue-C-13:50
Possamai Bastos, Rodrigo: Thu-A-11:50
Postel-Pellerin, Jeremy: Thu-A-09:30
Potin, Olivier: Thu-A-11:50
Potter, Kenneth: Tue-Expo-17:30-P45
Preu, Harald: Wed-C-16:10
Pufall, Reinhard: Tue-Expo-17:30-P15

## R

Rafiee, Peyman: Tue-Expo-17:30-P54
Raghavan, Nagarajan: Thu-A-08:30-Invited, Thu-A-09:50, Thu-A-12:10, Tue-Expo-17:30-P01
Rajamanickam, Sivanyanam: Tue-Expo-17:30-P35
Ramli, Rahizar: Tue-Expo-17:30-P37
Ramom, Eloi: Tue-Expo-17:30-P13
Rampazzo, Fabiana: Thu-B-10:50, Tue-Expo-17:30-P48, Tue-Expo-17:30-P50
Randoll, Richard: Wed-B-15:00
Rebaï, Mehdi Mohamed: Wed-A-12:00
Rech, Paolo: Tue-Expo-17:30-P46
Redman-White, William: Tue-Expo-17:30-P45
Reid, Derryck T.: Wed-A-13:30-Invited
Reis, Ricardo: Thu-A-14:30, Tue-Expo-17:30-P46
Reisinger, Hans: Thu-A-14:10
Reuther, Georg Michael: Tue-Expo-17:30-P15
Reverdy, Antoine: Wed-A-11:20
Riccio, Michele: Thu-B-08:30, Wed-B-10:40, Wed-B-11:00, Wed-B-11:40
Riedl, Thomas: Tue-C-13:50
Rimmen, Peter De Place: Tue-A-10:50
Robbiano, Valentina: Tue-C-15:40
Robinson, Colin: Thu-A-09:10
Roche, Philippe: Thu-A-11:10
Rodriguez, Raul: Wed-C-12:00
Roetz, Hagen: Tue-Expo-17:30-P18
Röhner, Michael: Thu-B-13:50
Ronchi, Nicolò: Thu-B-09:10
Rongen, René: Tue-A-11:10, Wed-C-13:30-Invited
Ronsisvalle, Cesare: Tue-Expo-17:30-P26
Rossetto, Isabella: Tue-Expo-17:30-P50
Rostaing, Gilles: Wed-B-11:40
Rott, Gunnar Andreas: Thu-A-14:10
Rott, Karina: Thu-A-14:10
Rouzeyre, Bruno: Thu-A-11:50
Rückerl, Andreas: Tue-Expo-17:30-P03
Rudolf, Ralf: Thu-B-13:50, Tue-Expo-17:30-P18
Rzepka, Sven: Wed-C-12:00

## S

Saarinen-Pulli, Kirsi: Tue-Expo-17:30-P40
Sadowski, Michael: Tue-B-11:30
Sagnes, Bruno: Tue-Expo-17:30-P52
Sanchez, Kevin: Wed-A-14:20
Sander, Christoph: Wed-C-11:40
Sanseverino, Annunziata: Thu-B-09:30, Tue-Expo-17:30-P26
Santini, Thomas: Tue-A-16:20
Sarafianos, Alexandre: Thu-A-11:50
Sari, Ali: Tue-B-15:20, Tue-B-16:00
Satoh, Toshikazu: Wed-B-14:40
Savoia, Claudio: Tue-Expo-17:30-P20
Schaubroek, David: Tue-Expo-17:30-P33
Schlangen, Rudolf: Tue-B-11:50
Schletz, Andreas: Wed-B-15:00
Schneider-Ramelow, Martin: Thu-B-13:30
Scholz, Philipp: Tue-B-11:30
Schulz, Matthias: Thu-B-08:50
Schwarz, U. T.: Thu-C-09:40
Schweinboeck, Thomas: Wed-A-11:00
Seif, Marcelino: Tue-Expo-17:30-P52
Seima, Shili: Tue-Expo-17:30-P05
Selberherr, Siegfried: Tue-Expo-17:30-P19, Wed-C-11:20
Shaw, Chris: Tue-Expo-17:30-P45
Shevchenko, Sergey: Thu-B-08:50
Shi, Xiaoping: Wed-C-10:40
Siddabathula, Mahesh: Thu-A-13:50
Simon-Najasek, Michél: Tue-B-10:50
Sintamarean, Nicolae Cristian: Tue-A-10:50
Siol, Christopher: Tue-C-15:20
Soci, Fabio: Thu-B-11:30
Soellner, Norbert: Wed-C-16:10
Soin, Norhayati: Tue-Expo-17:30-P43, Tue-Expo-17:30-P44
Soufflet, Pierre: Thu-B-14:10
Sowade, Enrico: Tue-Expo-17:30-P13
Squiller, David: Tue-A-13:30
Stefani, Andrea: Tue-C-16:00
Steiert, Matthias: Tue-A-13:50
Stern, Lewis: Tue-B-10:20-Invited
Stirlen, Neal: Wed-A-10:40
Stocco, Antonio: Thu-B-10:50, Tue-Expo-17:30-P48
Stoffels, Steve: Thu-B-09:10, Tue-Expo-17:30-P47
Strasser, Marc: Tue-Expo-17:30-P18
Stucchi, Michele: Wed-C-10:40
Sudzius, Markas: Tue-C-16:20
Sun, Fenglian: Tue-Expo-17:30-P34, Tue-Expo-17:30-P39
Supono, Ihsan: Tue-Expo-17:30-P22

## T

Takaishi, Junpei: Thu-B-14:30
Talut, Georg: Tue-A-11:50
Tan, Chuan Seng: Tue-A-11:30
Tan, Yik Yee: Tue-Expo-17:30-P35
Tang, Baojun: Thu-A-09:10, Tue-A-13:10
Tapero, Konstantin I.: Tue-Expo-17:30-P04
Tee, Kheng Chok: Tue-A-11:30
Teo, Kok Seng: Tue-Expo-17:30-P35
Tetzner, Kornelius: Tue-Expo-17:30-P12
Thoben, Markus: Wed-B-13:30-Invited
Tokei, Zsolt: Tue-A-13:10
Toledano-Luque, Maria: Thu-A-09:10, Tue-A-13:10
Tonfat, Jorge: Tue-Expo-17:30-P46
Tormen, Fabio: Tue-Expo-17:30-P20
Torres, Lionel: Tue-Expo-17:30-P46
Tournier, Dominique: Thu-B-11:10
Tran, Son-Ha: Tue-Expo-17:30-P25
Tremouilles, David: Thu-B-11:10
Trentzsch, Martin: Thu-A-13:50

Trivellin, Nicola: Thu-C-09:00, Thu-C-09:40
Trost, Sara: Tue-C-13:50
Tsukuda, Masanori: Thu-B-14:30, Thu-B-14:50
Turatti, Guido: Tue-C-16:00

## U

Ueda, Hiroyuki: Thu-B-11:50
Uesugi, Tsutomu: Thu-B-11:50
Ulimov, Viktor N.: Tue-Expo-17:30-P04
Unni, Vineet: Tue-Expo-17:30-P49
Urresti, Jesus: Tue-Expo-17:30-P22

## V

Vakanas, George: Tue-Expo-17:30-P33
Van Besien, Els: Wed-C-10:40
Van den Bosch, Geert: Thu-A-09:10
van Dijk, Marius: Wed-B-14:20
van Elsbergen, Volker: Tue-A-09:10-Keynote
Van Houdt, Jan: Thu-A-09:10
Van Hove, Marleen: Tue-Expo-17:30-P47
Van Huylenbroeck, Stefaan: Wed-C-10:40
Vandecasteele, Bjorn: Tue-Expo-17:30-P33
Vanhuffel, Béatrice: Wed-A-10:40
Vanzi, Massimo: Thu-C-10:00
Vazquez, Manuel: Thu-C-10:50
Velardi, Francesco: Thu-B-09:30, Tue-Expo-17:30-P26
Vellvehi, Miquel: Thu-B-09:50, Wed-B-11:20
Venegas, Rafael: Thu-B-09:10
Venet, Pascal: Tue-B-15:20, Tue-B-16:00
Victory, James: Tue-Expo-17:30-P26
Villani, Fulvia: Tue-Expo-17:30-P13
Vinassa, Jean-Michel: Tue-B-15:20, Tue-Expo-17:30-P29
Vogel, Dietmar: Wed-C-12:00
von Seggern, Heinz: Tue-C-15:20

## W

Wachowiak, Andre: Tue-Expo-17:30-P18
Wade, Massar: Wed-C-15:00
Wagner, Catejan: Tue-Expo-17:30-P18
Wagner, J.: Thu-C-09:40
Wagner, Tim: Tue-C-16:20
Walter, Jürgen: Wed-C-16:10
Wan Muhammad Hatta, Sharifah Fatmadiana: Tue-Expo-17:30-P43
Wan Muhammad Hatta, Sharifah Fatmadiana: Tue-Expo-17:30-P44
Wan, Xinggong: Thu-A-13:50
Wang, Huai: Tue-A-10:50
Wang, Xiang-Dong: Wed-A-10:40
Wang, Yangang: Tue-Expo-17:30-P23
Wang, You: Tue-Expo-17:30-P11
Wang, Yunqi: Thu-A-09:10, Tue-A-13:10
Wang, Zhongrui: Tue-A-16:00
Weber, Yann: Wed-A-10:40
Wehrmeister, Sebastian: Tue-C-14:10
Weide-Zaage, Kirsten: Tue-A-16:40, Tue-Expo-17:30-P32, Wed-C-15:00
Weig, T.: Thu-C-09:40
Weinbub, Josef: Tue-Expo-17:30-P19
Wilcox, Geoffrey: Tue-Expo-17:30-P33
Wilde, Jürgen: Tue-A-13:50
Willems, Geert: Tue-Expo-17:30-P33
Wilshaw, Peter: Thu-C-11:30
Wirth, Gilson: Tue-Expo-17:30-P46
Wolf, J.: Wed-C-11:00
Wondrack, Wolfgang: Wed-B-15:00
Wong, Cell K.Y.: Tue-Expo-17:30-P34
Wouters, Yves: Tue-A-14:10
Wrachien, Nicola: Tue-C-16:00
Wu, Chen: Wed-C-10:40
Wu, Huimeng: Tue-B-10:20-Invited
Wu, Tian-Li: Tue-Expo-17:30-P47
Würfl, Hans-Joachim: Thu-B-08:50

## Y

Yamada, Yasushi: Wed-B-14:40
Yamamoto, Kenichi: Thu-B-14:50
Yang, Li: Thu-B-08:30
Yoshida, Hidetaro: Thu-B-14:50
You, Shuzhen: Thu-B-09:10, Tue-Expo-17:30-P47
Yu, Chon Gun: Tue-Expo-17:30-P42
Yuan, Cadmus A.: Tue-Expo-17:30-P34
Yun, Ilgu: Thu-C-11:50

## Z

Zahn, Dietrich: Wed-C-12:00
Zanoni, Enrico: Thu-B-10:50, Thu-B-11:30, Thu-C-09:00, Thu-C-09:40, Tue-Expo-17:30-P48, Tue-Expo-17:30-P50
Zeisel, Roland: Tue-Expo-17:30-P03
Zhang, Ganggang: Tue-Expo-17:30-P28
Zhang, Guoqi: Tue-Expo-17:30-P34
Zhang, Hongwu: Tue-Expo-17:30-P39
Zhang, Jian: Tue-Expo-17:30-P43
Zhang, Jianfu: Thu-A-09:10
Zhang, Wei: Tue-Expo-17:30-P43
Zhang, Weidong: Thu-A-09:10
Zhang, Xing: Tue-Expo-17:30-P28
Zhang, Yue: Tue-Expo-17:30-P11
Zhao, Jia: Tue-Expo-17:30-P34
Zhao, Weisheng: Tue-Expo-17:30-P11
Zhigang, Ji: Tue-Expo-17:30-P43
Zhou, Zhen: Tue-Expo-17:30-P39
Zisser, Wolfhard H.: Tue-Expo-17:30-P19
Zschech, Ehrenfried: Wed-C-11:00

# Notes

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# Equipment Exhibition

Accel-RF Instruments Corporation

www.accelrf.com

KUMMER SEMICONDUCTOR TECHNOLOGY

www.jpkummer.com

ALLIED HIGH TECH PRODUCTS, INC.

www.alliedhightech.com

LATTICEGEAR Cleaving Tools www.latticegear.com

www.latticeGear.com

FEI™

www.fei.com

NEOCERA

www.neocera.com

Fraunhofer IZM

www.izm.fraunhofer.de

PVA TePla

ww.pva-analyticalsystems.com

HAMAMATSU PHOTON IS OUR BUSINESS

www.hamamatsu.de

ROHDE&SCHWARZ

www.rohde-schwarz.de

IRLabs A SUBSIDIARY OF INFRARED LABORATORIES, INC.

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SECTOR TECHNOLOGIES

www.sector-technologies.com

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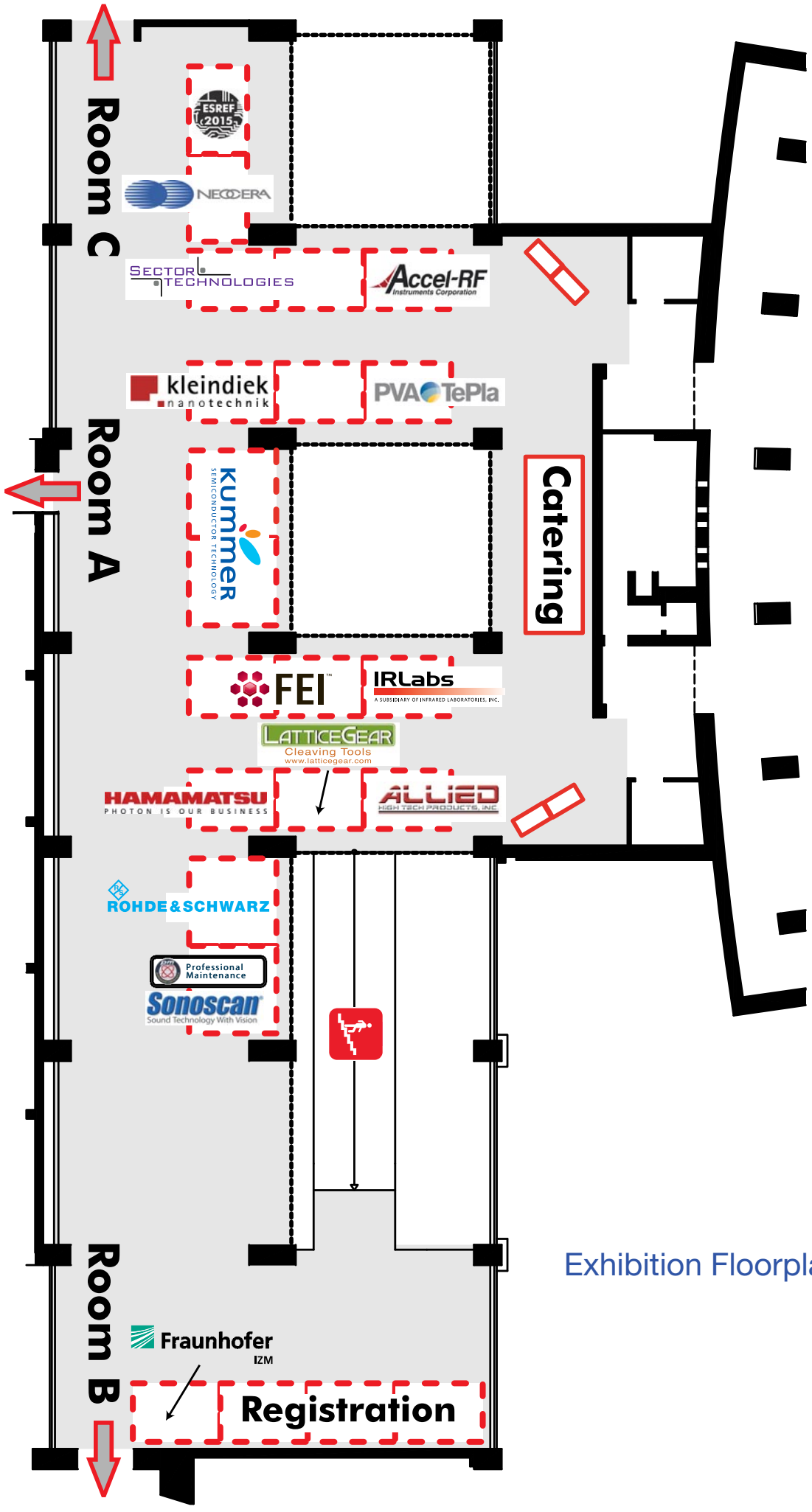
www.nanotechnik.com

Professional Maintenance

Sonoscan Sound Technology With Vision

www.pm-service-gmbh.de, www.sonoscan.com




Exhibition Floorplan

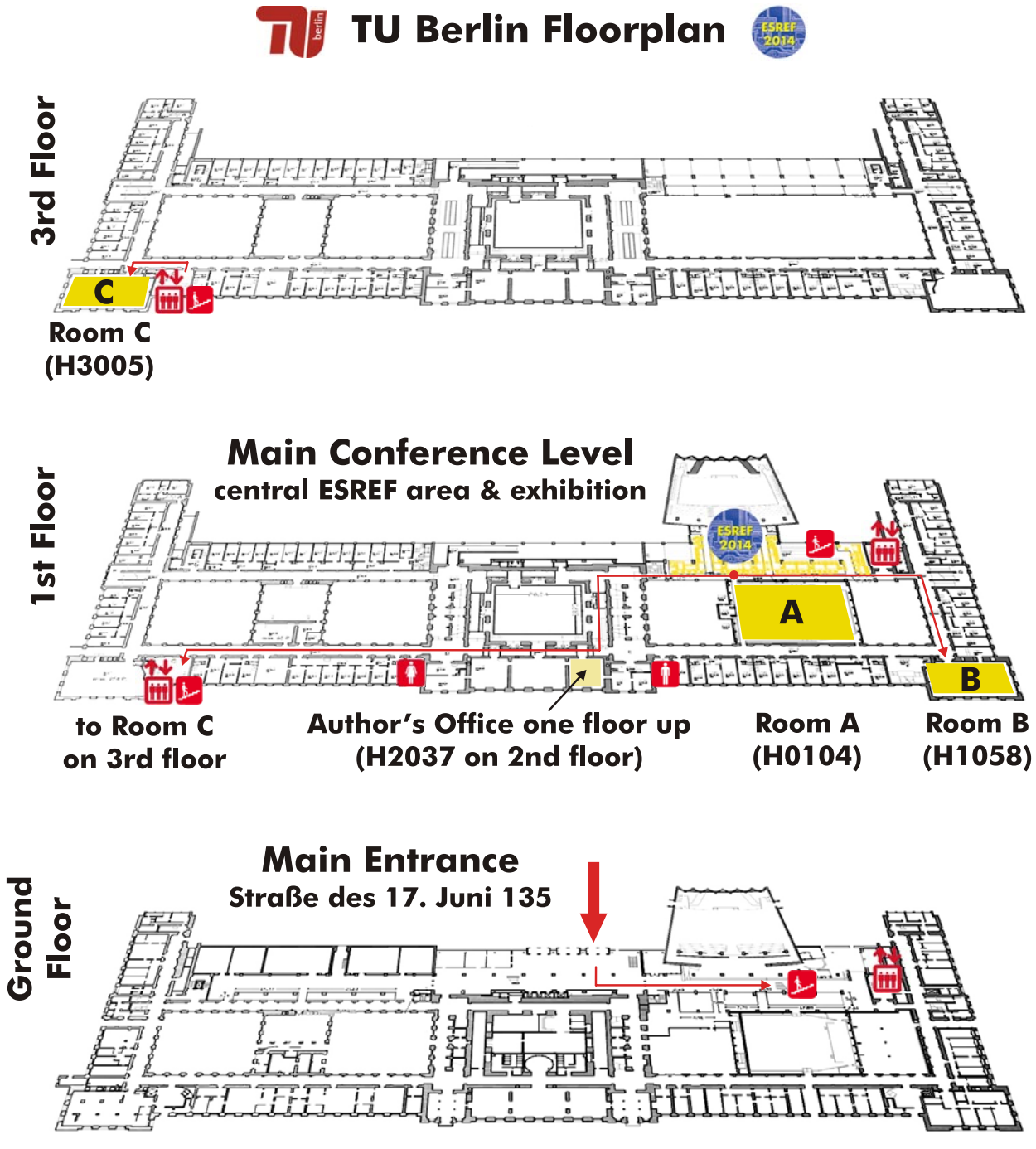
# TU Berlin Floorplan – How to find your way around the venue

ESREF 2014 uses 5 main locations at the TU Berlin:

- Central ESREF area and exhibition area on the 1st floor
- Room A - plenary hall (H0104) on the 1st floor
- Room B (H1058) on the 1st floor
- Room C (H3005) on the 3rd floor
- Author's Office (H2037) on the 2nd floor

The map shows you suggested routes leading from the central ESREF area (right next to Room A) to Room B and Room C.

Every presentation, tutorial and workshop has its unique code to tell you when and where it is taking place. The code reads "Day-Room-Time-Category", e.g. "Tue-A-10:20-Invited" - while Category is not used for oral presentations.



| | Room: A | Room: B | Room: C |
|---|---|---|---|
| **Monday 29.09.2014** | | | |
| 18:00 | Official Opening | | |
| 18:20 | Exchange Papers<br>IEEE IRPS 2014, IEEE IPFA 2014, ISTFA 2013 | | |
| 19:20 | Exhibition Opening | | |
| 19:40 | Room: Exhibition Area — Opening Reception | | |
| **Tuesday 30.09.2014** | | | |
| 08:30 | Keynote 1: Organic photovoltaic stability: Designed to last | | |
| 09:10 | Keynote 2: OLEDs quality and reliability | | |
| 09:50 | Coffee Break | | |
| 10:20 | Quality and Reliability Assessment - Techniques and Methods for Devices and Systems | Focused Ion Beam and European FIB User Group | Tutorial Reliability & Failure Mechanisms of Organic Devices |
| 12:10 | Lunch Break | | |
| 13:10 | Quality and Reliability Assessment - Techniques and Methods for Devices and Systems | Workshop Focused Ion Beam and European FIB User Group | Reliability & Failure Mechanisms of Organic Devices |
| 14:50 | Coffee Break | | |
| 15:20 | Quality and Reliability Assessment - Techniques and Methods for Devices and Systems | Power Devices Reliability – Passive & Supercapacitors | Reliability & Failure Mechanisms of Organic Devices |
| 17:00 | Coffee Break | | |
| 17:30 | Poster Session | | |
| **Wednesday 01.10.2014** | | | |
| 08:30 | Tutorial Failure Analysis | Tutorial Power Devices Reliability | Tutorial Chip-Package Interactions and 3D Reliability & Failure Mechanisms |
| 10:10 | Coffee Break | | |
| 10:40 | Failure Analysis | Power Devices Reliability<br>Electrical & Thermal Analysis, Modelling | Chip-Package Interactions and 3D Reliability & Failure Mechanisms |
| 12:20 | Lunch Break | | |
| 13:30 | Failure Analysis | Power Devices Reliability<br>Power Device Assembly | Reliability & Failure Mechanisms in Packages and Assembly |
| 15:20 | Coffee Break | | |
| 15:50 | Workshop + EUFANET Failure Analysis | Workshop Power Devices Reliability | Reliability & Failure Mechanisms in Packages and Assembly |
| 18:30 | Bus Transfer with Guided City Tour - Pickup in front of TUB Main Entrance (Straße des 17. Juni 135) | | |
| 19:30 | Social Event - Palais at the Kulturbrauerei (Bus Transfer is provided back to TU Berlin) | | |
| **Thursday 02.10.2014** | | | |
| 08:30 | Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics | Reliability & Failure Mechanisms of Wide Bandgap Devices | Reliability & Failure Mechanisms of Photonic and Special Devices |
| 10:20 | Lunch Break | | |
| 10:50 | Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics ESD/SER | Reliability & Failure Mechanisms of Wide Bandgap Devices | Reliability & Failure Mechanisms of Photonic and Special Devices |
| 12:30 | Lunch Break | | |
| 13:30 | Reliability & Failure Mechanisms in Si-Technology and Nanoelectronics FEOL | Power Devices Reliability<br>Devices & Processes | Chip-Package Interactions and 3D Reliability & Packages and Assembly & Failure Mechanisms Workshop |
| 15:10 | Coffee Break | | |
| 15:30 | Closing Ceremony and Best Paper Award | | |