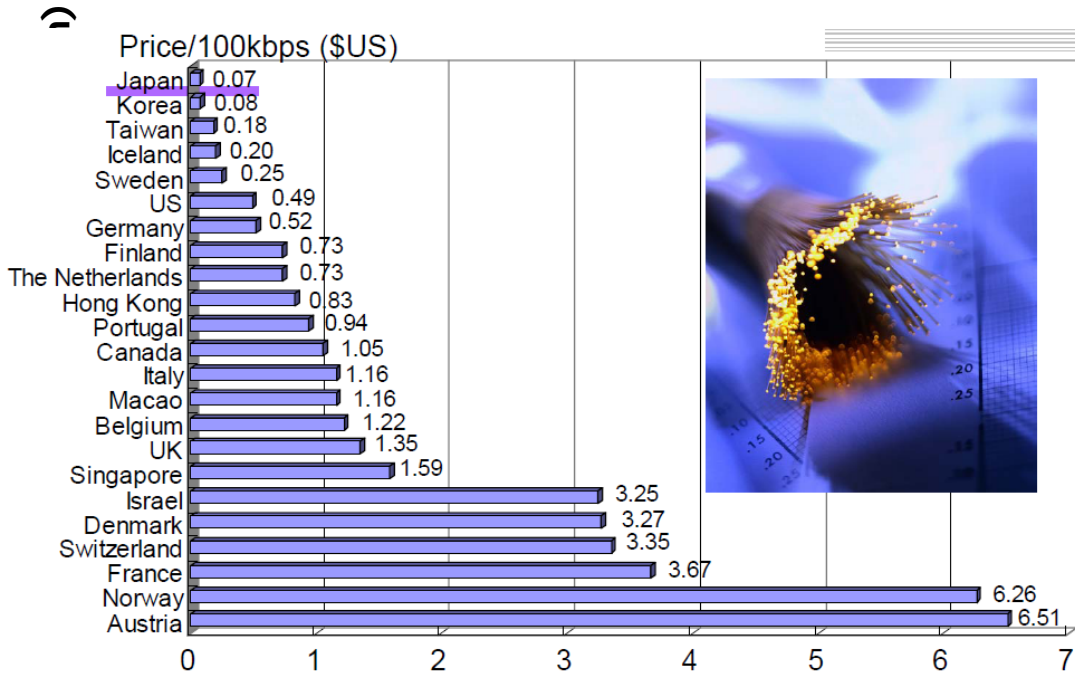# 100G – A carrier's view as an infrastructure

2009.9.20
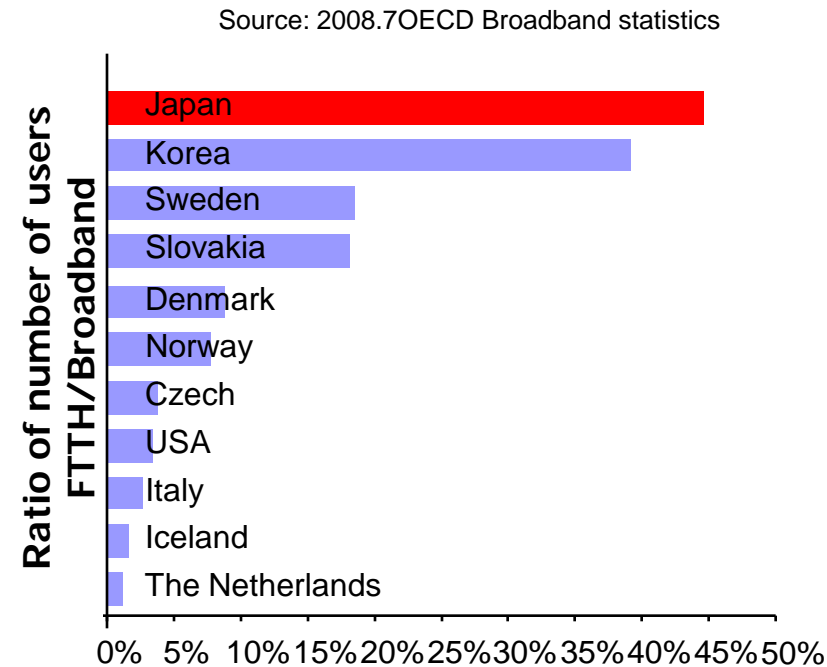
Yutaka Miyamoto, and Masahito Tomizawa

NTT Network Innovation Labs.

FTTH update in NTT and Japan

Price/100kbps ($US)

Country	Value
Japan	0.07
Korea	0.08
Taiwan	0.18
Iceland	0.20
Sweden	0.25
US	0.49
Germany	0.52
Finland	0.73
The Netherlands	0.73
Hong Kong	0.83
Portugal	0.94
Canada	1.05
Italy	1.16
Macao	1.16
Belgium	1.22
UK	1.35
Singapore	1.59
Israel	3.25
Denmark	3.27
Switzerland	3.35
France	3.67
Norway	6.26
Austria	6.51

Source:"ITU Internet Reports 2005: The Internet of Things"(Nov. 2005)

Total Fiber length~3.7 x 10^9 m
Coverage ~ 90% (@2009 forecast)

Source: 2008.7OECD Broadband statistics

Ratio of number of users FTTH/Broadband

Japan
Korea
Sweden
Slovakia
Denmark
Norway
Czech
USA
Italy
Iceland
The Netherlands

0% 5% 10% 15% 20% 25% 30% 35% 40% 45% 50%

Nearly 50% of broadband users in Japan enjoy services over FTTH infrastructure.

Necessity of higher-speed on a wave

- **New services**
  - Router-to-router connection
    - 40GPOS/40GE/100GE bulk service by BIG routers/switches
    - Driver of the initial installation of 40G, 100G transport
- **CapEX**
  - Huge data in smaller number of fibers
    - Ramping up of the volume 10GEthernet services.
    - Avoiding new fiber deployment
    - Spectral efficiency is a key
    - Lower cost/bit/s
- **OpEX**
  - For easier operation
    - Decreasing the frequency of line-card insertion
    - Relaxing the management of line-card logistics

Carriers are always interested in the highest-speed on a wavelength.
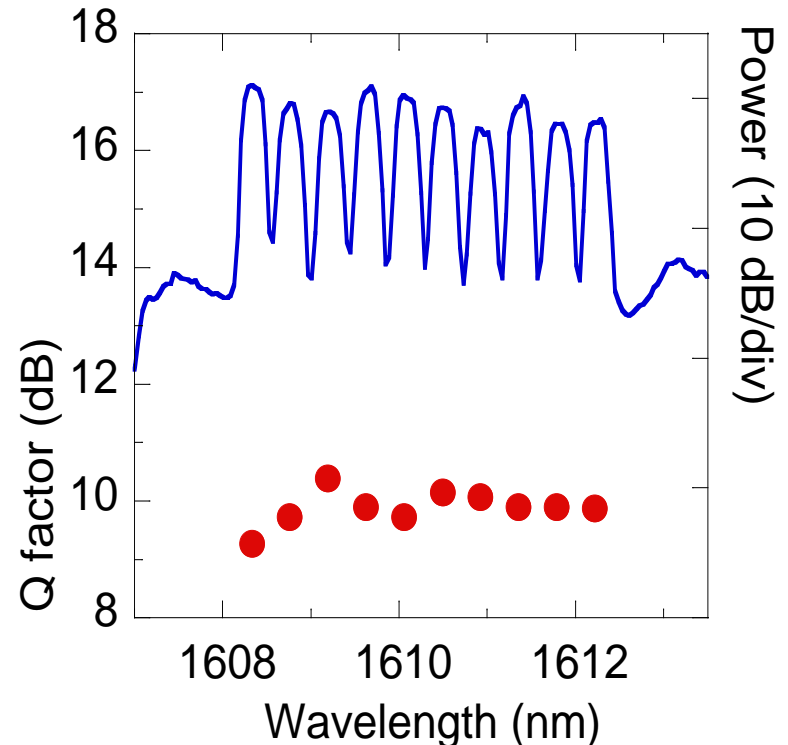
Requirements

- Some carriers ask vendors to release 100G transport
  - 2010 Q2

- 100G transport is very challenging in 10G based design links
  - 50GHz spacing
  - 1000-2000km
  - Coherent transmission assisted by DSP will be required.

- Very high-speed optical transmission market is small.
  - We cannot change the device roadmap of semiconductors.
  - When is the timing for 100G transport?
    - To have an appropriate format/device selection
    - To get a sensible investment

Potential performances
of 100G Digital Coherent Technologies

13.5 Tbps (135 x 111G) -7209km
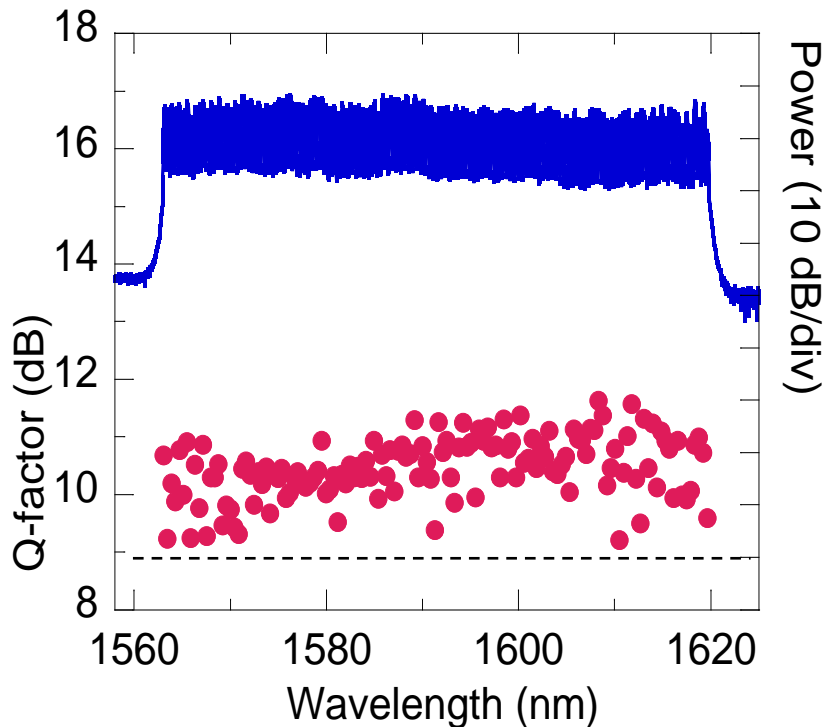
1 Tbps (10 x111G) -10093 km

50 GHz spacing WDM transport over 1000 km is feasible using digital coherent system.

100G level ADC in CMOS

43G ADC in CMOS   112G ADC in CMOS (43 x 2.5)

2006 UPDATE TECHNOLOGY REQUIREMENTS TABLES

Table 46a   RF and Analog Mixed-Signal CMOS Technology Requirements—Near-term Years

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	35	32
Performance RF/Analog [1]									
Supply voltage (V) [2]	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1	1
T_{ox} (nm) [2]	2.2	2.1	2.0	1.9	1.6	1.5	1.4	1.4	1.3
Gate Length (nm) [2]	75	65	53	45	37	32	28	25	22
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$ [3]	47	40	32	30	30	30	30	30	30
1/f-noise ($\mu V^2 \cdot \mu m^2$/Hz) [4]	190	180	160	140	100	90	80	80	70
$\sigma\ V_{th}$ matching (mV·µm) [5]	6	6	6	6	5	5	5	5	5
I_{ds} (µA/µm) [6]	19	15	13	11	9	8	7	6	6
Peak F_t (GHz) [7]	120	140	170	200	240	280	320	360	400
Peak F_{max} (GHz) [8]	200	220	270	310	370	420	480	530	590
Revised Peak Fmax (GHz) in 2008 revision				200	240	290	340	390	440	510

Analogue & RF in CMOS; 1.1~1.2 x speed enhancement by every year.
Suppose that 43G-level (10Gbaud) ADC in CMOS was operated in 2006 in volume commercial systems.
The same level 112G-level ADC would be operable in 2012 in volume commercial systems.

Timing for 100G transport

- When is the timing for 100G transport?
    - Following the semiconductor roadmap.
- The enabler and bottleneck for early adoption
    - ADC in CMOS (with DSP) by 1-chip
        - Supposing 43G-ADC in 2006, 112G-ADC will be operated in 2012 in commercial (volume) phase.

    - We have to take a careful attention whether the linear extension is applicable or not.
        - Semiconductor crisis by economic downturn
        - Speed enhancement seems slow-down from 2006-roadmap to 2008-roadmap.
        - Standby power reduction, design tool-kits in 45-35nm CMOS process.

- An interim step for 100GE/OTN would be necessary for early adopters.
    - About 2010
    - Not for volume business, but for some demonstration
    - Challenging technologies (sometimes tricky) may be adopted in the early stage.

Interim steps candidates

- About 2010,
- 1) Use of existing infrastructure
    - 100GE can be mapped into 2 x 43G or 2 x 56G
        - Subcarriers, optical PolDMX, WDM,..

- 2) ADC and DSP separation for serial 112G
    - ADC in SiGe-BiCMOS technologies, DSP in CMOS
    - Special type of interconnection should be developed.
    - Power,..

- 3) Innovation on the current CMOS-ADC for serial 112G
    - Special type of sampling technology is required.