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Challenges for VLSI implementation of 100G digital coherent receivers

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Acknowledgments

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- Fujitsu advanced technology
- Fujitsu Laboratories

Example configuration of 100G digital coherent LSI

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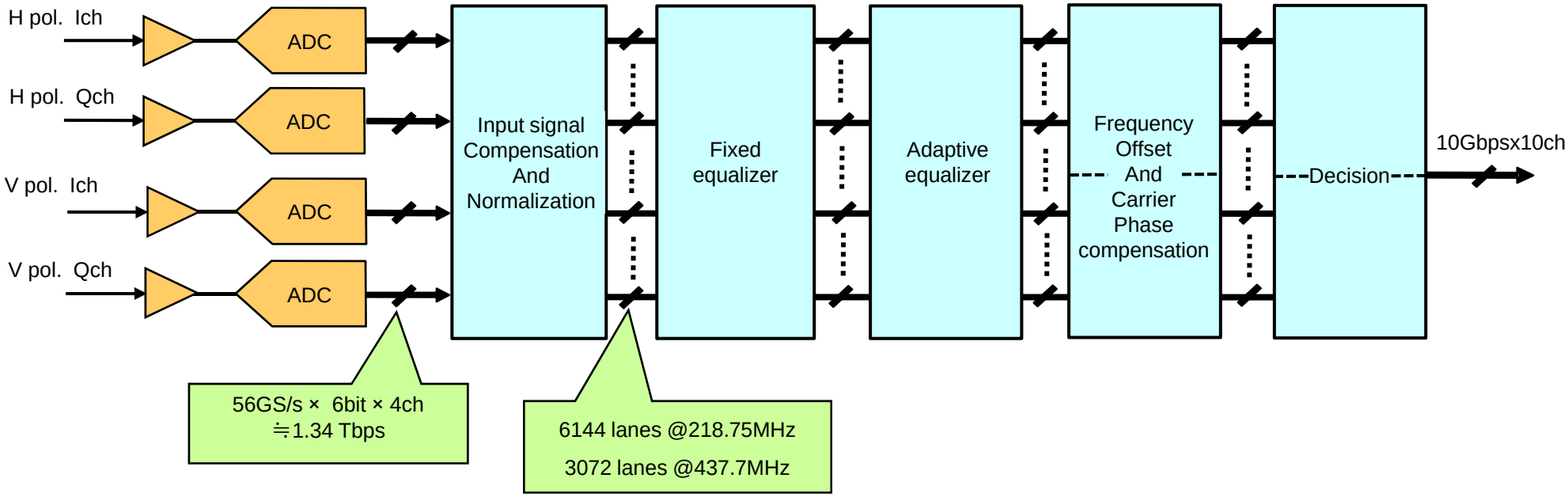

Technical challenges

- Connection between ADC and DSP
- Lower power consumption
- Efficiency improvement of LSI development

Technical challenge 1
Connection between ADC and DSP

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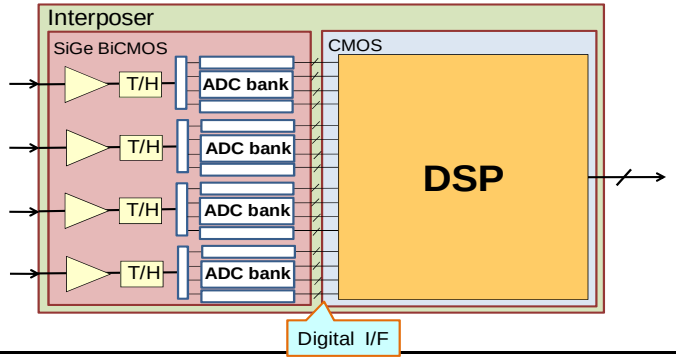
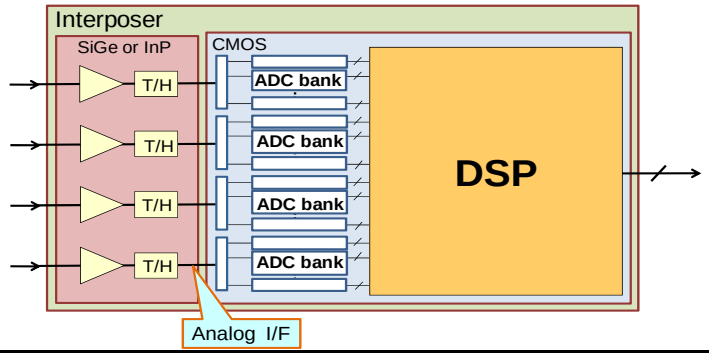
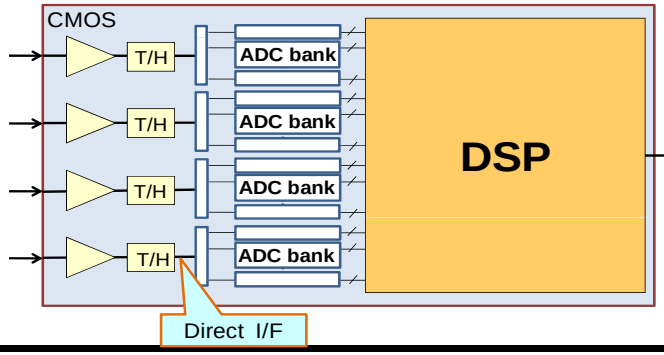
Case	Connection method		Technical Subjects
(a)		• Multichip configuration - ADC: SiGe Bi-CMOS - DSP: CMOS • Connection with digital signal	• Tbps class digital interconnection between ADC and DSP • Hybrid packaging of ADC and DSP
(b)		• Multichip configuration -T/H: SiGe, InP etc. -ADC Bank, DSP: CMOS • Connection with analog signal	• Noise and crosstalk in connection of analogue signal • Hybrid packaging of ADC and DSP
(c)		• Monolithic configuration -All functions are integrated on Si • Direct connection on Si	• Ideal configuration • Feasibility of CMOS ADC • Mixed signal system LSI design

Discussion about power consumption of 100G MSA module in OIF

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Power Dissipation

OIF

Assumption:

- Air temperature before module: 55° C
- Module temperature: ~70° C

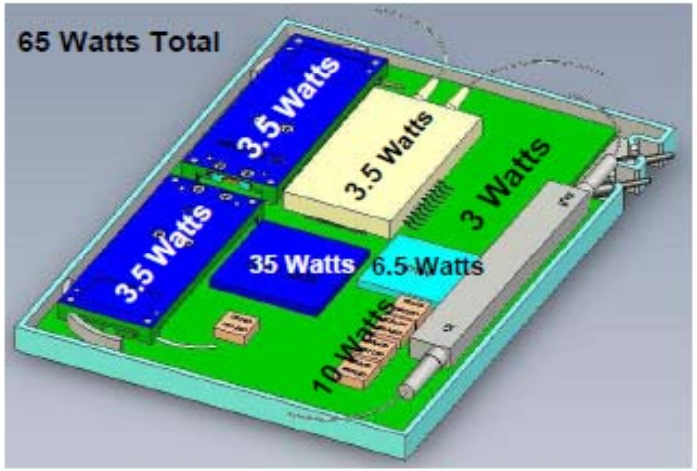
Maximum power dissipation:

Airflow	20 mm height with 13 mm fins	16 mm height with 17 mm fins
1 m/s	59W	65W
2 m/s	73W	80W

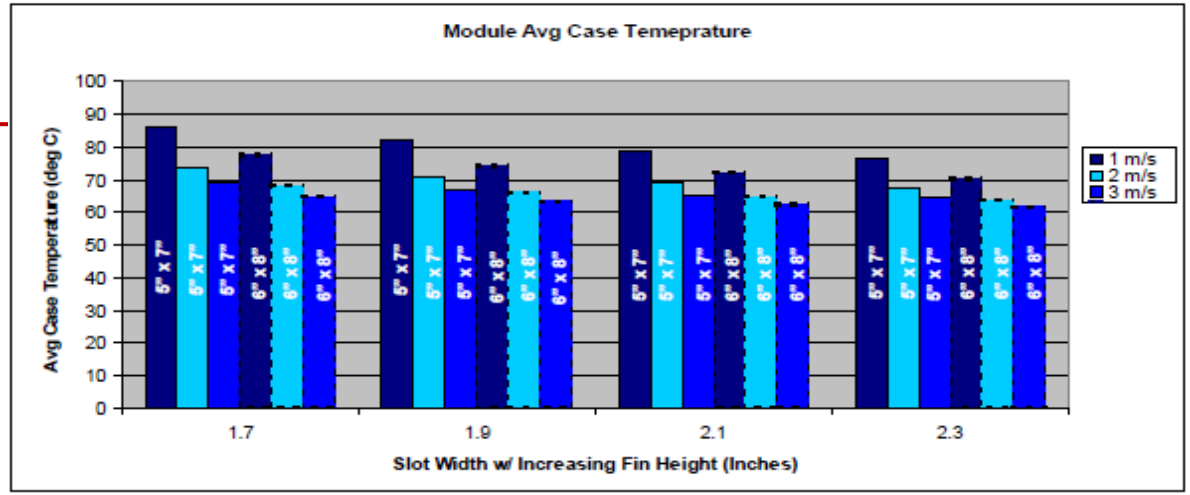
Question 31 - Maximum power allowed

- ≤ 80W

OIF2009.052.00
Drink Barthel
CoreOptics



OIF2009.139.01
Roberto Marcoccia
Opnext



module size: 5 inch x 7 inch
6 inch x 8 inch

Technical challenge 2
Heating issue

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40G DWDM 300pin MSA module
- Size: 5 inch x 7 inch
- Maximum power: ~ 30W

For 100G MSA module ?

- **65W cannot be allowed considering junction temperature of transistor**
- **For 100G MSA module, it is necessary to decrease 35W or less, and target power of LSI should be about 15W**
- **Details will be discussed in next OIF meeting**

Technical challenge 3
Efficiency improvement of VLSI development

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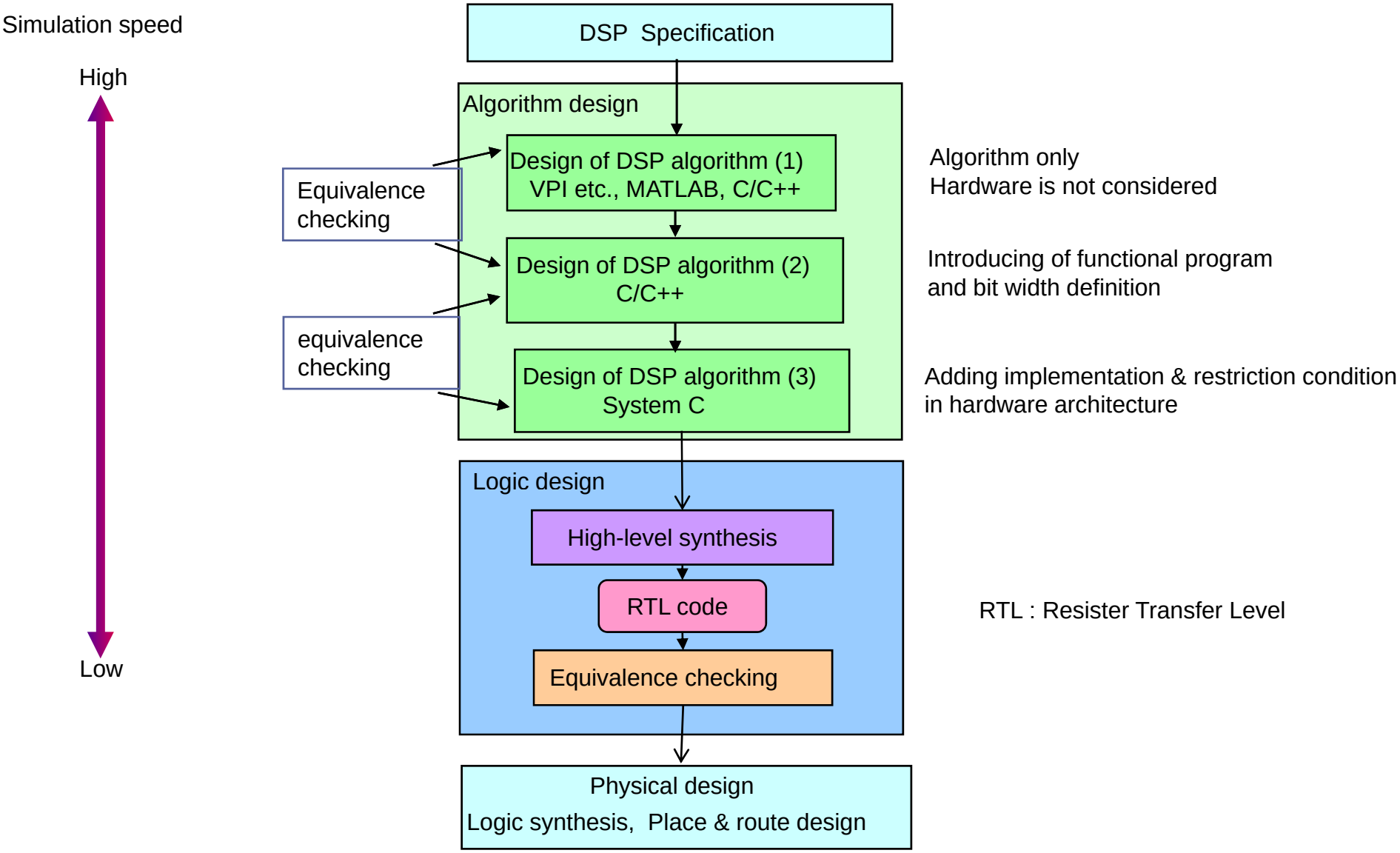

Advantages of High-level Synthesis

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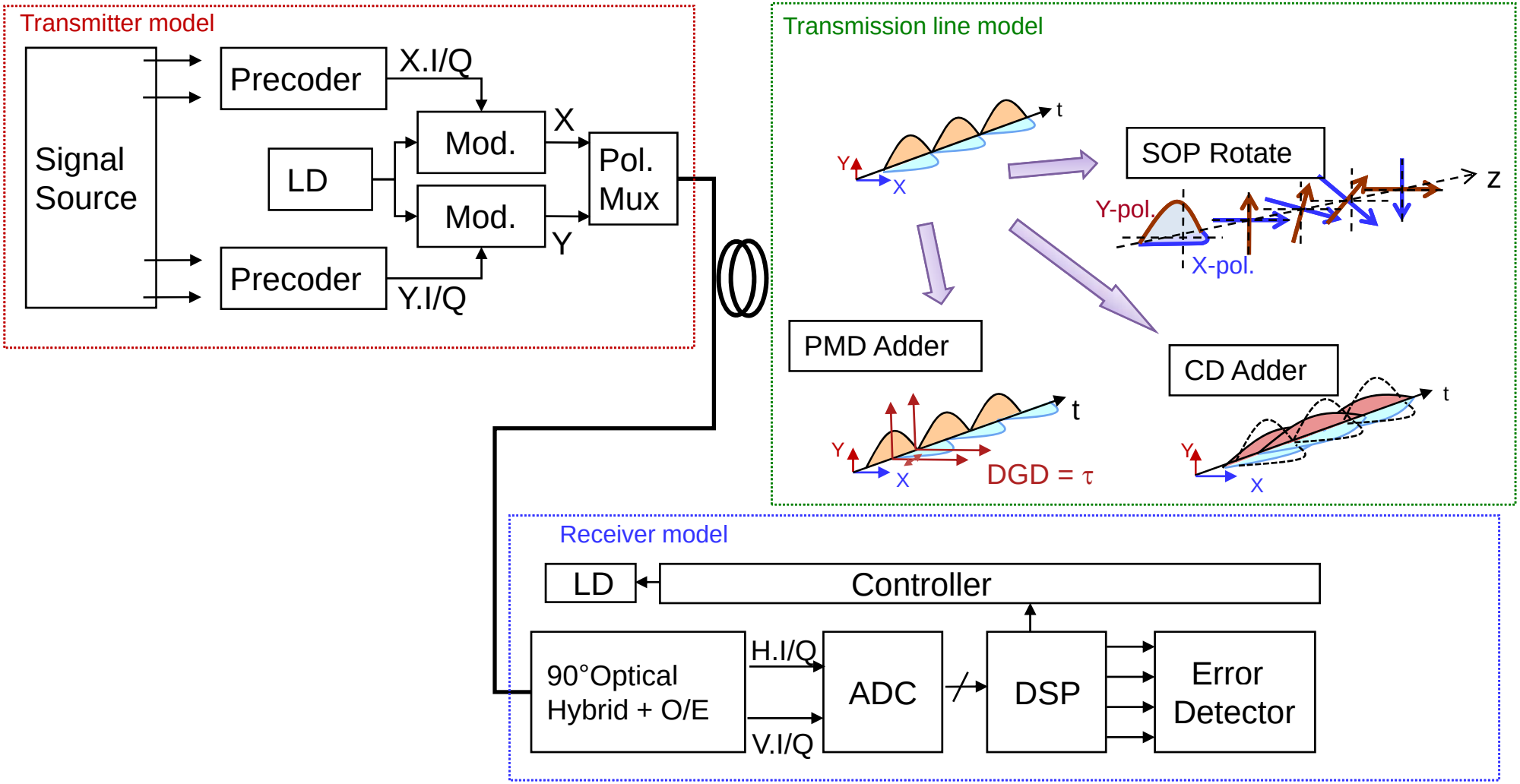
Automated design process that interprets an algorithmic description using C++/System C and creates RTL (Resister Transfer Level) code

- **Shortened design term:** Introducing automatic design at early stage
- **Decrease in design mistake:** Human error is prevented by automated synthesis
- **Expansion of design area:** Better architecture can be decided in consideration of trade-offs because various choices can design/evaluate in a short time
- **Easiness of design:** Decrease of description amount and increase of understanding level by enhancing abstraction level of design

All systems simulator including transmitter, transmission line, and receiver model

- Precise verification of DSP operation with restriction and condition of hardware by using all systems simulation



Design example by using High-level synthesis

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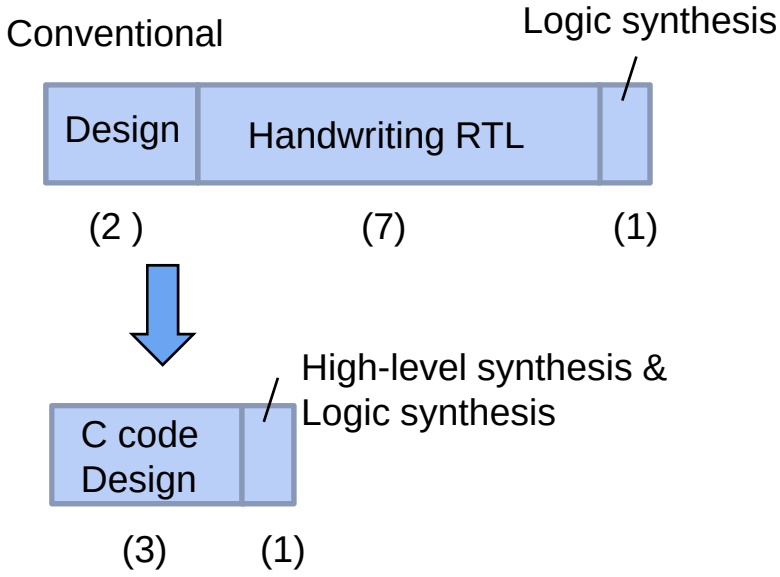
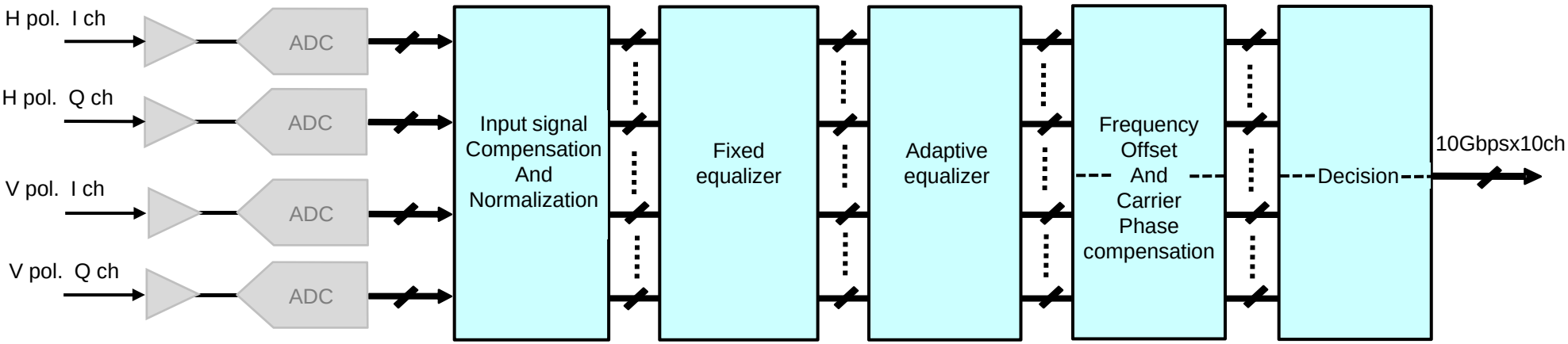
Fixed Equalizer	Line number	Gate count
C model (System C)	3,091	
RTL (High-synthesis)	259,016	6.8M gates x2

Adaptive Equalizer	Line number	Gate count
C model (System C)	328	
RTL(High-synthesis)	42,712	3.4M gates



- Line number of Synthesized RTL increased to 100 times that of C model
- Line number of handwriting RTL increase to about 10 times that of C model
- Gate number by high-level synthesis confirms becoming the same as handwriting RTL

Estimated gate counts of 100G DSP



Total: 26.2 M Gates

Summary

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- 100G DSP can be realize on a realistic gate scale. Necessary to reduce power by half for 5 inch x 7 inch MSA module
- High-level synthesis tool is very effective for development of 100G DSP
- All system simulation is very useful for precise verification of ADC/DSP operation

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