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Enhanced FEC for 40G / 100G

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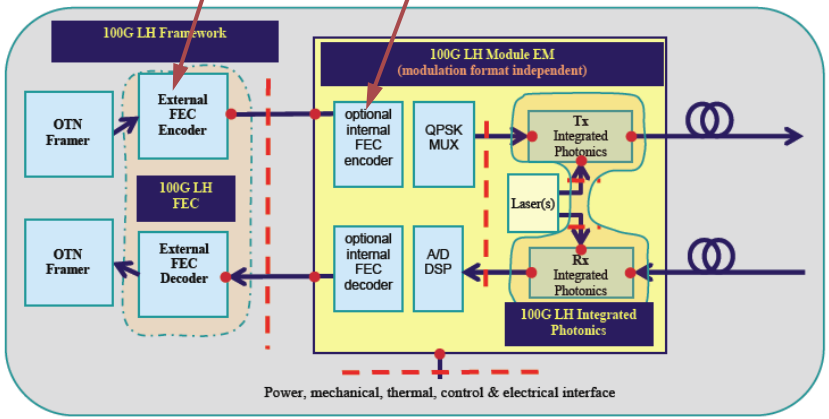
eFEC Issues at 40G / 100G

- Better FEC NECG required for both 40G metro and future 100G deployments
  - Carriers' goal to deploy 40G/100G on networks engineered for 10G
  - Advanced modulation schemes (DQPSK, DP-QPSK) reduce required bandwidth
  - Stronger FEC still required to overcome decrease in OSNR
- OIF: Proceeding with 100G long-haul module study
  - Envisions 100G implementations with high-overhead soft-decision FEC in module
  - Supports 100G OTU4 with 7% FEC / eFEC applied in OTN Framer
  - Issues with availability, power, cost, line rate for 20% SD-FEC
- ITU-T: 100G metro performance requirements not yet clear
  - RS-FEC standardized for short-reach applications
  - No agreement on 100G metro application requirements
- Newly-identified concern re OTN Latency
  - At least 3 contributions to next week's ITU-T SG15 identify OTN latency as an issue
  - One suggests disabling FEC to reduce latency



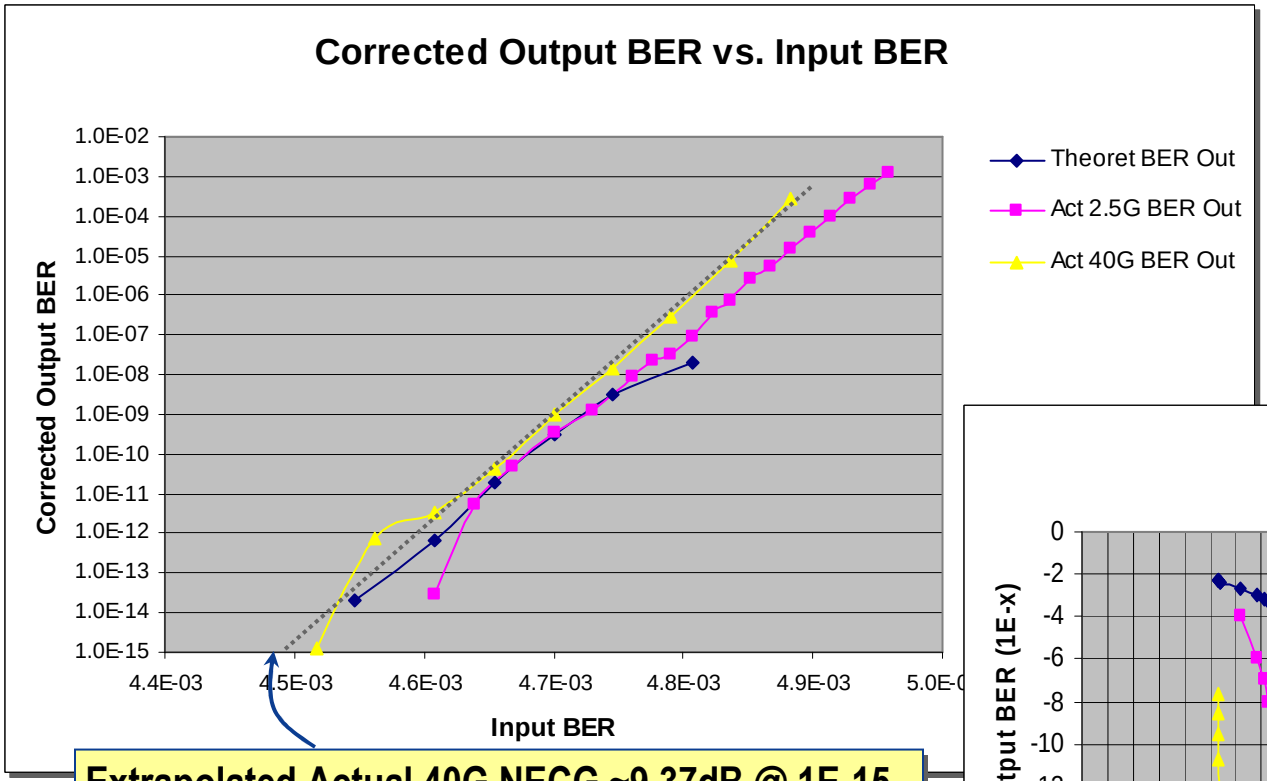
Source: OIF-FD-100G-DWDM-01.0

CI-BCH eFEC Summary

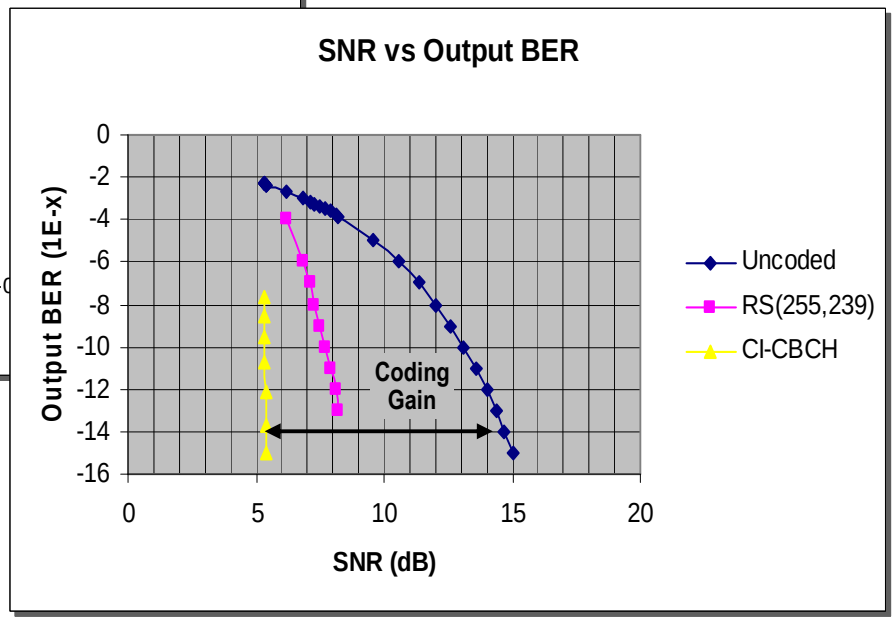
- CI-BCH: Continuously Interleaved BCH enhanced FEC (eFEC)
  - Based on interleaved BCH(1020,988) codewords
  - Continuous interleave **tolerates 1500 consecutive error** burst
  - Delivers **9.35dB NECG** at output BER of 1E-15 with 1Mbit latency (10µs @ 100G)
    - Better NECG than any of the G.975.1 FEC codes at standard 7% overhead
    - With 7% OH, can operate within ITU-T MLD and SFI-S lane rate limits
  - Continuous interleave enables **variable latency decoder** with common encoder
  - Provides **FEC-corrected error feedback** to help optimize RX equalizer / decision circuit
- Low-implementation complexity
  - No Chien search or matrix inversion required (uses algebraic equation solver)
  - Extremely low flaring floor eliminates need for flaring correction (no erasure decoding)
- Even higher NECG performance possible with CI-BCH:
  - Utilize higher-overhead rates for CI-BCH implemented in module
  - Small improvement possible using stronger BCH polynomial or higher latency

CI-BCH NECG Performance

- Theoretical and actual results @ 40G OTU3



Extrapolated Actual 40G NECG ~9.37dB @ 1E-15

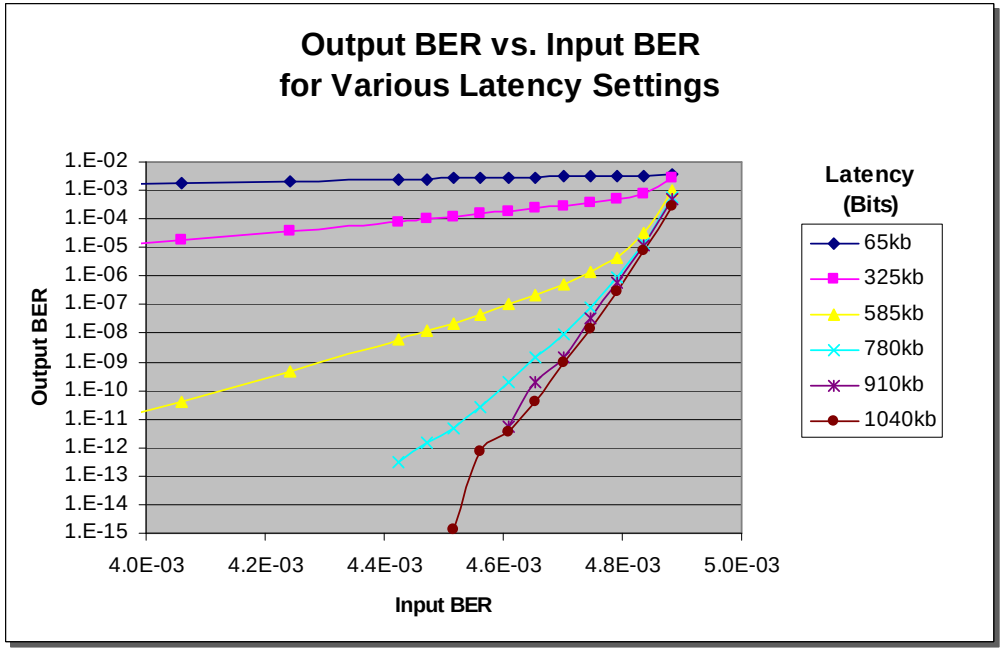


Note: NECG ~9.35dB for corrected BER = 1E-15 @ input BER = 4.4E-03
NECG ~9.40dB for corrected BER = 1E-15 @ input BER = 4.6E-03

Encoding / Decoding Latency

- Carriers expressing concern regarding latency over OTN Networks
  - ITU-T SG15 C-412 (Verizon) and C-472 (China Telecom, CMCC, China Unicom):
    - Identify latency-sensitive applications; Propose latency measurement using OTN OH
  - ITU-T SG15 C-452 (Huawei):
    - Cites latency-sensitive Fibre Chan; Notes latency can be reduced by disabling FEC
- CI-BCH Encoder & Decoder Latency:
  - Encoder: < 10,000 bits
  - Decoder: ~1,000,000 bits
  - **Decoder configurable to provide lower latency at expense of NECG**

Latency (bits)	Latency (µs)		NECG (dB)
	OTU3	OTU4	
65,000	1.5	0.6	4.3
325,000	7.6	2.9	7.7
585,000	13.6	5.2	9.0
780,000	18.2	7.0	9.3
1,040,000	24.2	9.3	9.35



Low Implementation Complexity & Size

- Resources utilized for 40G CI-BCH FPGA implementation (relative to available LX330T resources)
  - Slices: 20,976 (40.5% of 51,840 available slices)
  - Flip Flops: 55,419 (26.7% of 207,360 available FF)
  - Block RAMs: 84 (25.9% of 324 available block RAMs)
  - DSP blocks: 0
- Estimated resources for 100G CI-BCH FPGA-based implementation (relative to available resources in EP4S100G5)
  - LUTs: 178,480 (42% of 424,960 available LUTs)
  - Registers: 138,570 (32% of 424,960 available registers)
  - Memory bits: 6.8 Mbits (32% of available 21.2 Mbits)
  - DSP blocks: 0
- Significantly smaller than popular, lower-performing G.975.1 eFEC codes

Extending CI-BCH to Higher Gain

- Improved Performance possible with:
  - Higher overhead ratio
  - Stronger FEC polynomial (longer codeword / higher latency)
  - Higher decode latency (Decode more codewords per corrected bit; Diminishing returns)
- Examples:

eFEC Code	FEC Overhead	Latency	NECG @1E-15
CI-BCH-3	6.7% (std)	1Mbit	9.35 dB
	12%		9.9 dB
	20%		10.3 dB
CI-BCH-4	6.7% (std)	8Mbit	9.55 dB
	12%		10.0 dB
	20%		10.5 dB

Where:

- CI-BCH-3 is 3-error correcting BCH(1020,988)
- CI-BCH-4 is 4-error correcting BCH

Summary

- Carriers have a goal to deploy 40G & 100G transmission rates on optical networks engineered to 10G design rules
- Advanced modulation schemes, EDC and better eFEC technology required to achieve this goal
- Better eFEC offers the best "bang for the buck" but…
  - High overhead FEC cannot be delivered across module interfaces limited to ~11G lane rates
  - Soft-decision FEC solutions are power-hungry, not yet available, and expected to be costly
  - For metro applications, unclear that power and cost of SD-FEC is warranted
  - Time-sensitive financial transactions require low latency transmission
- Hard-decision CI-BCH eFEC offers improved NECG and lower latency at reasonable power, low complexity and low cost
  - 7% CI-BCH eFEC delivers better NECG than any current 7% OH G.975.1 eFEC
  - CI-BCH eFEC can be register-configured to tradeoff latency vs. NECG
  - HD CI-BCH eFEC can achieve NECG as high as 10.5dB at 20% OH rate

25 YEARS OF INNOVATION

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Thank You!

Questions?

ECOC, Sep-2009

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Backup Slides

40G & 100G Deployment

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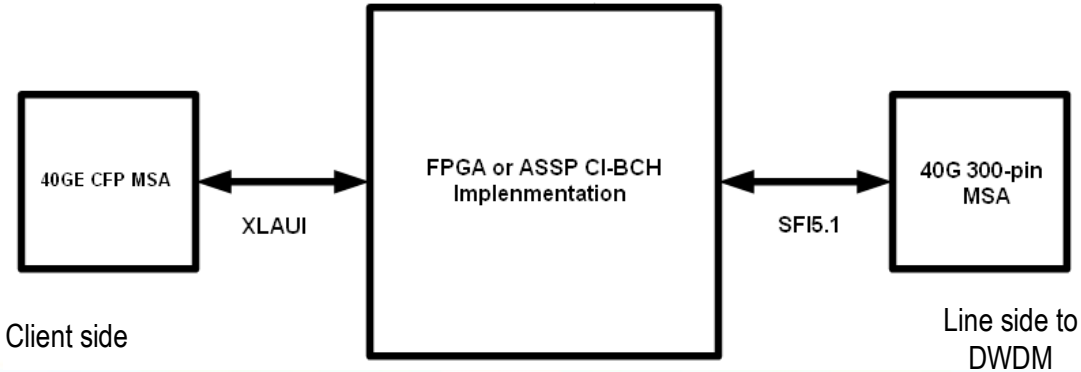
Implement High-efficiency CI-BCH for 40G

- Bandwidth is growing rapidly, 40G starts to get off the ground first in operator DWDM networks and enters into Metro ROADM space.
- 40G market moving towards MSA module deployments for sustainable business model with the evolution among different modulations schemes.
  - Volume leaders transitioning from ODB to DPSK now
  - DQPSK expected to dominate for next couple years.
  - DP-QPSK is emerging as another variant which takes advantage of 10G chipsets
- 7% OH eFEC can be implemented on both client-side CFP and line-side 300-pin MSA modules with well-specified interfaces.
  - Isolate variations in Optics and take advantage of the FEC feedback.



High-efficiency CI-BCH for 100G Long-haul

- Clear need for 100G; Industry standardizing 100G solutions
  - DP-QPSK with coherent receiver selected by OIF for long-haul; Leverage ~28G chipset
  - IEEE P802.3ba 40G/100G effort inspire the progress of client-side MSA module group.
- Advanced EDC/DSP and better eFEC are enabling technologies to help close the performance "gap".
  - Take advantage of FEC offset feedback.
  - Leverage the ~28G Electronics
  - Need very fast ADC mixed signal ASIC.