Reality check: Implementation of Soft-Decision FEC in a DSP LSI

September 20th, 2009
ECOC2009, Vienna

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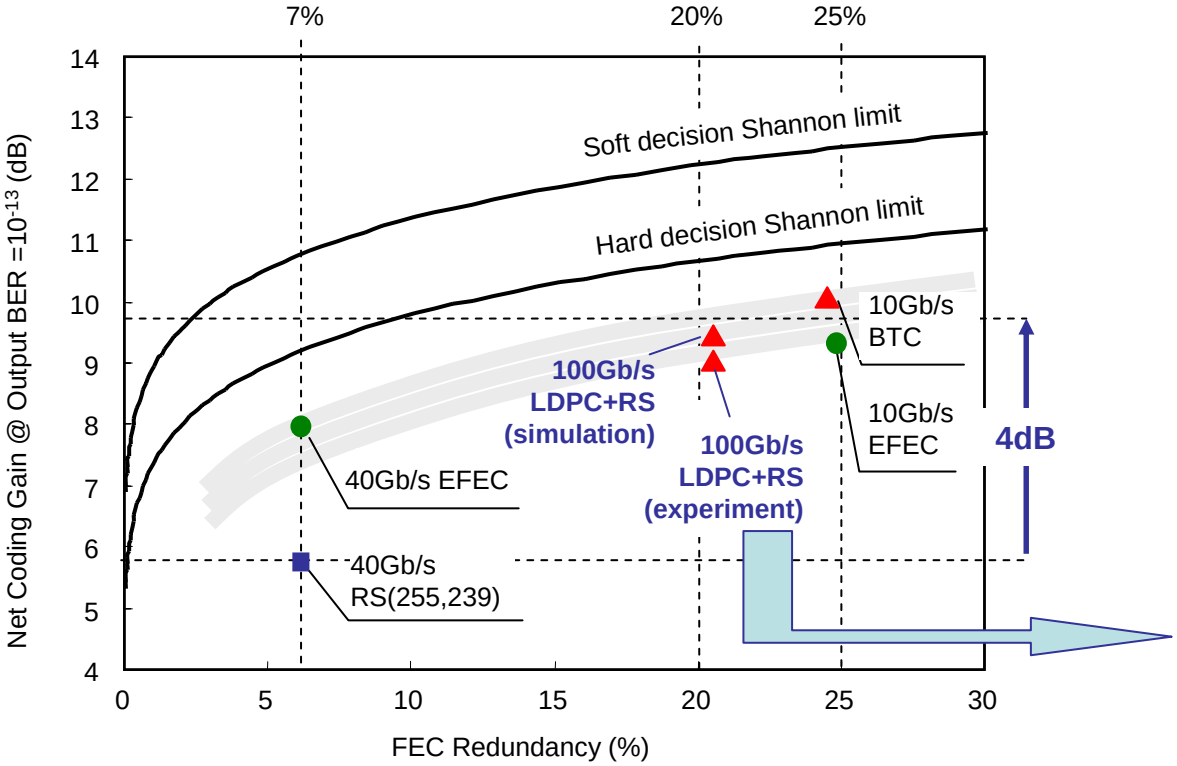
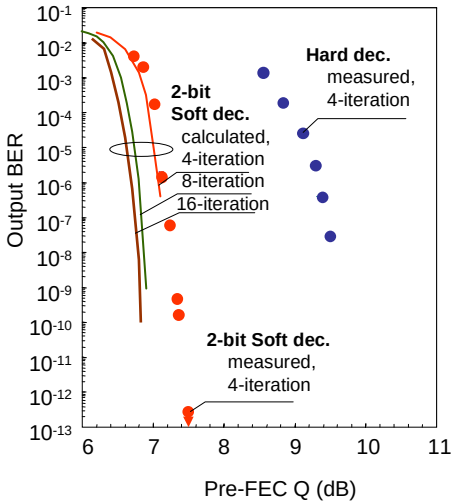
Expectation for SD-FEC

- For 100G FEC;
  At least 4dB (=10log(100/40)) better correction capability than for 40Gbps is mandatory
  RS(255,239) = 6.9% redundancy → NCG = 5.8 dB (@10^{-13})
  5.8dB + 4dB = 9.8dB is required
- >20% redundancy with soft decision decoding would be necessary
  → >125Gb/s for OTU4V



T. Mizuochi, et al., PTL, vol. 21, 1302, 2009.
T. Mizuochi, et al., ECOC2009, Tu.5.4, Symposium.



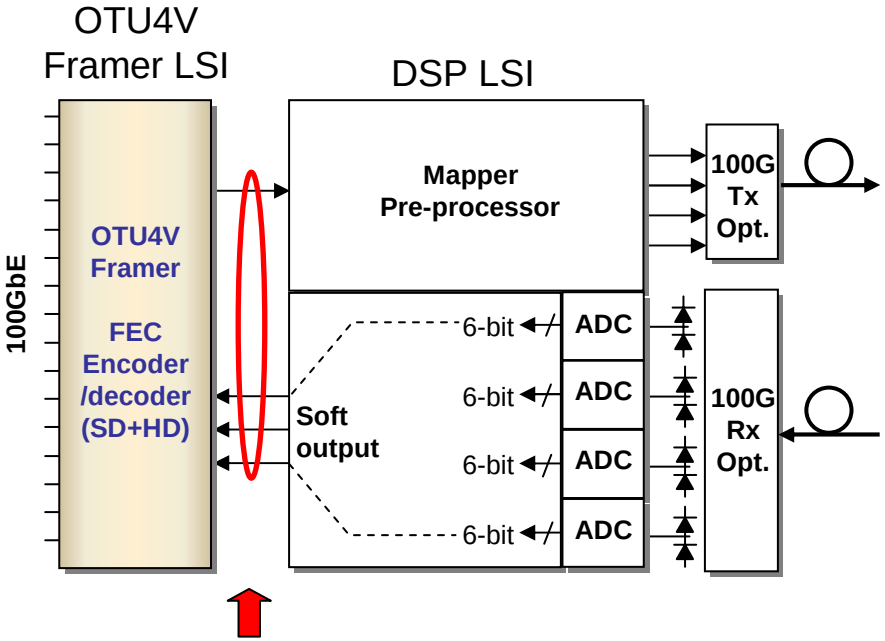
➢ To achieve NCG of > 10dB, SD-FEC is a promising technology for 100G systems.
How can we realize SD-FEC in a realistic LSI ? We check the implementation issues.

Issue 1: LSI Partitioning

- Soft decision with >3 bits is required for nearly ideal performance
- But, extremely complicated high speed I/O or circuit size

ex) Tx: 125G → I/Q mod + Pol-Mux. → 125G Opt. Signal
Rx: 125G Opt. Signal → 4x 6-bit ADC → 3-bit 125G out
→ 125G Soft-decision FEC

125G x 4 = 500G I/O



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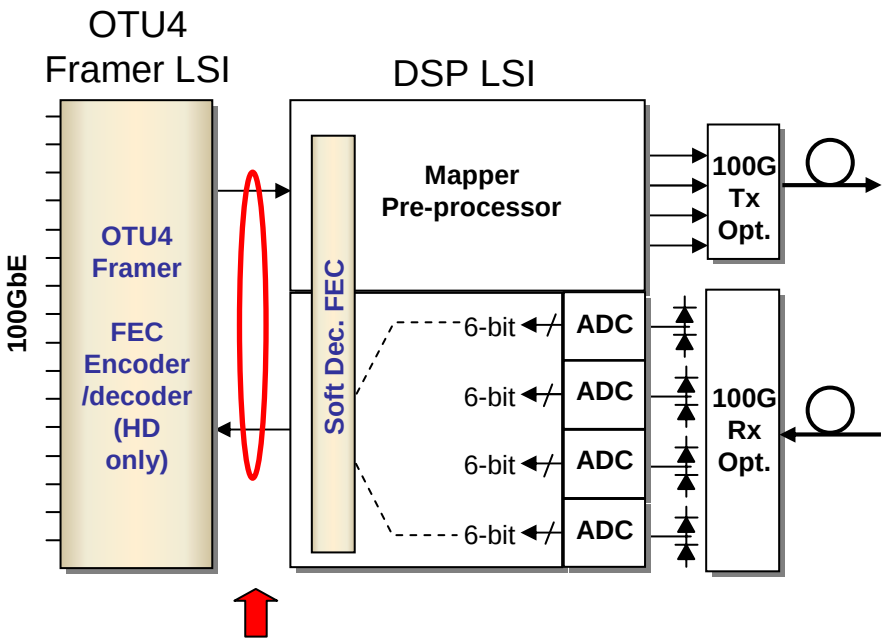


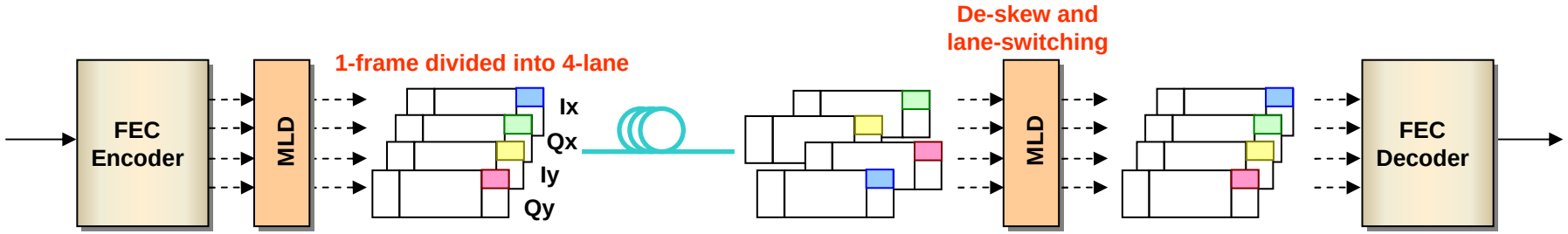
112G x 2 = 224G

➢ Deployment of SD-FEC in a DSP LSI is one of the solution to realize an optical transceiver.

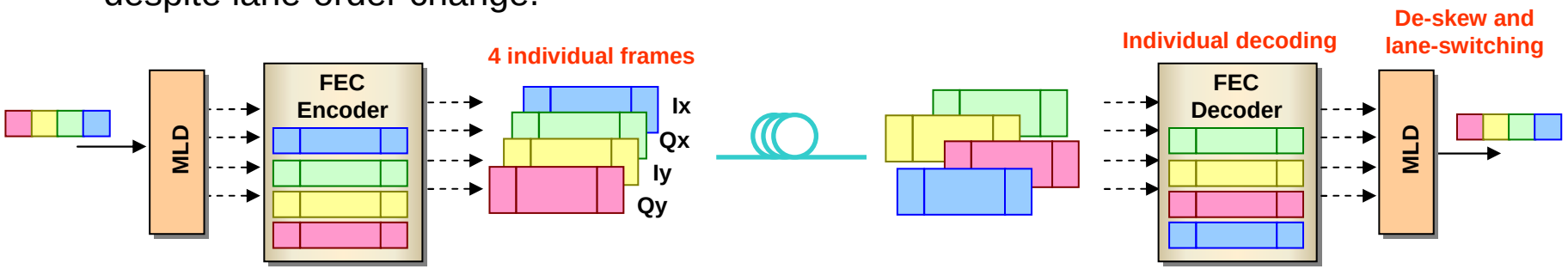
Issue 2: Multi-lane Distribution

- Generally, FEC frame format should be re-aligned correctly before SD-FEC decoder.
- But, Sub-bit skew and lane-switching are inevitable in a multi-lane transmission.
  ex) DP-QPSK: 4-lane of (Ix, Qx, Iy, Qy) transmitted in an optical fiber.
  → Skew and lane-switching between two polarization caused by PMD.
  Lane-switching between I-ch and Q-ch caused by cycle-slips.

➢ MLD-like lane re-alignment: Use OTU-OH (MFAS, etc.), easy to implement.



➢ Individual FEC frame: FEC frame for each transmission lane, properly decoding despite lane-order change.

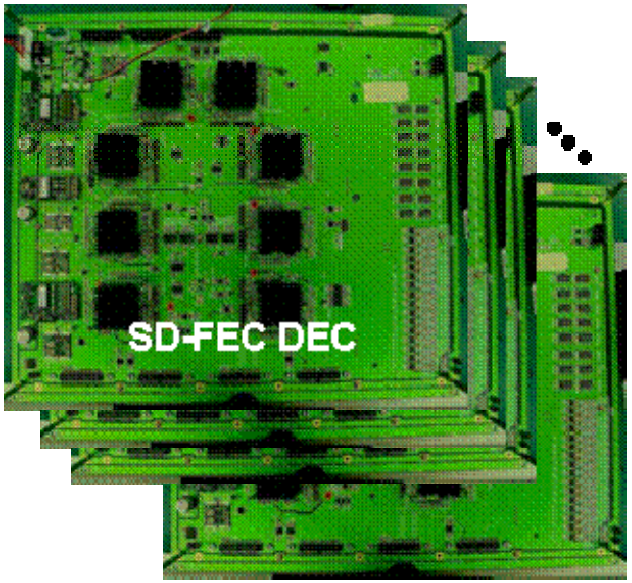


➢ Optimum choice of combination of MLD-like lane distribution and FEC frame structure is important design parameter.

Issue 3: Toward One-chip LSI

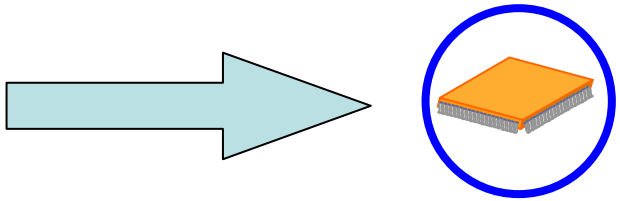
- FPGA based SD-FEC emulator
  90nm CMOS, 2 Mgates/fpga for 10 Gb/s throughput
  LDPC, 2-bit soft decision, 4-iteration → 16 Mgates
- 100G SD-FEC: 16 x 10 = 160 Mgates

T. Mizuochi, et al., ECOC2009, Tu.5.4, Symposium.



FPGA Emulator

1. Min-sum based algorithm
2. Optimization of coding parameter
3. Optimization of parallel expansion and pipe-line insertion
4. Progress of process technology (At least, < 45nm is preferable)



➢ To apply our developing algorithm based on LDPC, one-chip LSI for 100G is expected to emerge soon.

Conclusion

- To achieve NCG of > 10 dB using soft decision FEC, realistic implementation issues are discussed.
- In order to relax the design of circuit board, deployment of SD-FEC in a DSP LSI is one of the solutions to realize an optical transceiver.
  (OTU4V framer + HD-FEC + SD-FEC) + DSP
  → (OTU4 framer + HD-FEC) + (DSP + SD-FEC)
- Considering the lane-distribution in the optical transmission, we must take care of the skew and lane-switching.
  MLD-like operation before SD-FEC decoder
  Individual FEC frame to each transmission lane
- One-chip LSI of SD-FEC is expected to appear soon.
  Establishment of more sophisticated algorithm and progress of CMOS process brings 100G LSI having NCG of >10dB. It may emerge in 2010~2011.

This work was in part supported by "Lambda Utility Project" of the National Institute of Information and Communications Technology (NICT) of Japan, and "Digital Coherent Optical Transceiver Technologies" by the Ministry of Internal Affairs and Communications (MIC) of Japan