CoreOptics
Enabling Open Tolerant Networks

System level trade-offs in the design of a coherent receiver

Chris Fludger
ECOC2009

Driver

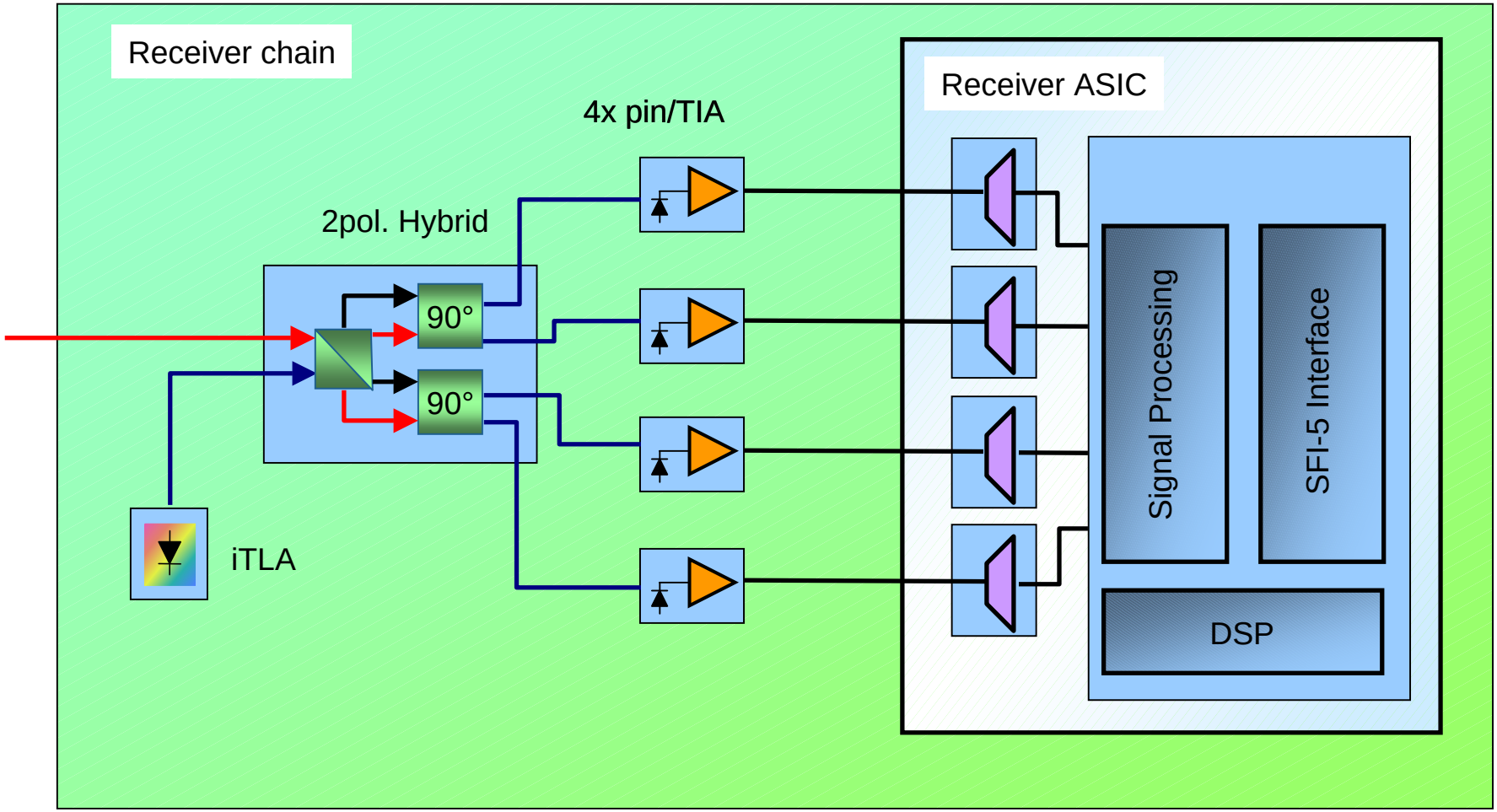
- Driver is always cost
  - CAPEX
    - More data capacity for less money (Gbits/Euro)
  - OPEX
    - less power dissipation
    - simplify maintainence costs

WHAT CAN YOU DO IN ELECTRONICS TO REDUCE COST ??

System level trade-offs : Possibilities

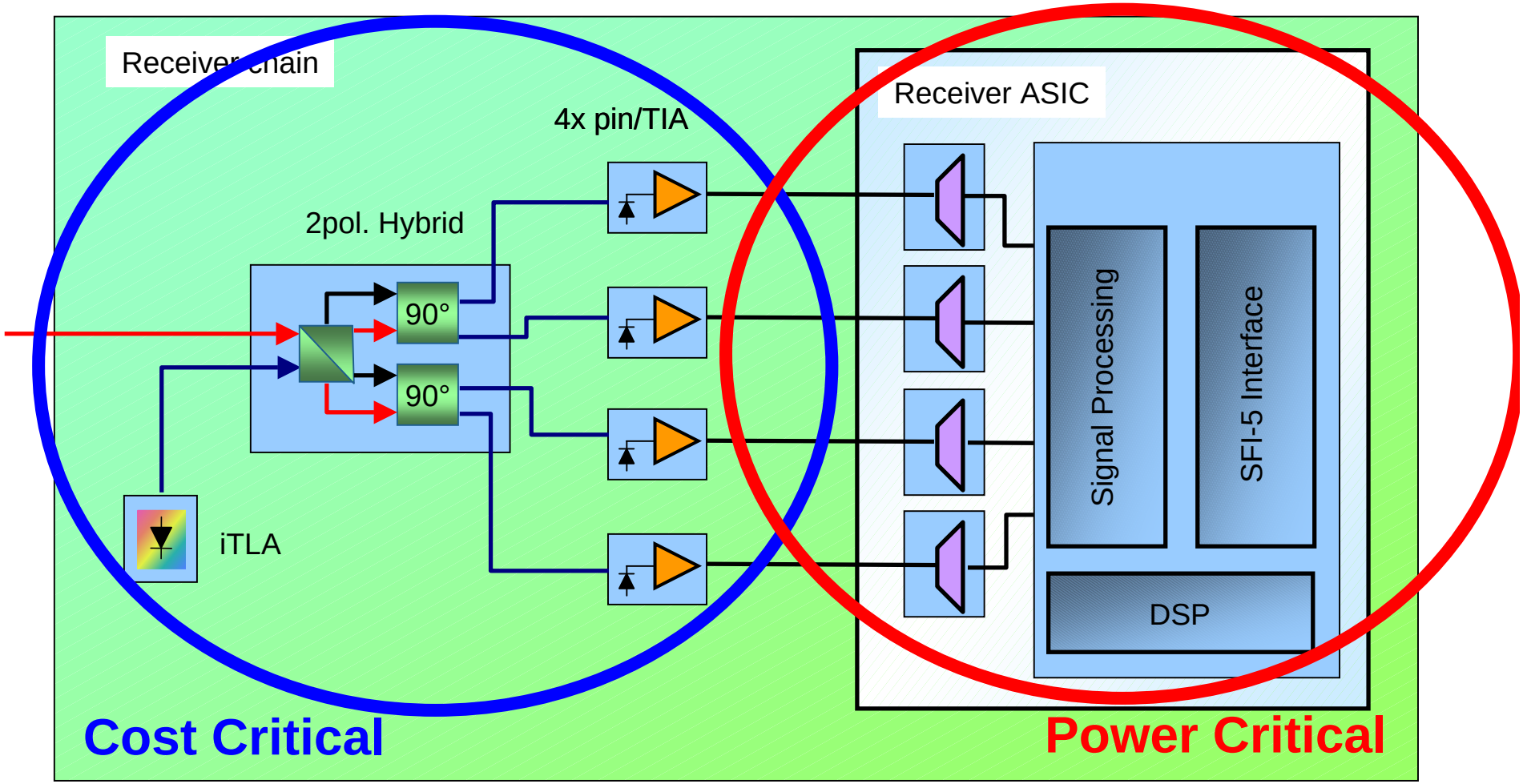
- Equaliser for CD mitigation
  - Remove DCMs / Amplifiers (CAPEX)
  - More CD reduces XPM from other channels
- Equaliser for PMD mitigation
  - Bad fibre can be used
- Removal of wavelength demux filters
- Non-linear compensation : Optical field is detected
  - Intra-channel
  - Inter-channel
- Channel parameter estimation
  - Measure CD / DGD / Polarisation variations

Receiver block diagram



Building blocks are common to 40/100G CP-QPSK / OFDM

Receiver block diagram

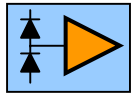


Building blocks are common to 40/100G CP-QPSK / n-QAM / OFDM

Cost Critical trade-offs

- Optical components tend to be expensive

- Balanced receivers



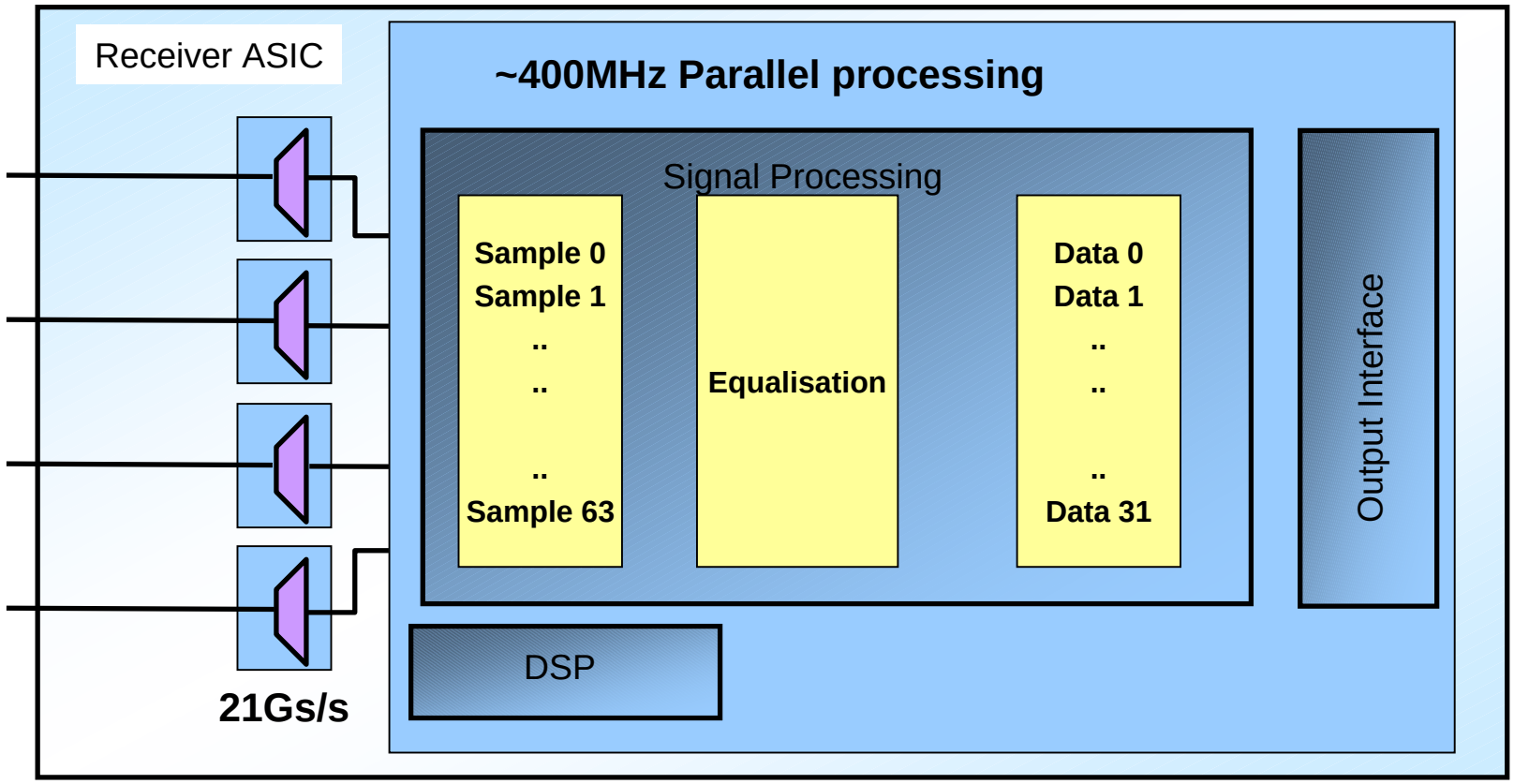
  - Better rejection of common-mode noise
  - Higher sensitivity / dynamic range
  - Expensive

- Shared Tx/Rx laser

  - Reduced cost
  - Transmit and receive wavelength must be the same
  - Reduced output power

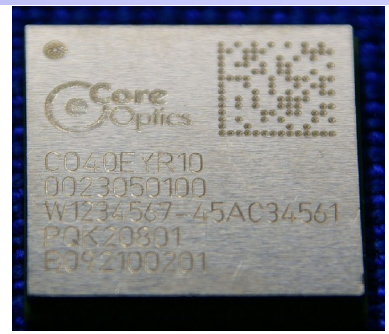
- Integration can drive the cost down
  - e.g. Hybrids and photo-detectors

Power Critical



- **Once the signal is digitized, CMOS technology can process the data efficiently in parallel.**

Power Critical trade-offs



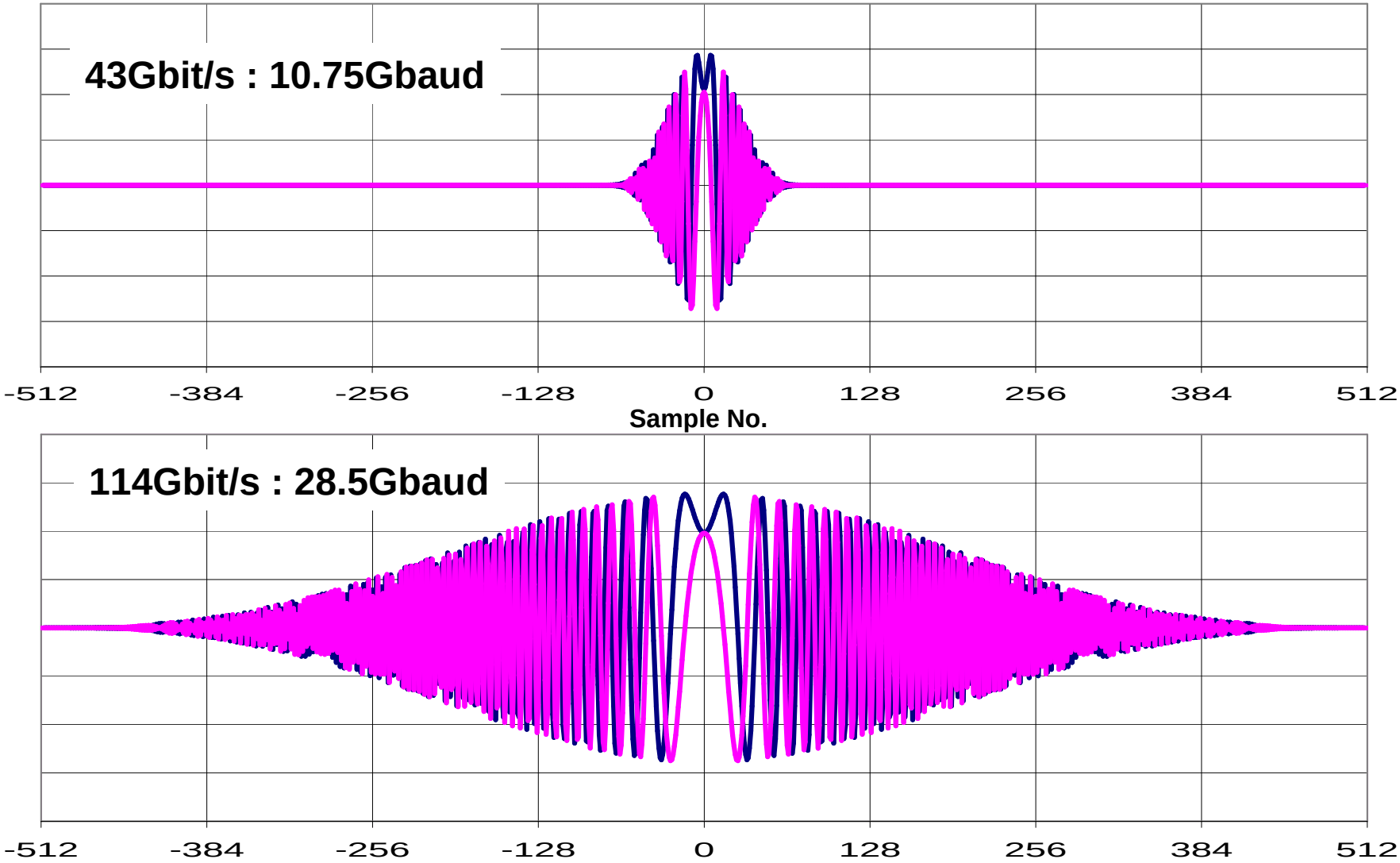
- General
  - Fixed value multiplication is good ✓
    - e.g. FFT or other transforms
  - Fixed value tables are good ✓
  - Running a technology (45/65nm) at high frequencies increases gate count and power dissipation ✗
  - High-speed Input/Output ports should be minimised ✗
- Control loops e.g. filter update
  - Latency can be a problem for feedback loops ✗
  - Feed-forward schemes are possible ✓
- Equalisation
  - CD Filter length increases with baud-rate^2 ✗
  - Frequency domain computation is cheap ✓
    - Required precision increases with FFT size ✗

Challenges for 100G (28Gbaud)

- Low cost optical components

- Power dissipation for ASICs
  - CMOS processors must do more in parallel
  - Symbols to be processed per clock cycle increases
  - Large filters for CD / PMD
  - CD scales as bitrate^2, PMD as bitrate
  - Polarisation tracking requirements is static

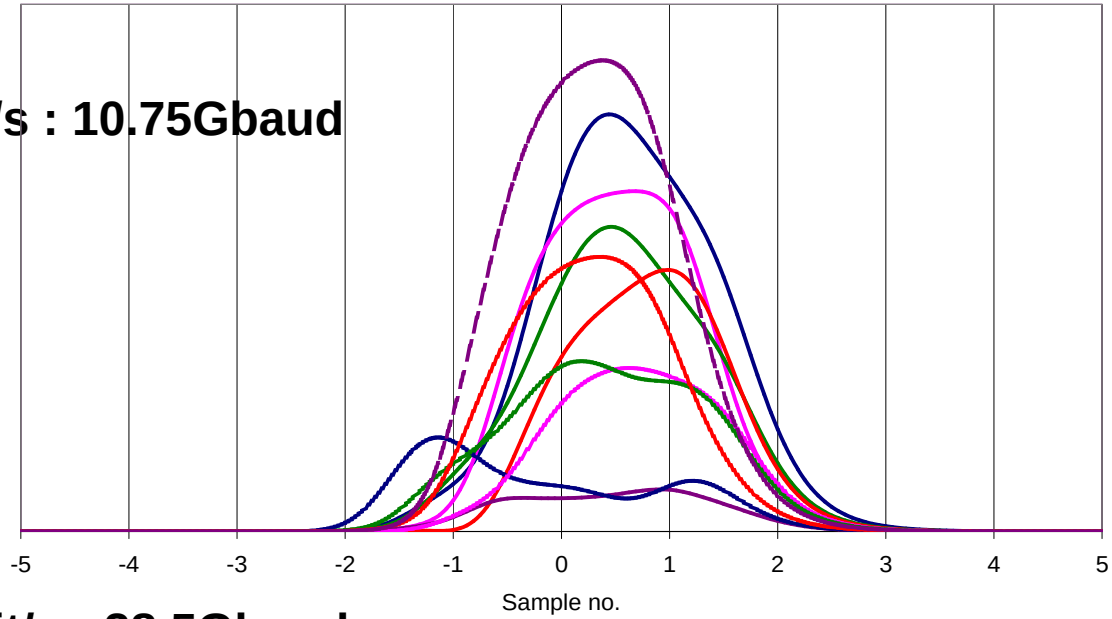
Chromatic Dispersion : 2000 km SMF



Impulse response is ~7 times longer at 28Gbaud

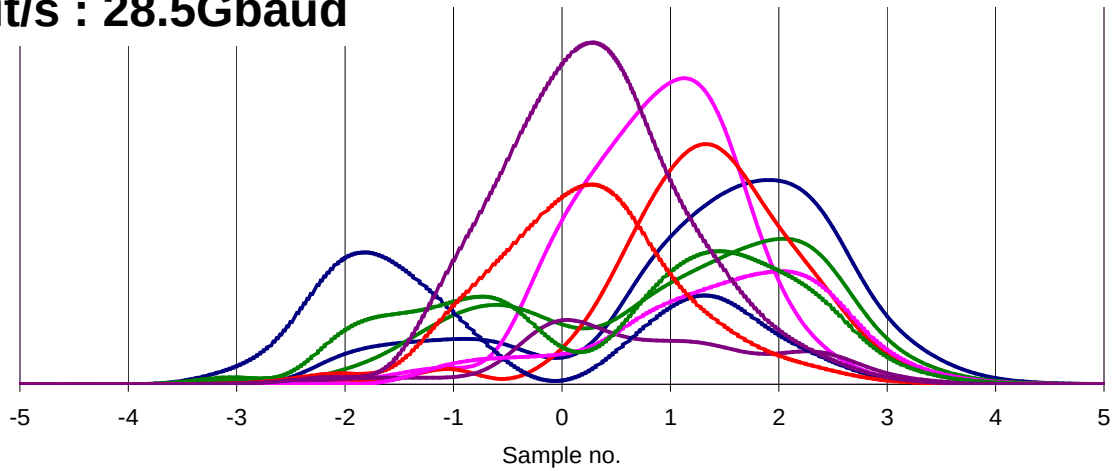
PMD and polarisation tracking

43Gbit/s : 10.75Gbaud



35 ps mean PMD

114Gbit/s : 28.5Gbaud



Impulse response is ~2.5 times longer at 28Gbaud

Rate of Polarisation change is the same

Challenges for 100G (28Gbaud)

- Clock recovery
  - Jitter tolerance masks are very stringent
  - Clock recovery must work with high dispersion and distortion

- OSNR limitation
  - Raman amplifiers are expensive
  - Higher launch powers required
    - Robust against non-linearities
  - FEC increases power dissipation and line-rate

Conclusions

- The driver for Coherent receivers is cost reduction
- Efficient algorithms can be designed for parallel processing
- Challenges for 100G
  - cost of optical components
  - power dissipation of signal processing