ECOC 2009
Workshop '*DSP & FEC: towards the Shannon limit*'

Future perspectives of CMOS technology for coherent receivers

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Outline

- **CMOS Enables New Signaling & DSP**
- **Example : 46Gb/s DP-QPSK Rx ASIC**
- **Scaling to Higher Capacity**
- **Concluding Remarks**

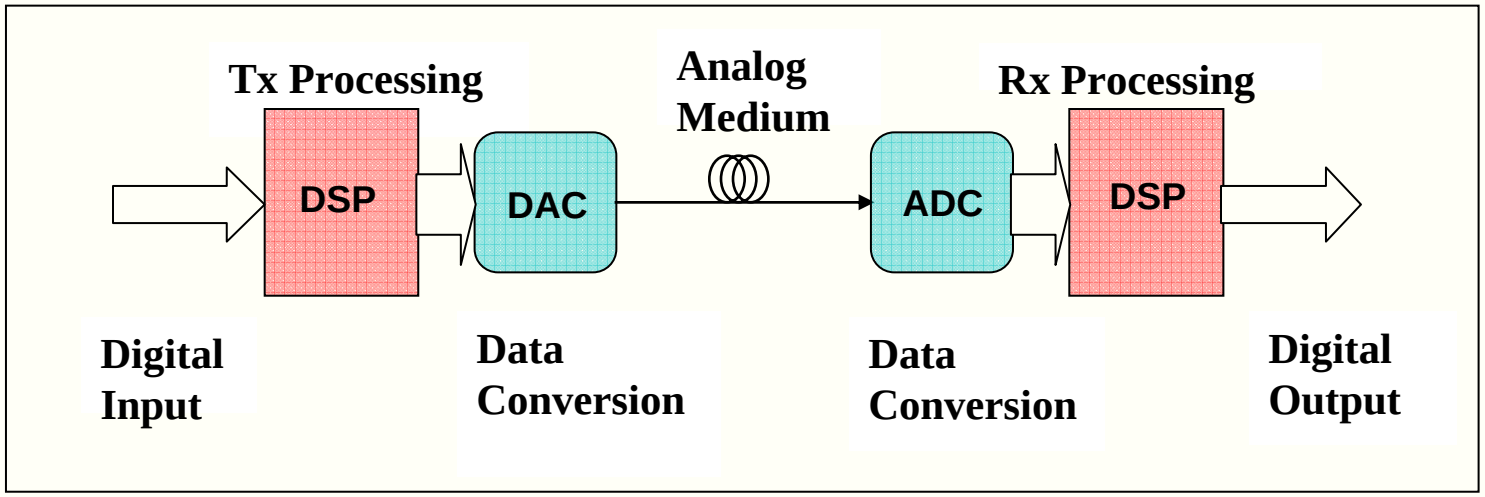
Technology Outlook

High Volume Manufacturing	2008	2010	2012	2014	2016	2018	2020	2022
Technology Node (nm)	45	32	22	16	11	8	6	4
Integration Capacity (BT)	8	16	32	64	128	256	512	1024
Delay Scaling	>0.7			~1?				
Energy Scaling	~0.5			>0.5				
Transistors	Planar			3G, FinFET				
Variability	High			Extreme				
ILD	~3			towards 2				
RC Delay	1	1	1	1	1	1	1	1
Metal Layers	8-9	0.5 to 1 Layer per generation						

Source: Intel

Digital Signal Processing:

High-Speed Data Converters and DSP



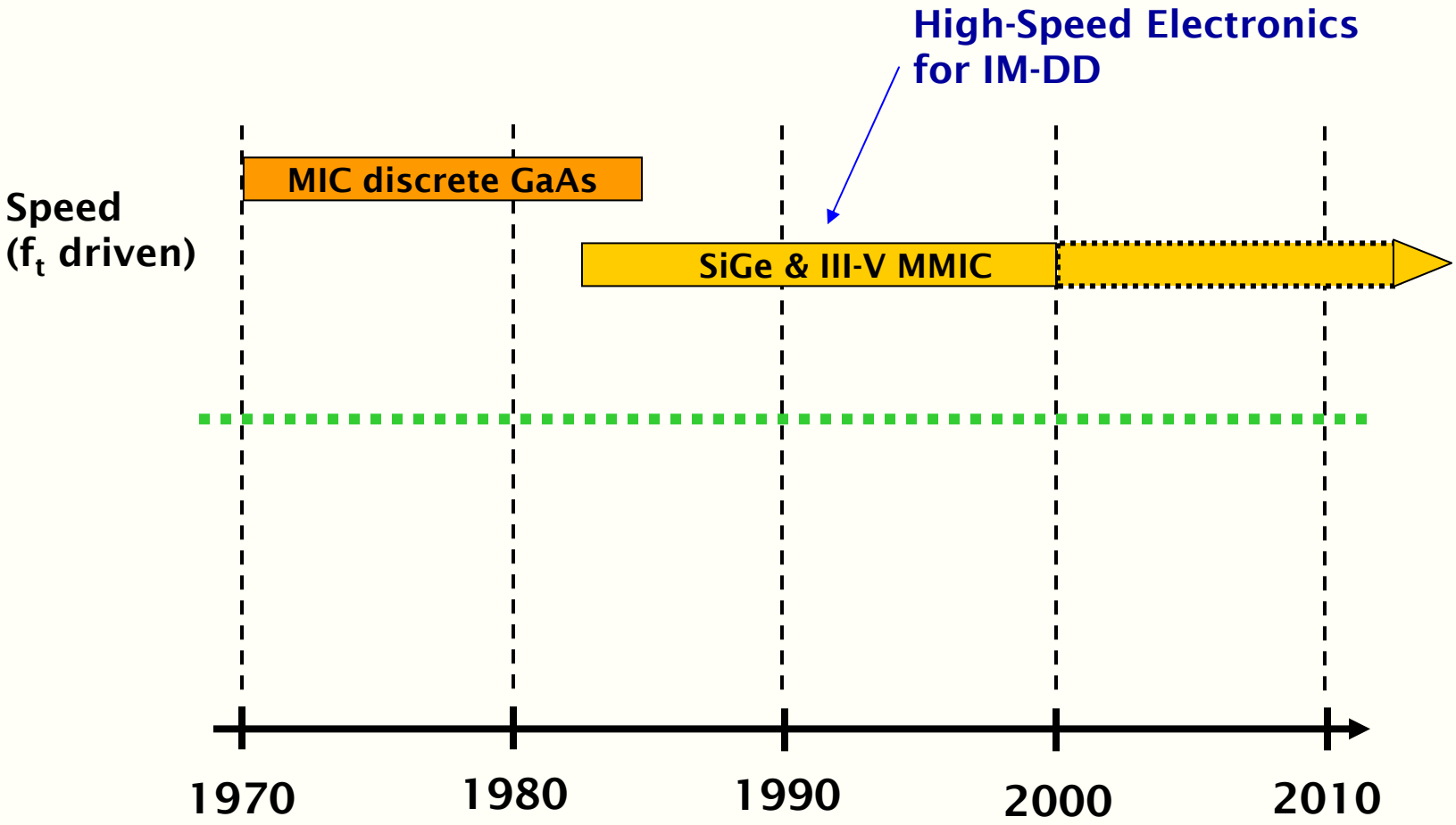
Compensation at Tx, Rx, or both

High-Speed Data Converters to Create / Receive High-Speed Signals

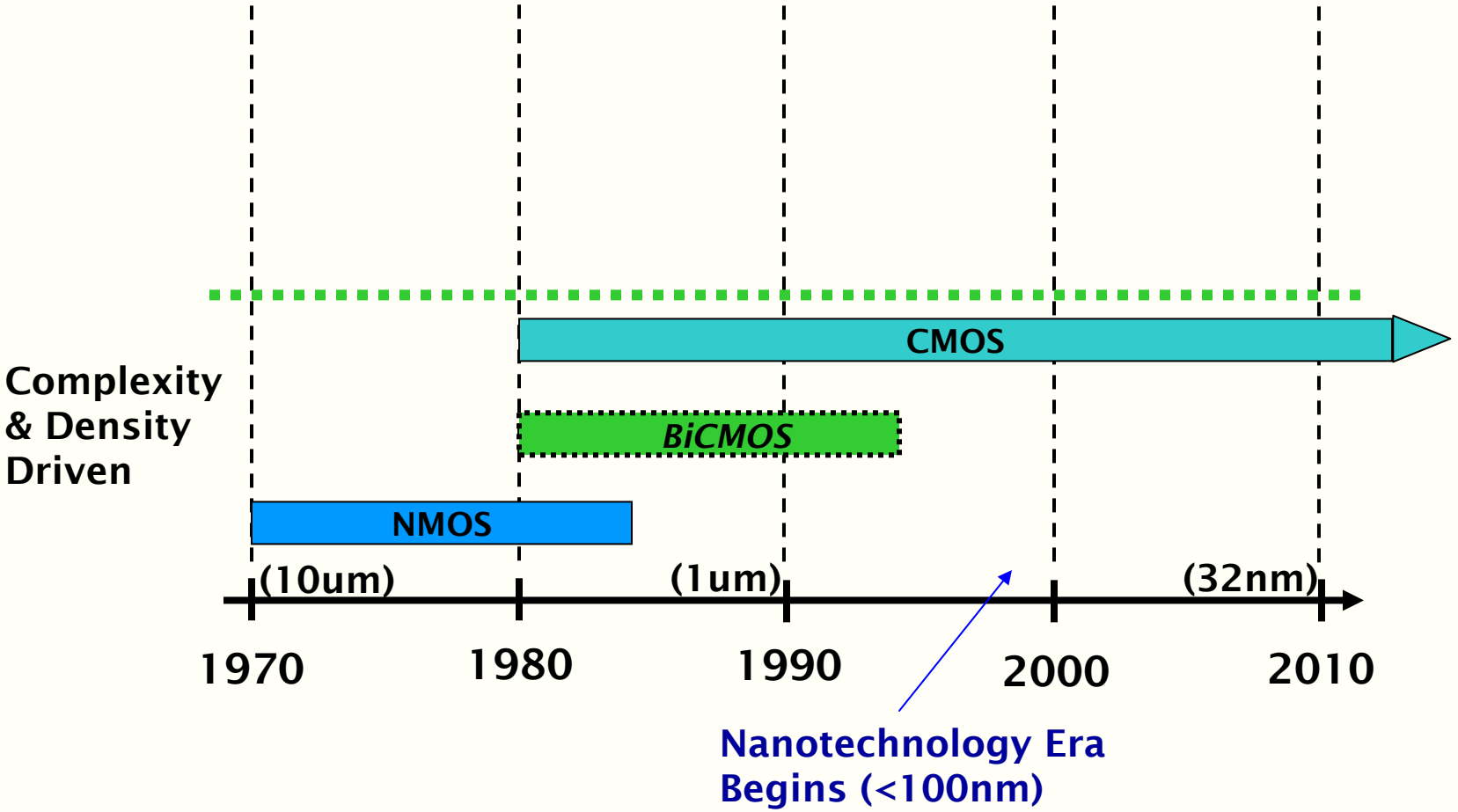
Digital Logic to do all else – eg correct for channel and electro-optic impairments

Need high-speed electronics AND lots of logic gates…

The CMOS Juggernaut

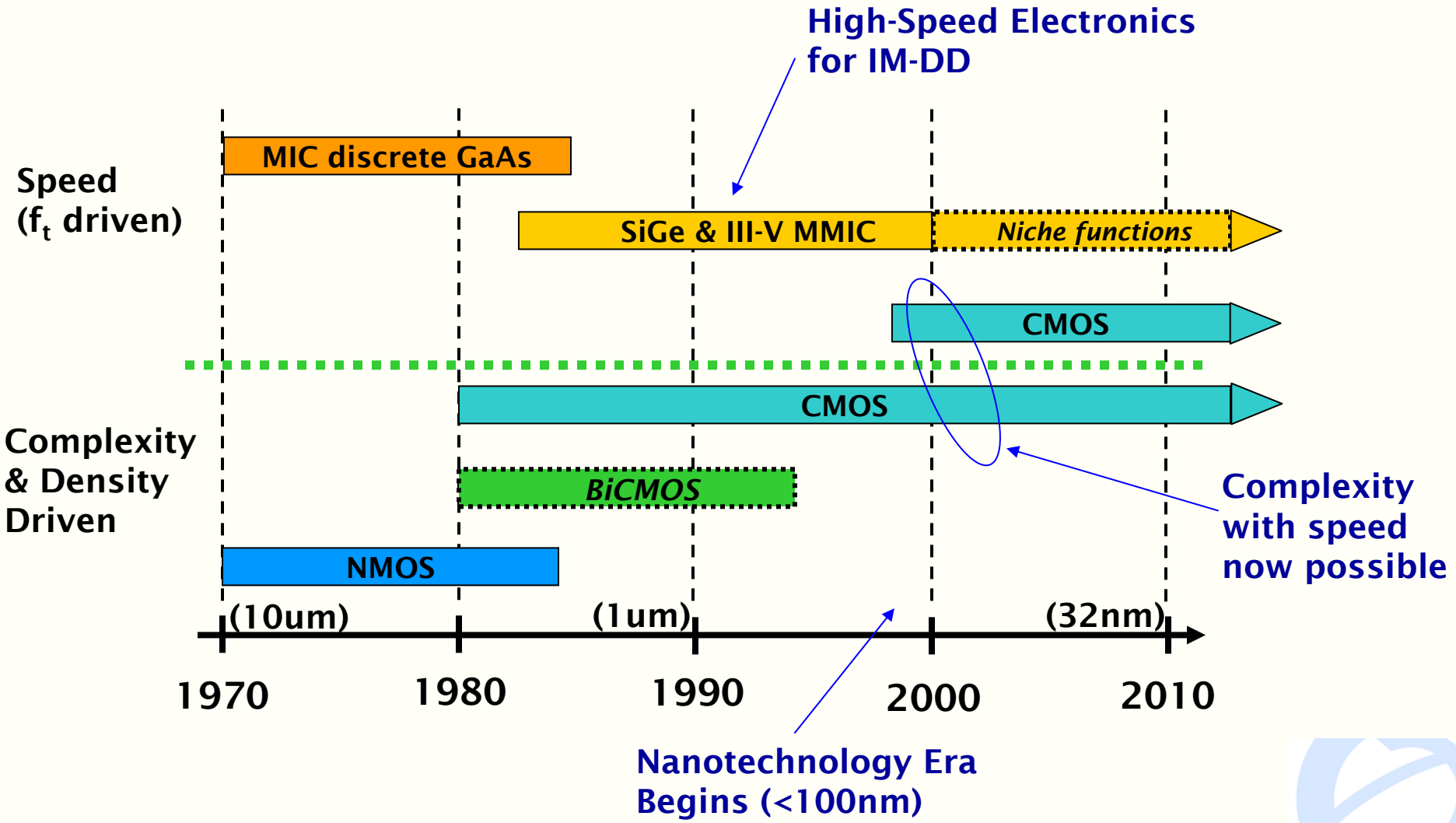


The CMOS Juggernaut

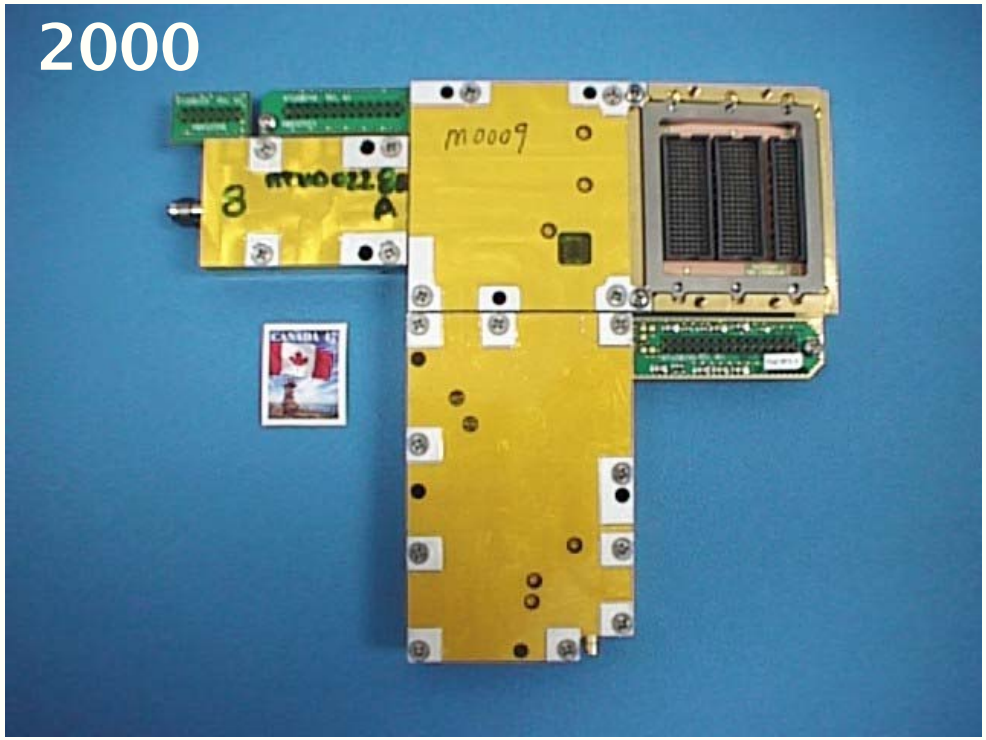


The CMOS Juggernaut –

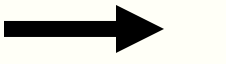
if it ain't CMOS, it ain't on the roadmap…



In less than a decade …



2008

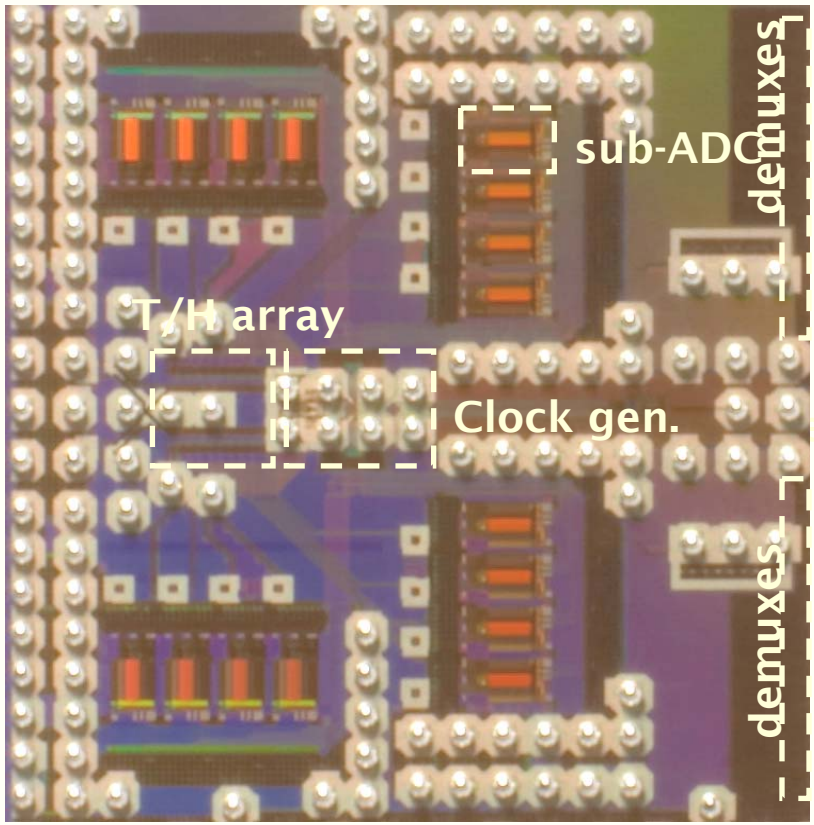


40G IM-DD Rx Electronics
37W
$,$$$
No CD or PMD Comp

40G DP-QPSK Rx Electronics
21W
$$
CD & PMD Comp Included

CMOS 22Gs/s ADC Macro

Yes, Virginia, you can have 1B transistors,
but none of them works worth a damn for analog



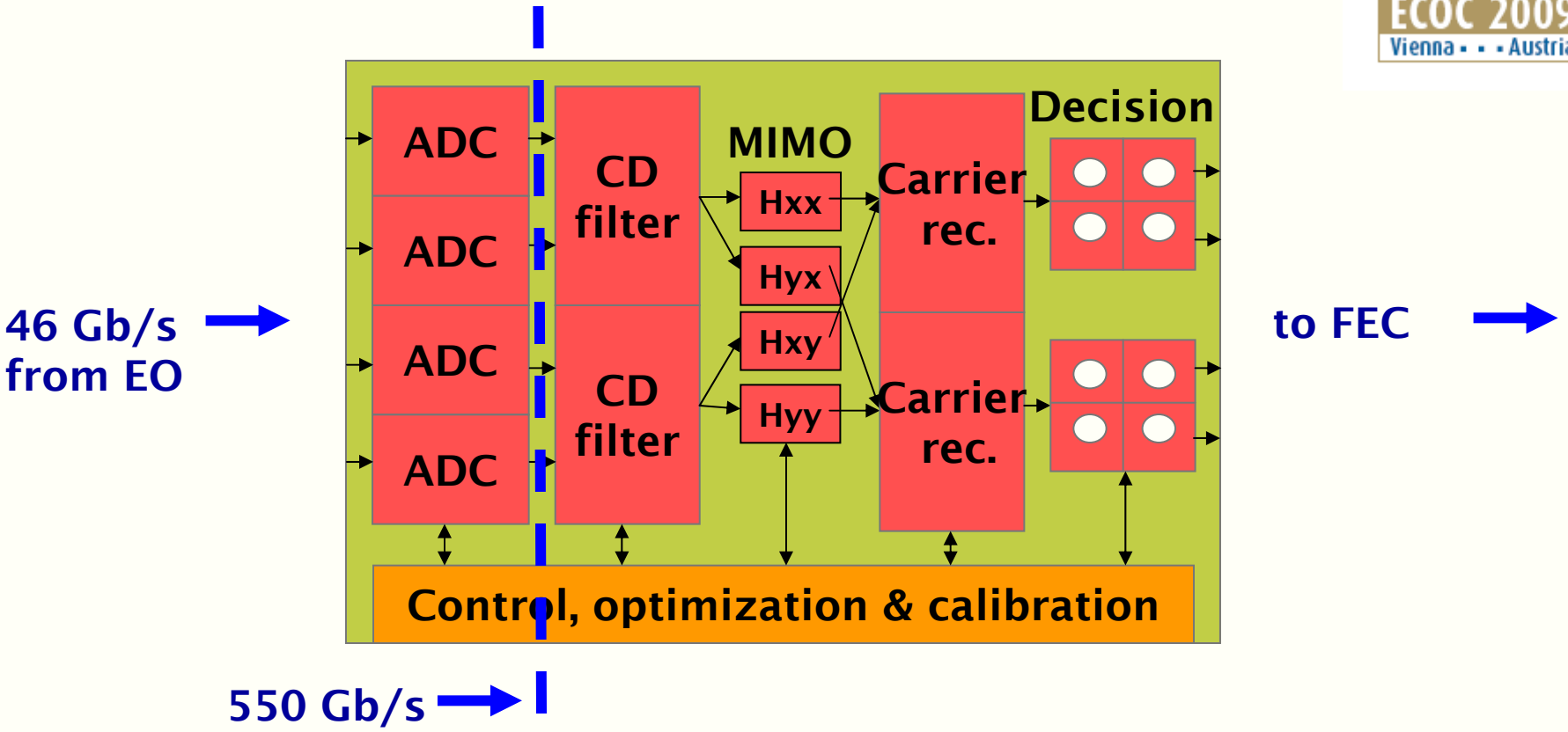
6-bit ADC performance

Resolution	6 bits
Conversion rate	0.1 - 24GS/s
Input range	$1.2V_{p-p}$ diff.
ENOB	4.8, F_{in}= 8GHz 4.1, F_{in}= 12GHz
SFDR	40dB @ 8GHz 35dB @ 12GHz
Power	1.2W @ 1V and 2.5V
ADC area	4 x 4 mm^2
Process	90nm digital CMOS

Design relies on:
uniform & linear inter-metal capacitance & fast comparators –
the rest is digital

Power and Macro Size Suitable for integration on CMOS ASIC

The Case for Integration

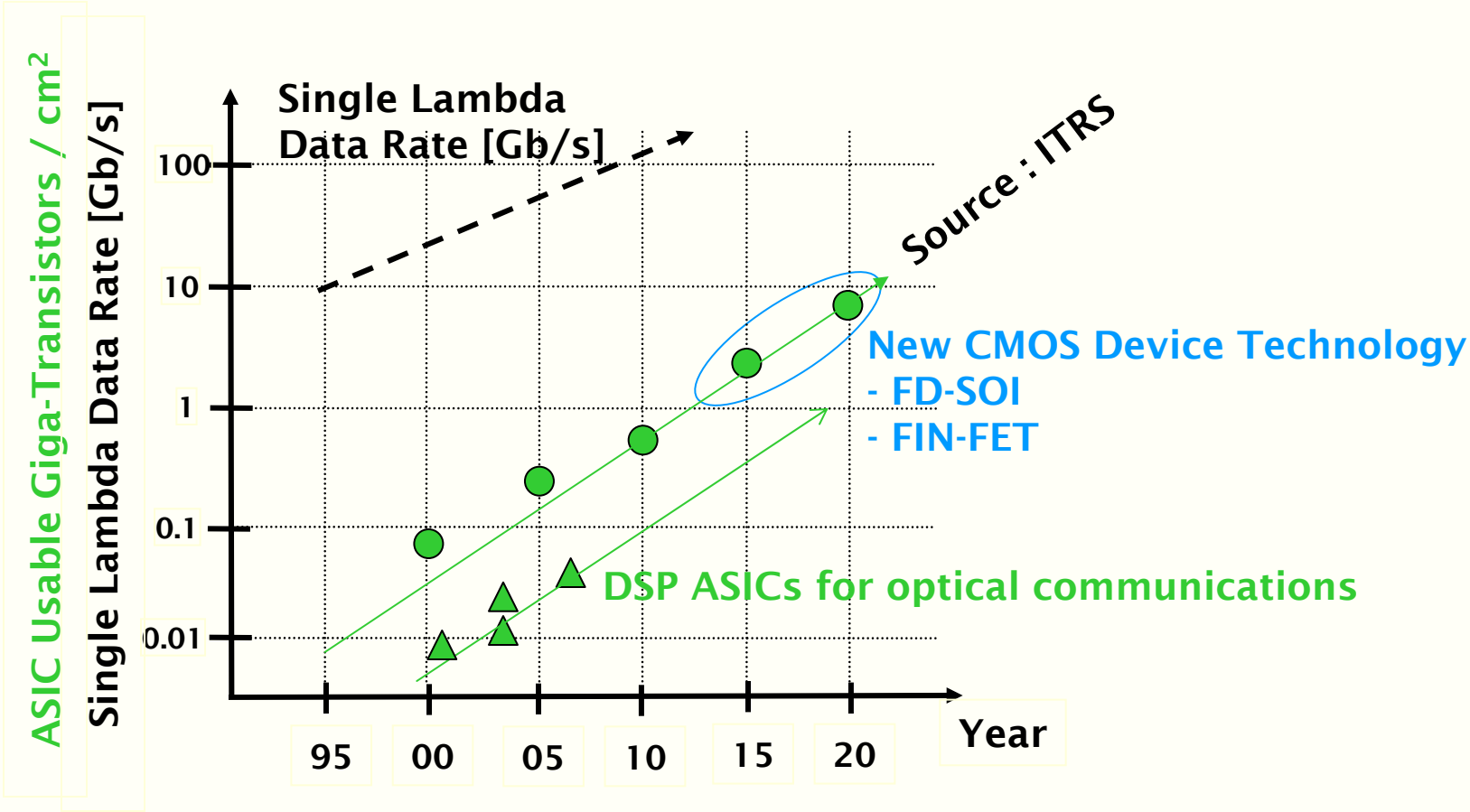


1/ Core with ADC

Off-chip SERDES links ~ 20-30mW/Gb/s
(11W-17W for example shown)

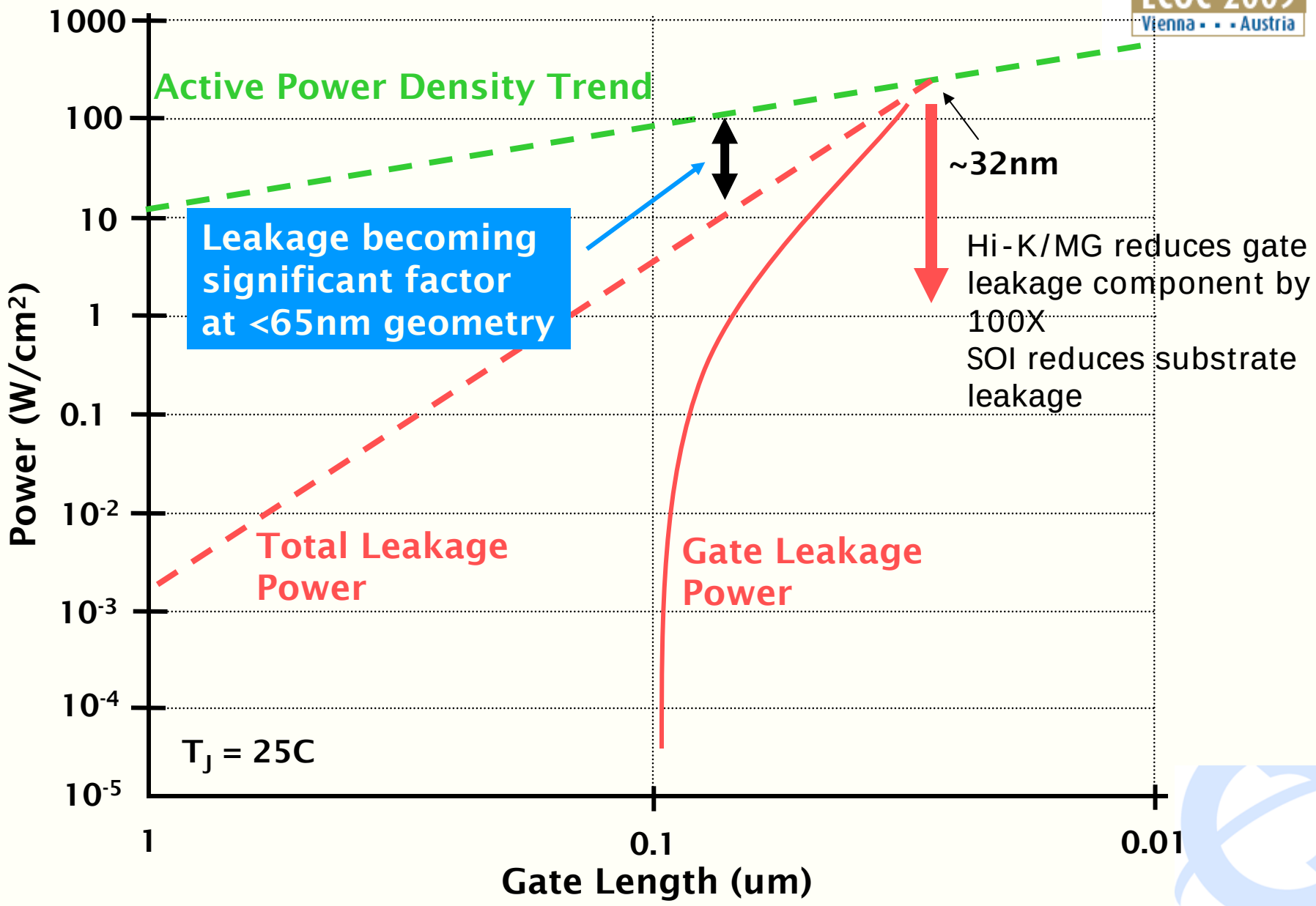
2/ FEC with Core (redoubled for soft FEC)

Roadmap – Enough Gates for Future DSP



Tracking Moore's Law Industry Curve

Leakage needs a technological fix



Wrap-up

Pure CMOS gives us what we need now:

- Fast enough for our data rates
- Suitable ADCs, VCOs …
- Enough gates to do the job

The roadmap has its challenges:

- Leakage needs work
- Voltage scaling has (almost) stopped
- Speed improvements are harder to get

But there's a $250B/year industry pushing those limits…..

I see CMOS ICs in optical's future

Acknowledgements

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Thank You