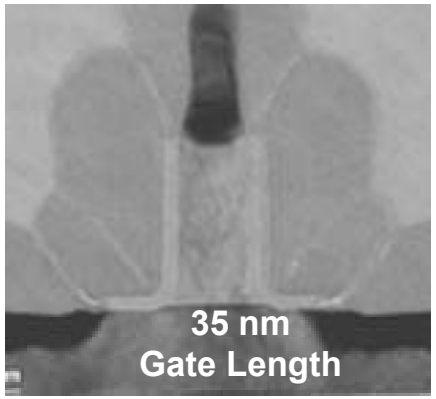
Zurich Research Laboratory

Electro-optical packaging trends for computing applications

Bert Jan Offrein

Innovation challenges at all levels of the computing system

- Miniaturization of the logic device



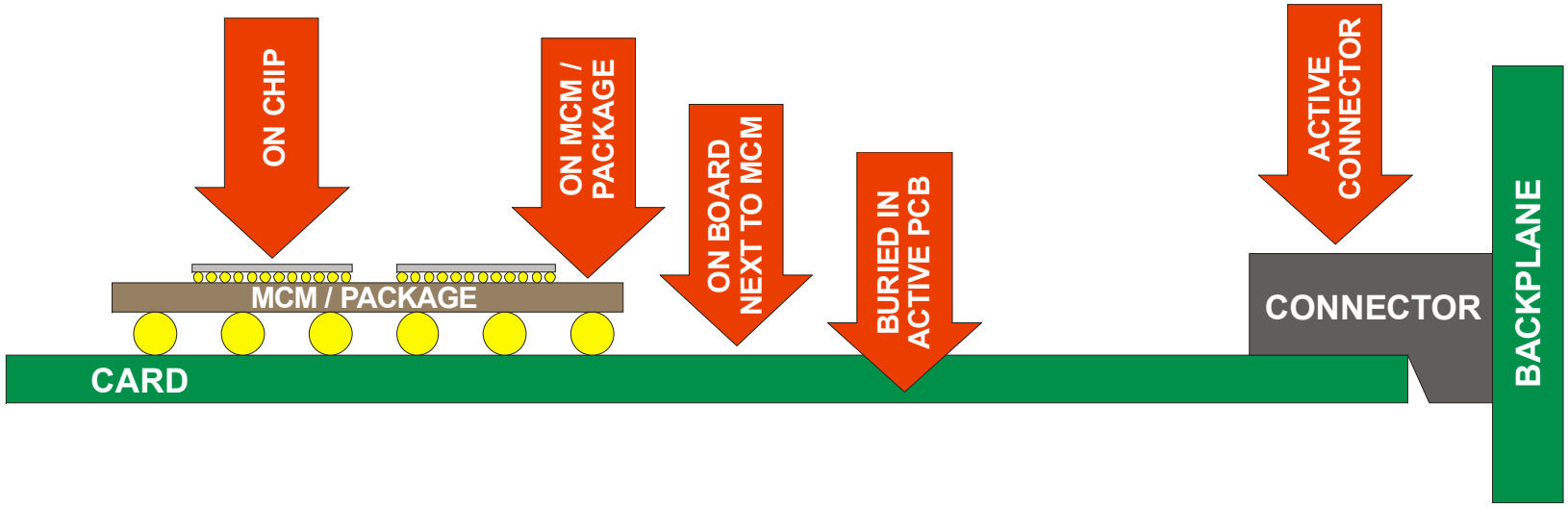
- Intra-system communication

- How can optics help?
  - Optical communications!
  - All-optical logic?

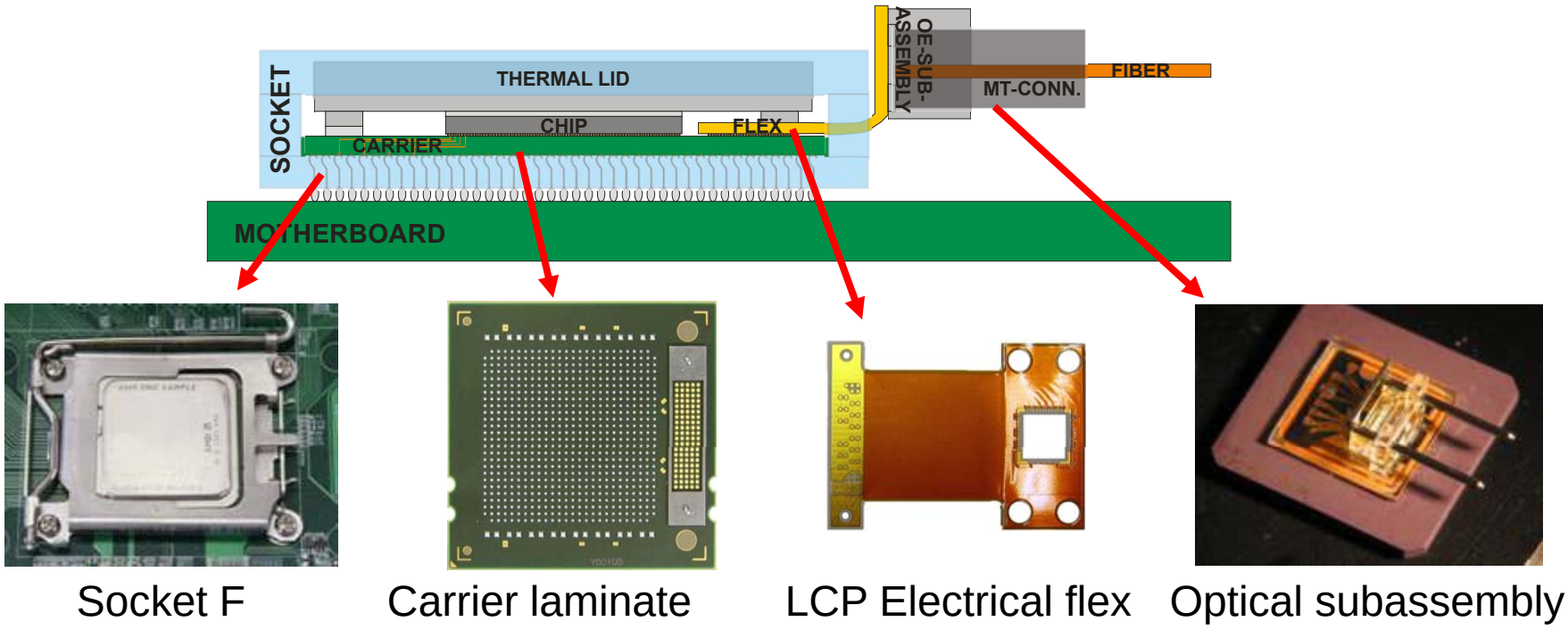
Where to attach the optics?

- Density advantage →As close as possible to the processor
- Signal quality → As close as possible to the processor

- Technology development → Build on existing technology
- Supplier ecosystem → Build on existing technology
- Technology acceptance → Build on existing technology



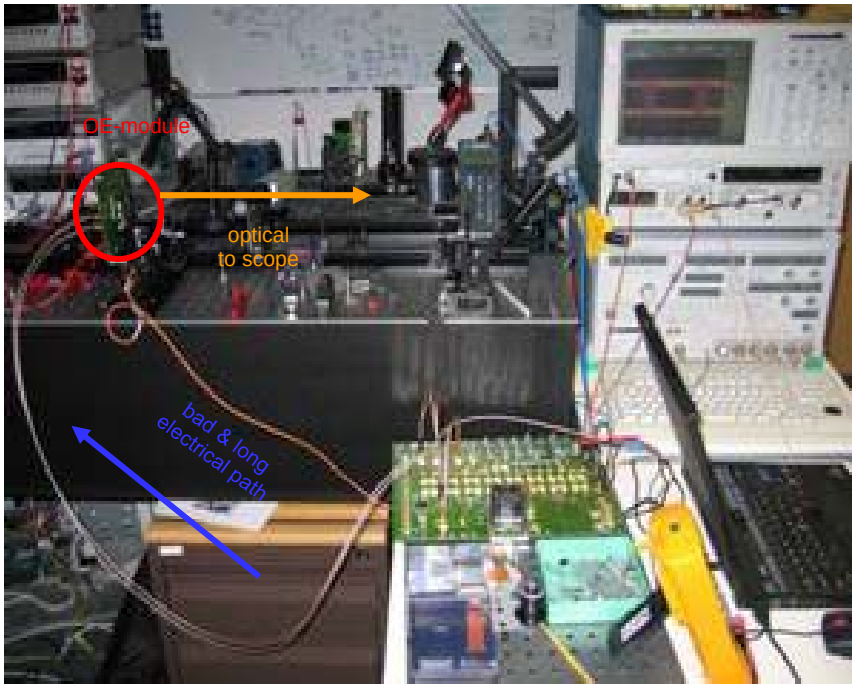
Optics to the carrier - Implementation



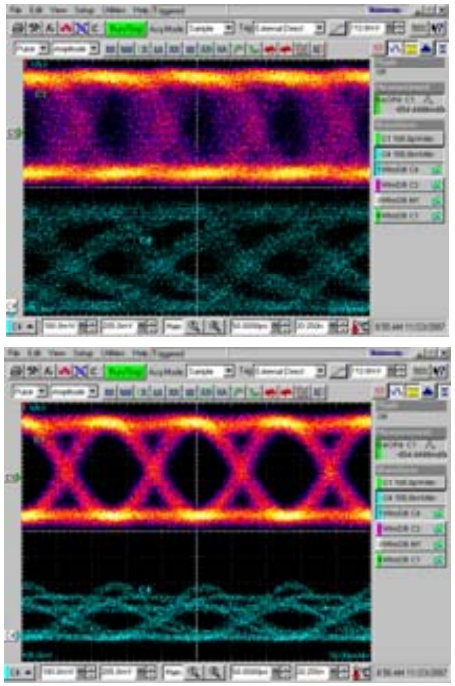
- Mostly standard processes and designs were applied
  - FPGA (Xilinx Virtex-4 FX60) in stead of a processor for flexibility and layout effort reasons

Optical characterization

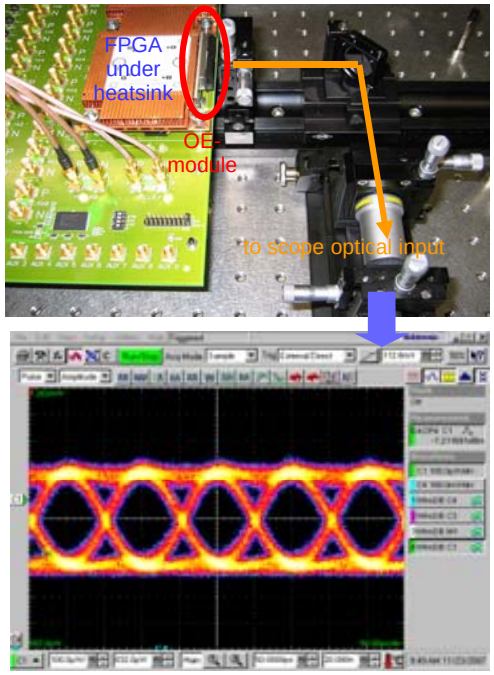
- OE-module driven by FPGA
  - Successful operation at 10 Gbps (Over-clocking)
  - Pre-emphasis tests on link through socket and long cables



Pre-test with OE-module on separate testboard



Without (top) and with pre-emphasis at 8 Gbps

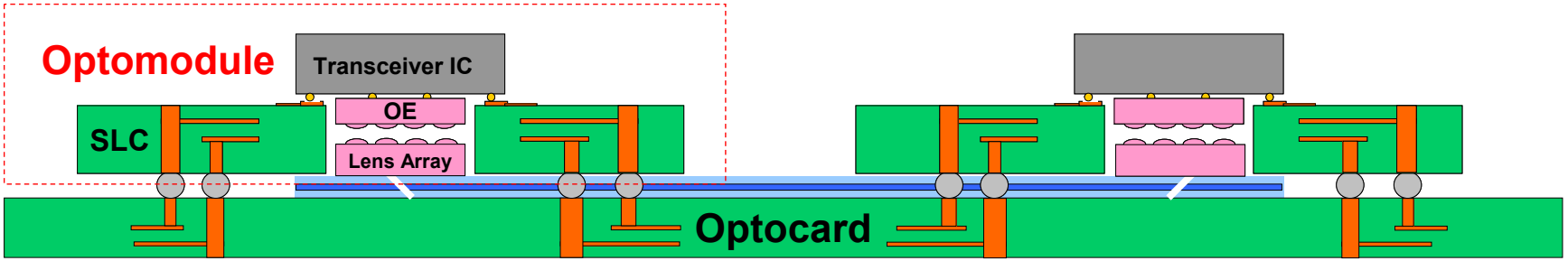


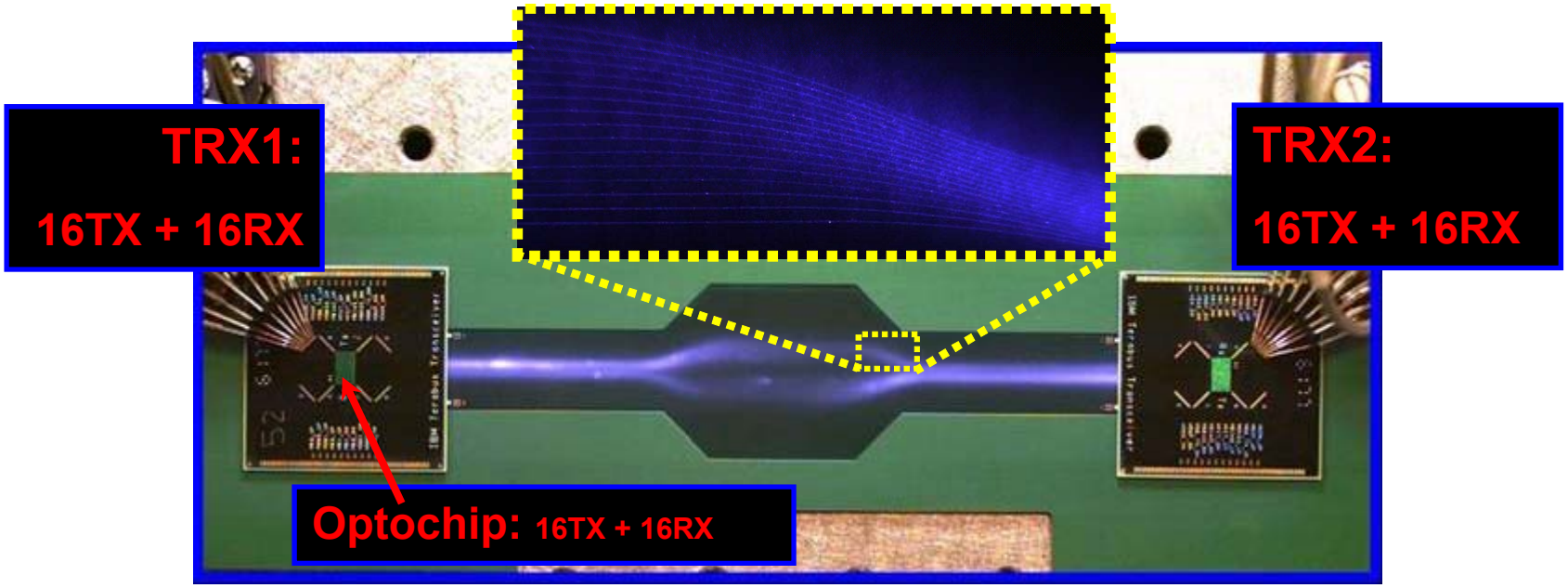
OE-module driven by FPGA at 10 Gb/s (no pre-emphasis)

Issues and challenges

- Additional assembly steps related to optics
- Cost, cost, cost, ….
- How much optics is required at all?
  - A lot! → Multiple Tb/s IO Bandwidth
  - 10 Gb/s per fiber → 100's to 1000's of fibers!
- Routing of many fibers is tedious and costly
- Cost, cost, cost, …

Terabus: Board-Level Optical Links

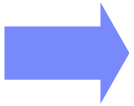


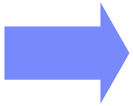


16 Channels TRX1 → TRX2 at 10Gb/s + 16 Channels TRX1 ← TRX2 at 10Gb/s

Challenges on optical printed circuit boards

- Alternative applications are required that drive development

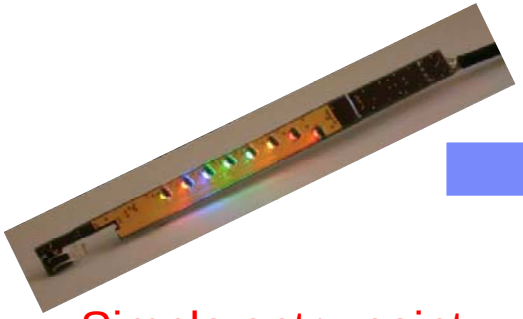


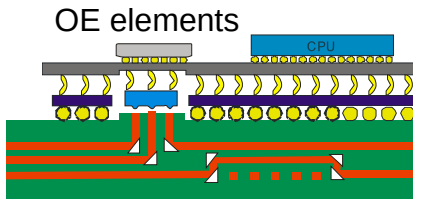

Simple entry point — Enabler — High-end application

Example: LCD display technology development chain

- Computing applications are high-end (Complex, # channels, reliability)

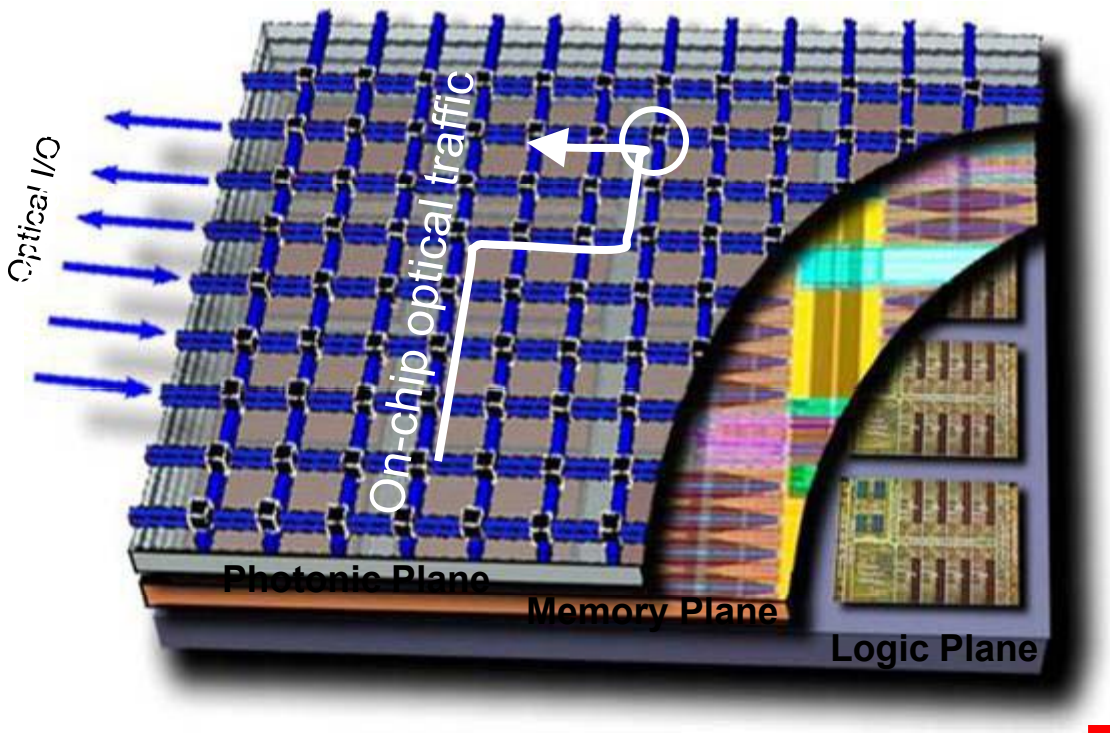
- How could this chain look for optical pcb technology?





Simple entry point — Enabler? — High-end application

Vision for 22nm CMOS (circa 2018) - 10 TFLOPs on a 3D chip



36 “Cell” chip (~300 cores)

System level study:
IBM, Columbia, Cornell, UCSB

Co-PIs:
Jeff Kash (IBM)
Keren Bergman (Columbia)
Yurii Vlasov (IBM)

Logic plane	~300 cores
Memory plane	~30GB eDRAM
Photonic plane	On-Chip Optical Network
	>70Tbps optical on-chip
	>70Tbps optical off-chip

Photonic layer is not only connecting various cores, but also routes the traffic

All future dates and specifications are estimations only. Subject to change without notice.

Conclusions

- Optical technology will play an important role in future HPC
- Where will it go? Rack to rack, board to board, chip to chip
- Two different optical technology classes will find its way
  - Multimode optics, short to middle term
  - Single mode optics (Si-photonics), longer term
- A high state of electrical / optical integration is required to make optics successful
- Evolution or revolution?

Thank you for your attention!

Bert Jan Offrein