Semiconductor Nanowire Heteroepitaxy on Arbitrary Substrates for Optoelectronic Devices and Massively Parallel Interconnects

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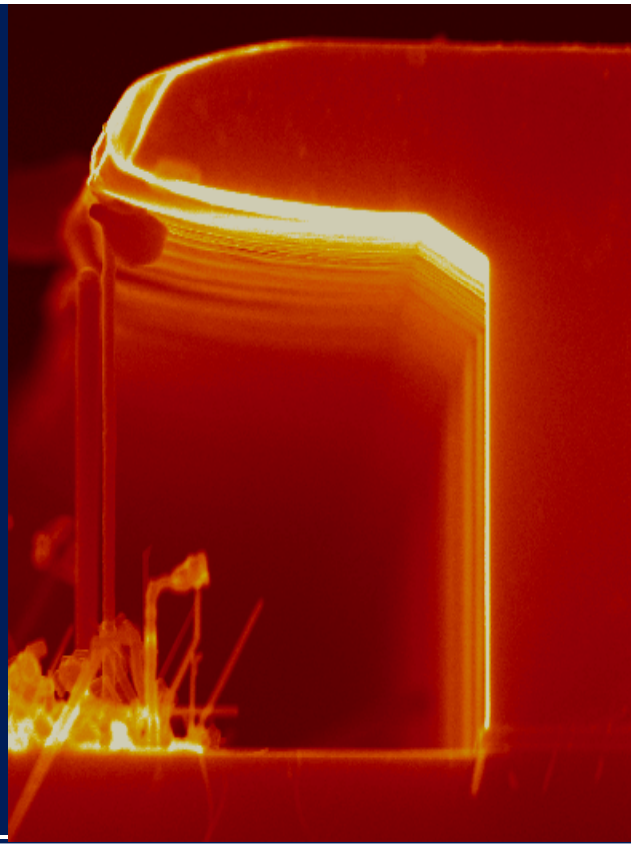
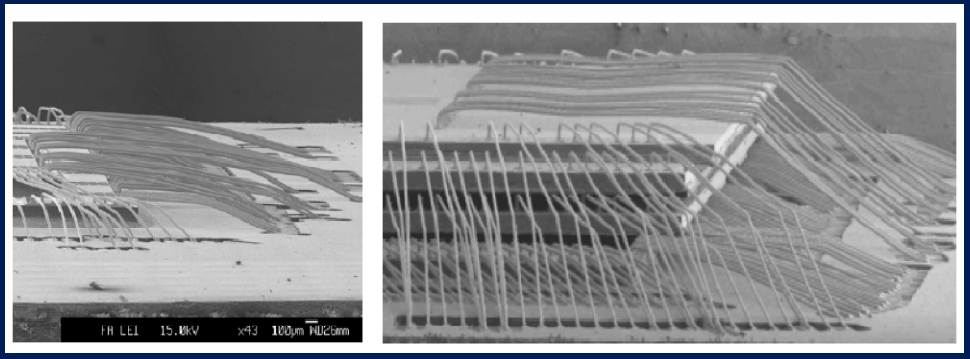
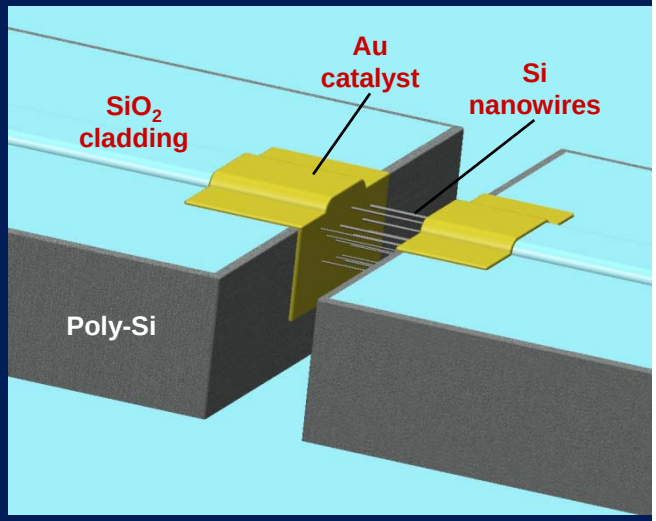


Outline

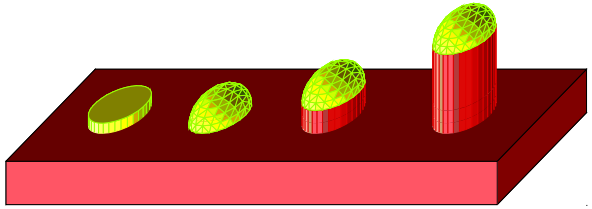
- **Semiconductor nanowires to overcome issues of heteroepitaxy**
  - **Constraints of substrates**
  - **Enabling Devices for Si Photonics**

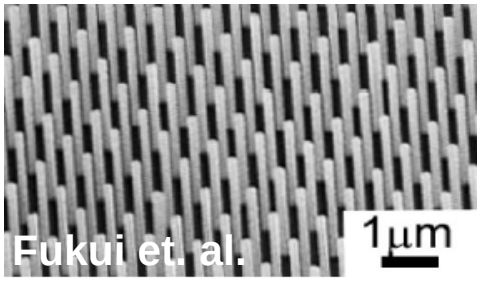
- **Nanowires as Interconnects**

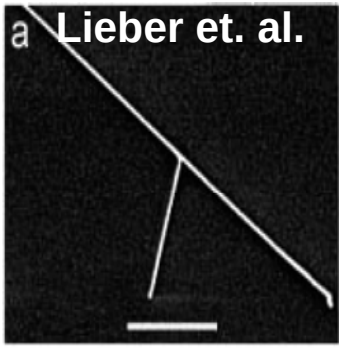


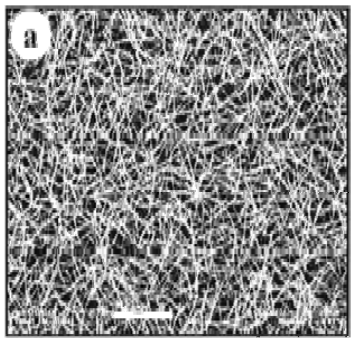


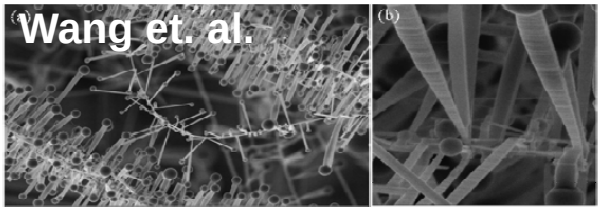
One-D Nanowires

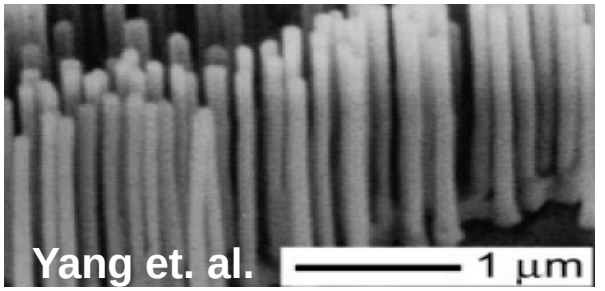


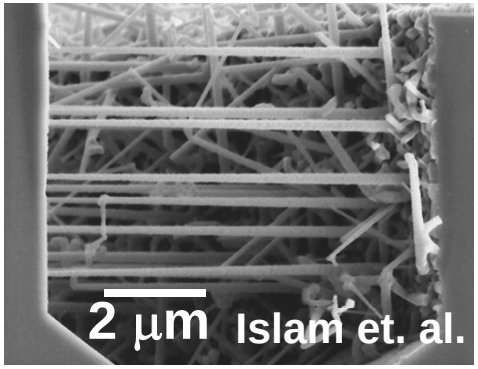


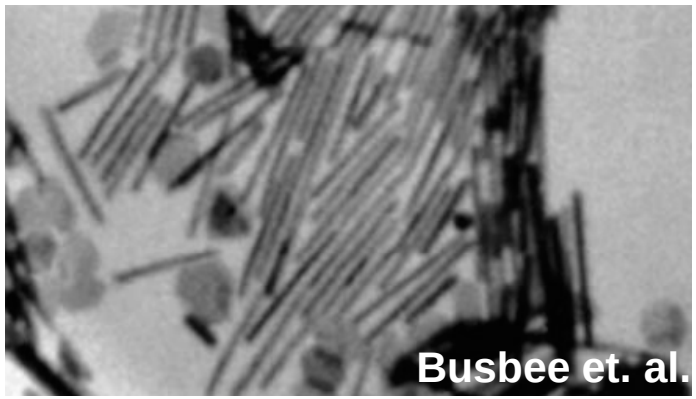


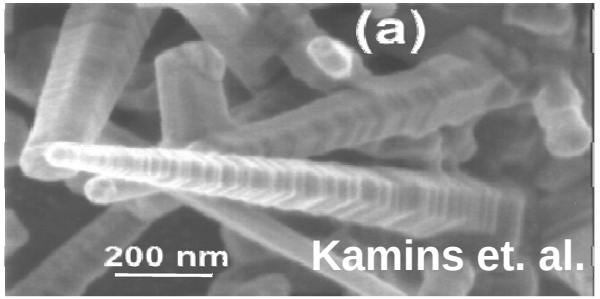


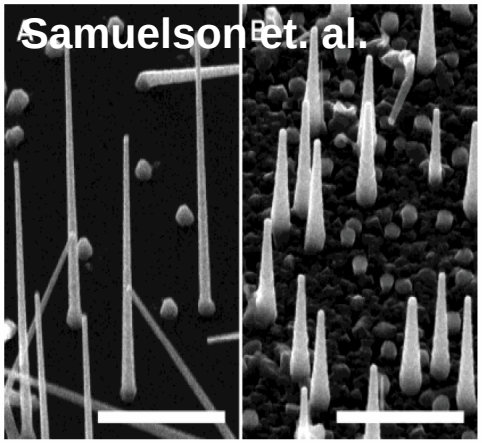


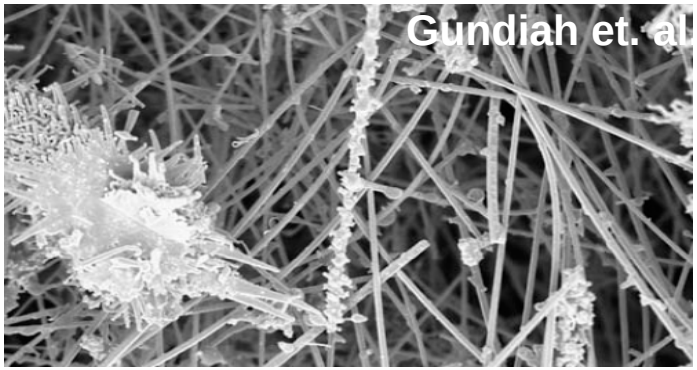


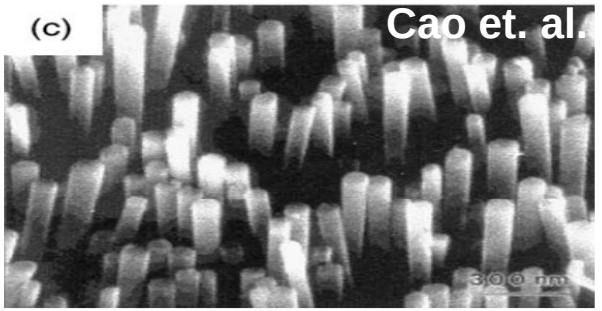










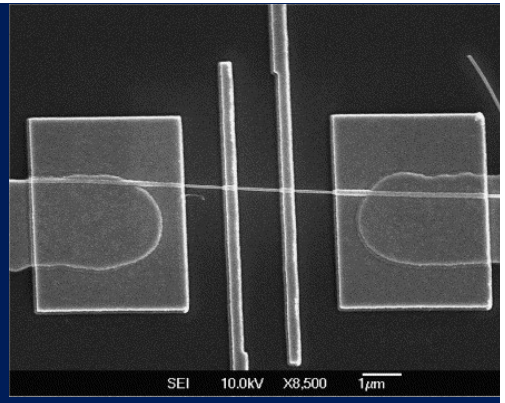


Zhou, Meyyappan, Kim, Ng, Samuelson …..Ag, Au, Zn, InP, ZnO, Si, Ge, Si-Ge, ZnS, GaN, InGaAs, In_2O_3

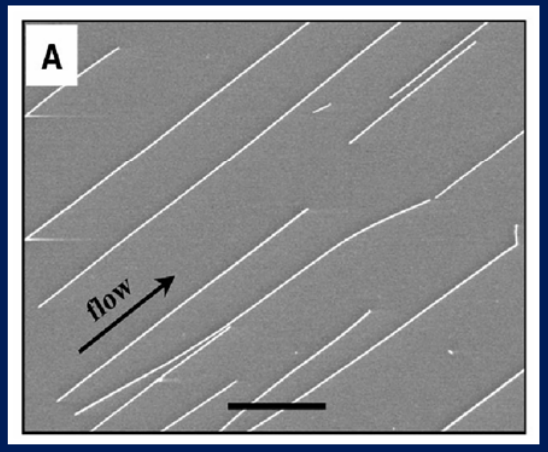
The Challenge: Interconnecting Nanowire Devices

Research based approach

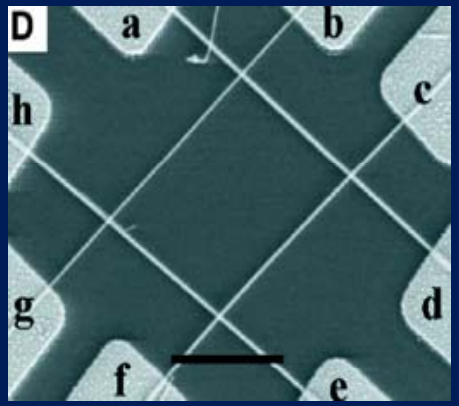
- Alignment by fluid flow & electric field
- Contact formed by e-beam lithography
- One device at a time
- Helps characterize & explore novel nanostructure device applications



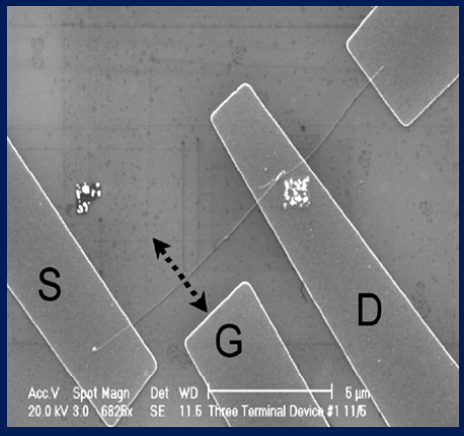
Mayer, Penn State



Lieber et. al. Science 2001 26, 291, 630-633

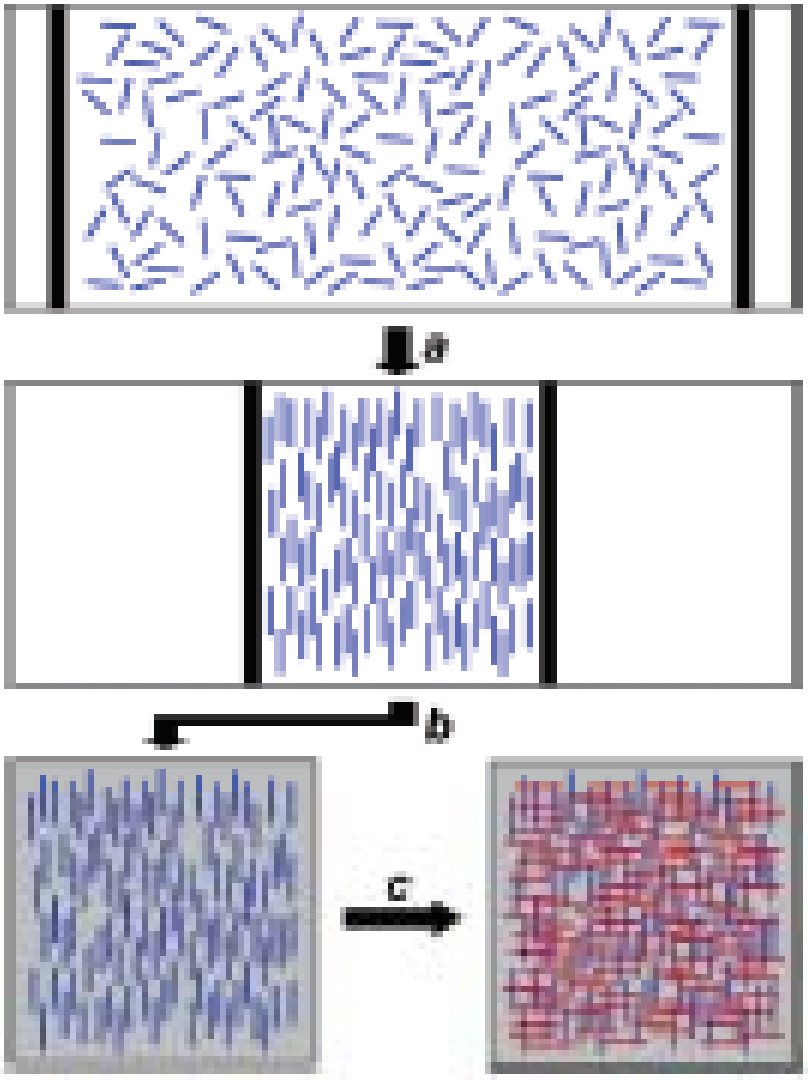


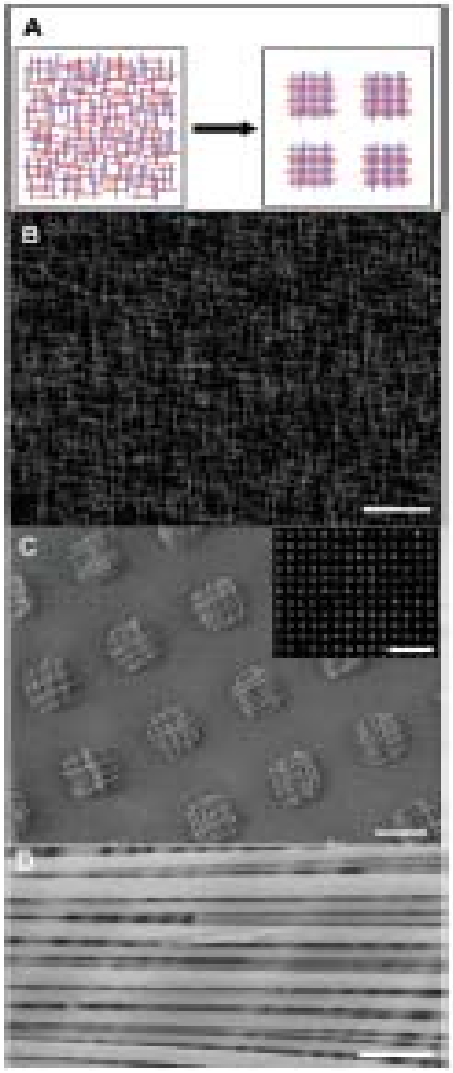
Lieber et. al., Harvard

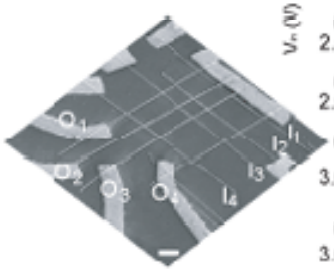


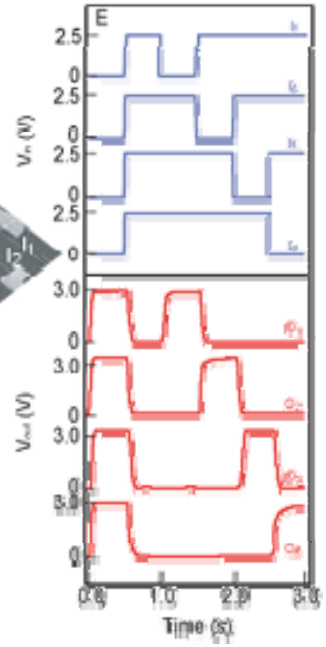
Heath et. al., UCLA/Caltech

Manipulation of NWs



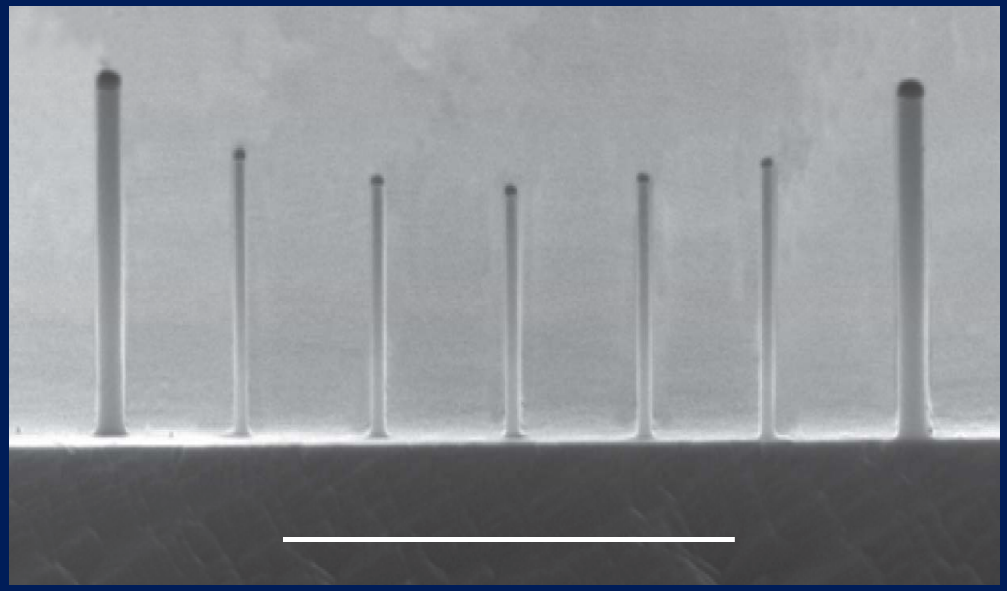






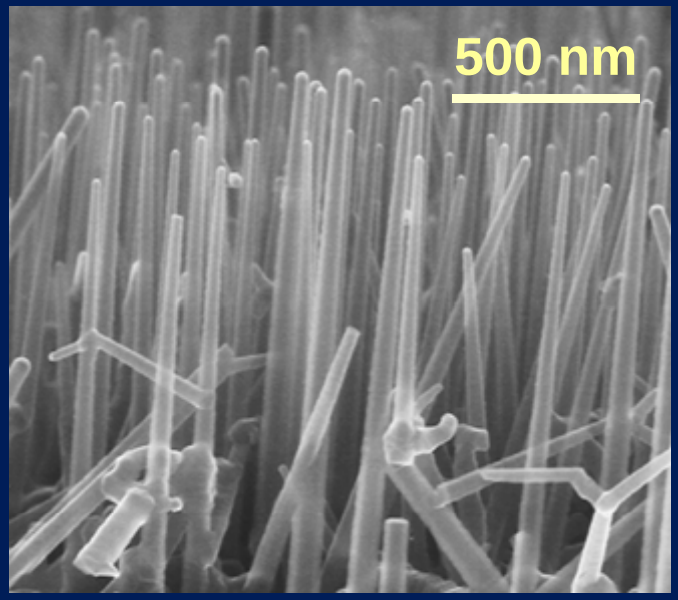
Lieber et. al., Harvard

Growth Direction and "Epitaxy"



Borgstrom et. al., 2007

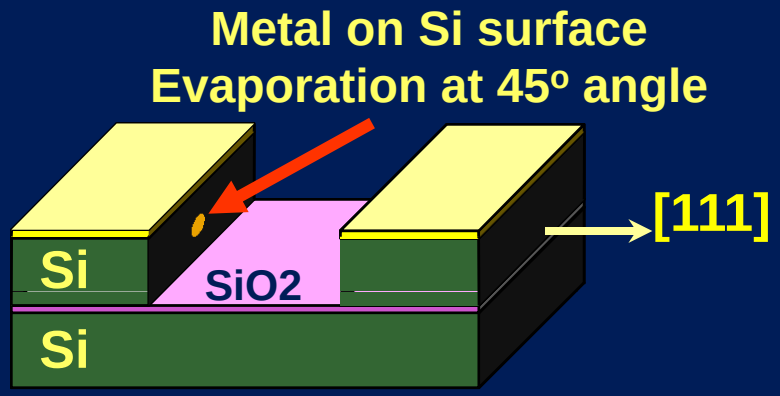
(111)-4° substrate



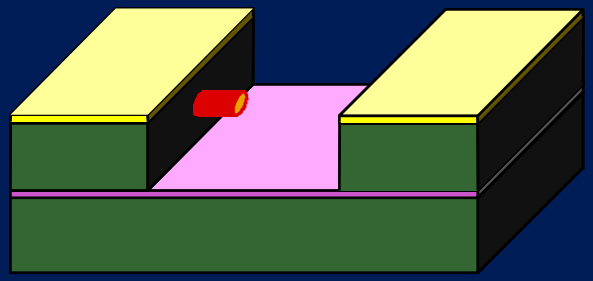
T I Kamins et. al.

Good electrical and mechanical connection to the substrate

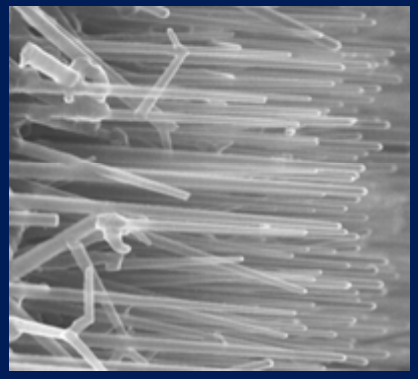
Simultaneous Growth of Nanowires and Connecting Electrodes

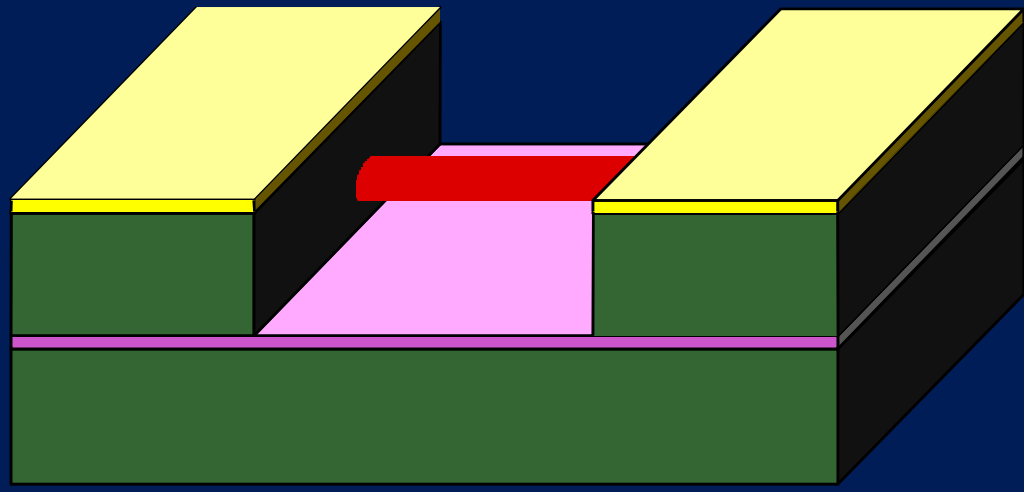


1. Metal deposition, metal-silicide formation



2. Growth of Nanowire



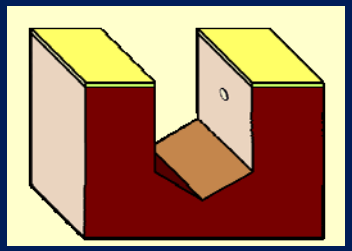


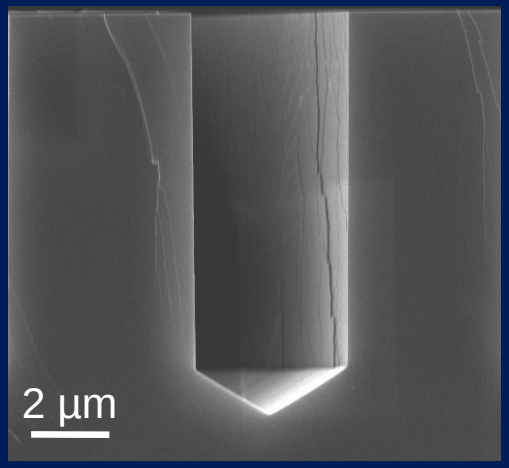
3. Nanowire Bridge

Saif Islam et. al., Nanotechnology 15 (2004) L5–L8

Connecting Nanostructures: Bridging Nanowires

Form trench and deposit catalyst





M. Saif Islam, S. Sharma, T. I. Kamins, and R. Stanley Williams, Nanotechnology **15**, L5-L8 (May 2004)

Connecting Nanostructures: Bridging Nanowires

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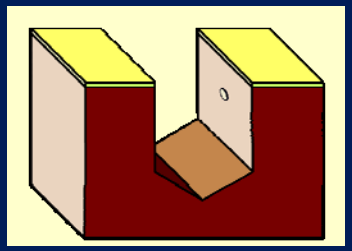
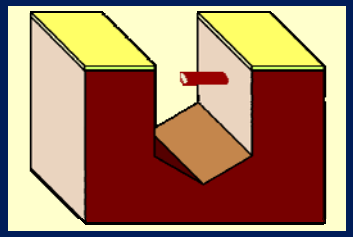
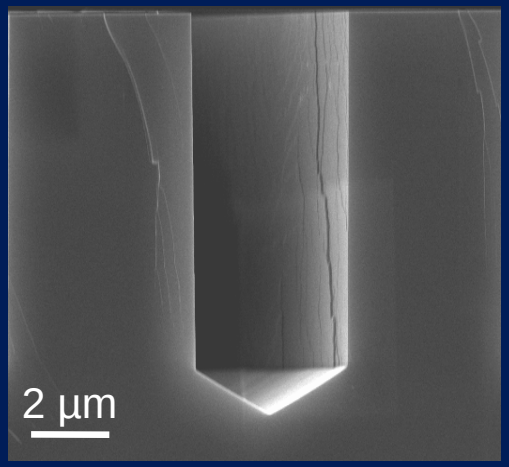
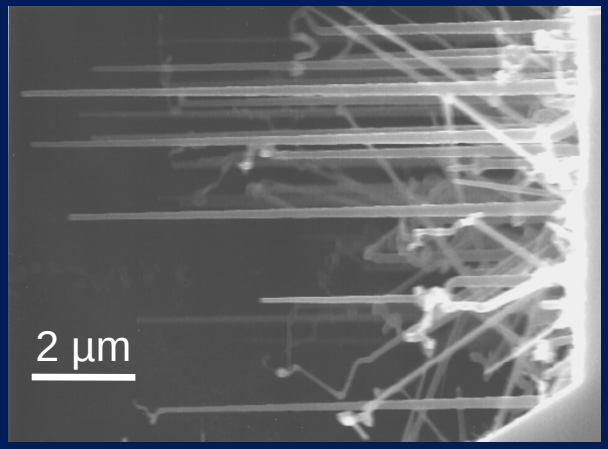


Nanowire grows perpendicular to (111)-oriented sidewall



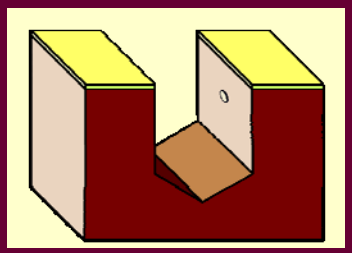




M. Saif Islam, S. Sharma, T. I. Kamins, and R. Stanley Williams, Nanotechnology **15**, L5-L8 (May 2004)

Connecting Nanostructures: Bridging Nanowires

Form trench and deposit catalyst



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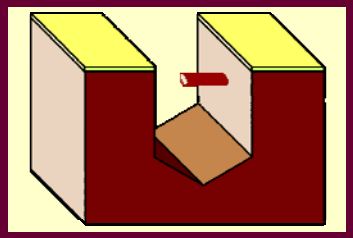
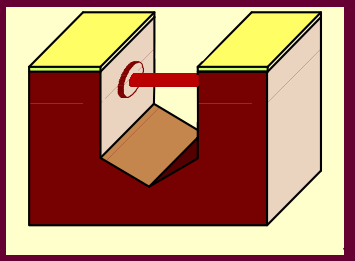
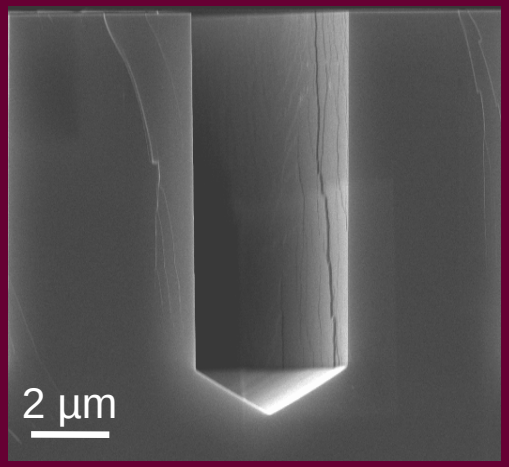
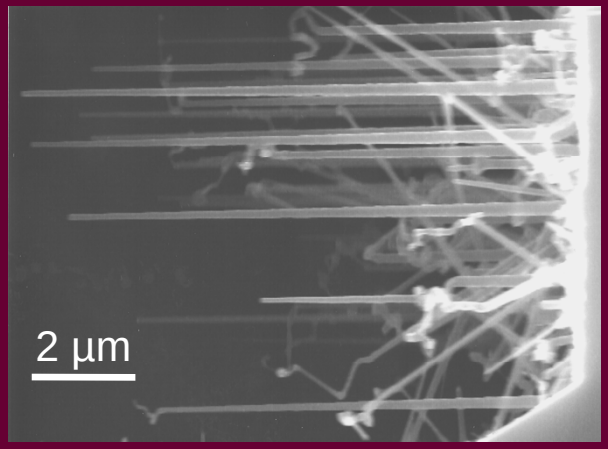
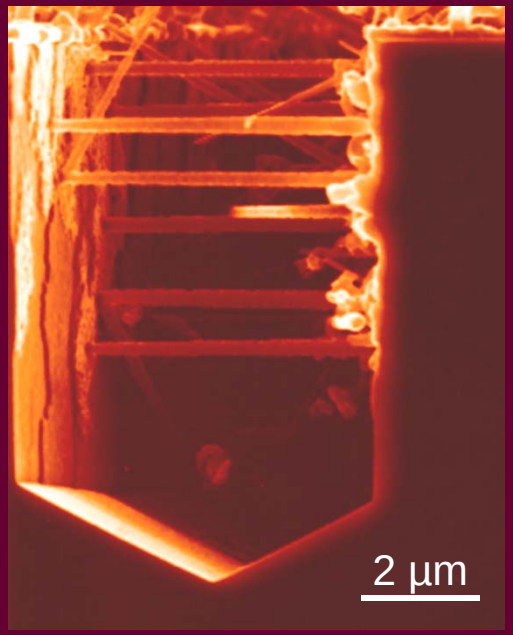


Nanowire connects to opposite sidewall



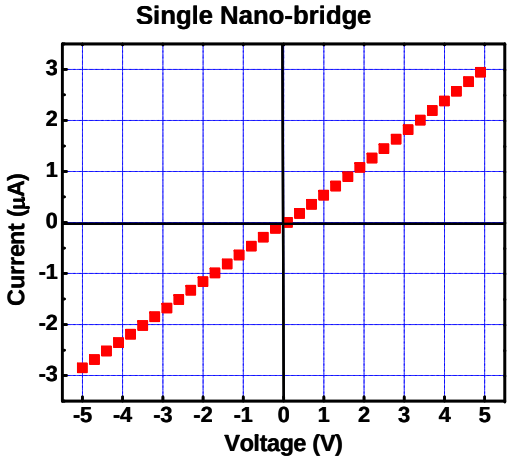


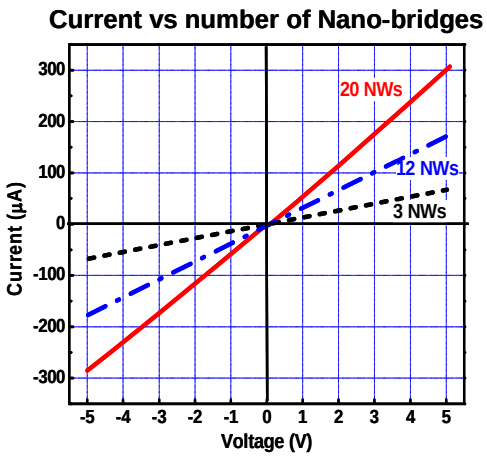


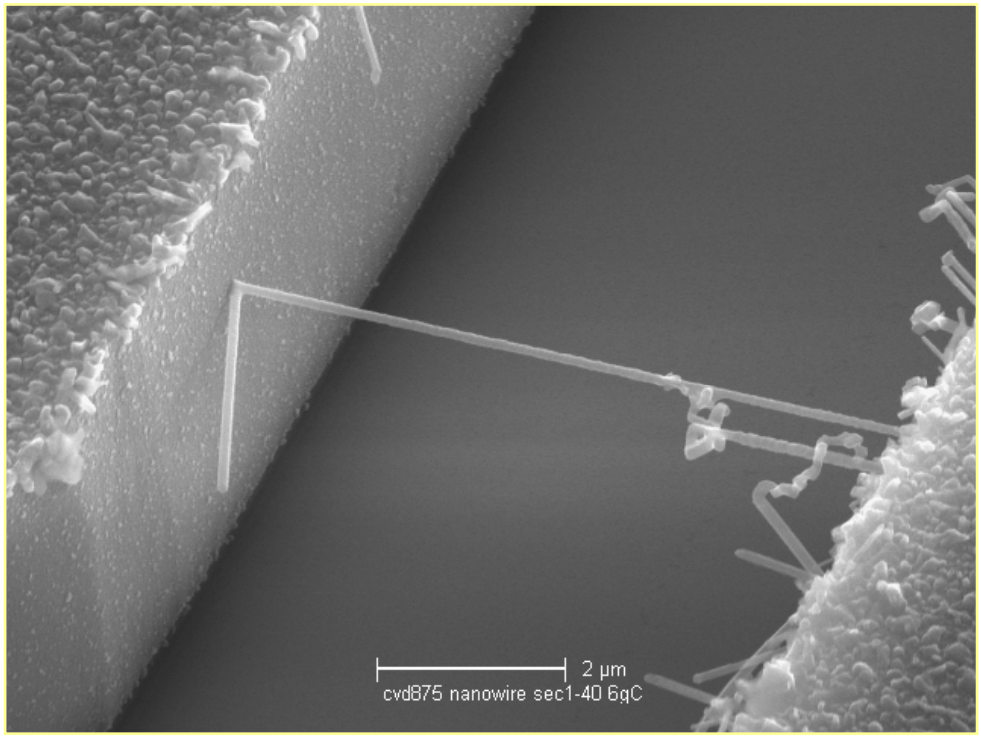


M. Saif Islam, S. Sharma, T. I. Kamins, and R. Stanley Williams, Nanotechnology **15**, L5-L8 (May 2004)

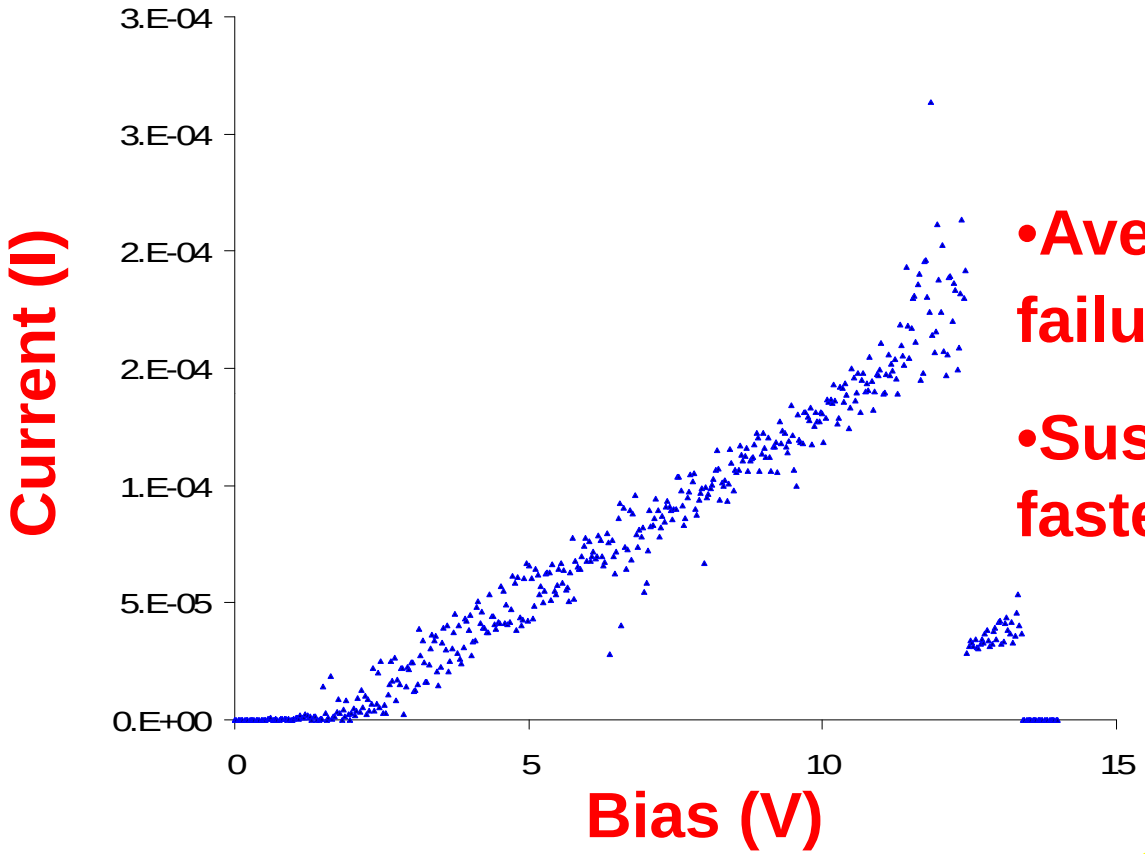
Easier Interfacing, Linear and Ohmic





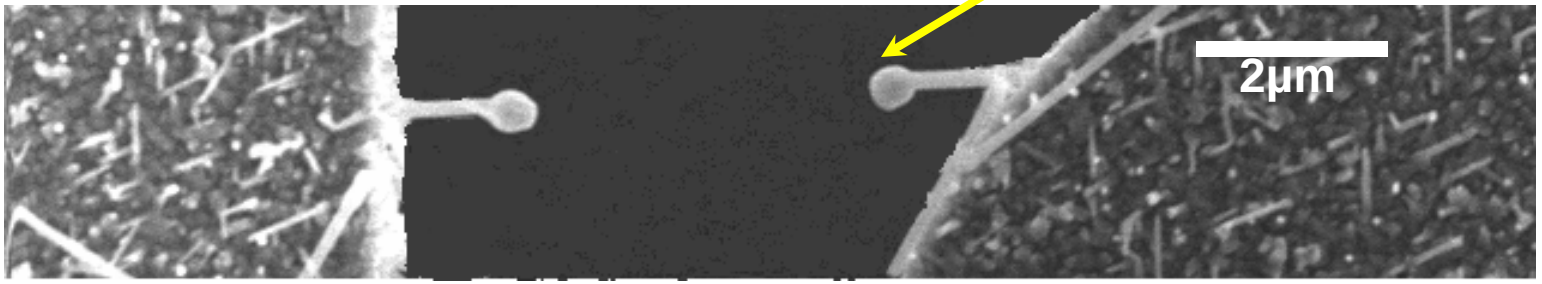


Bridging Si Nanowires



- Average current density at failure 3.8×10^6 A/cm^2
- Suspended bridges help in faster thermal dissipation

Nano-lollipops

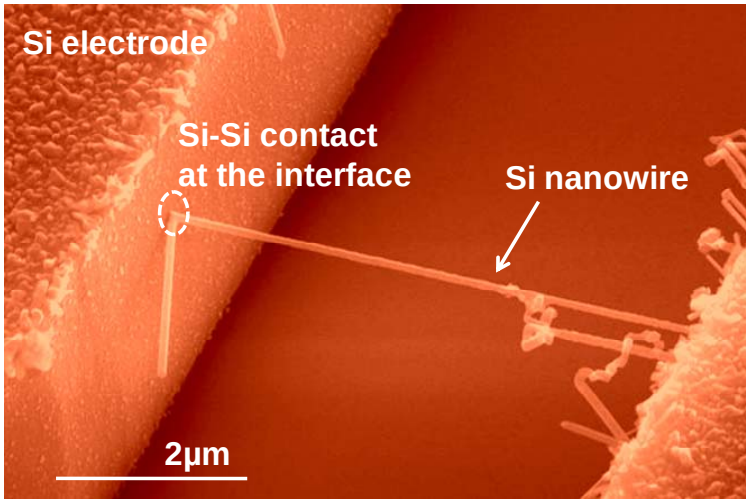


Length vs Resistance

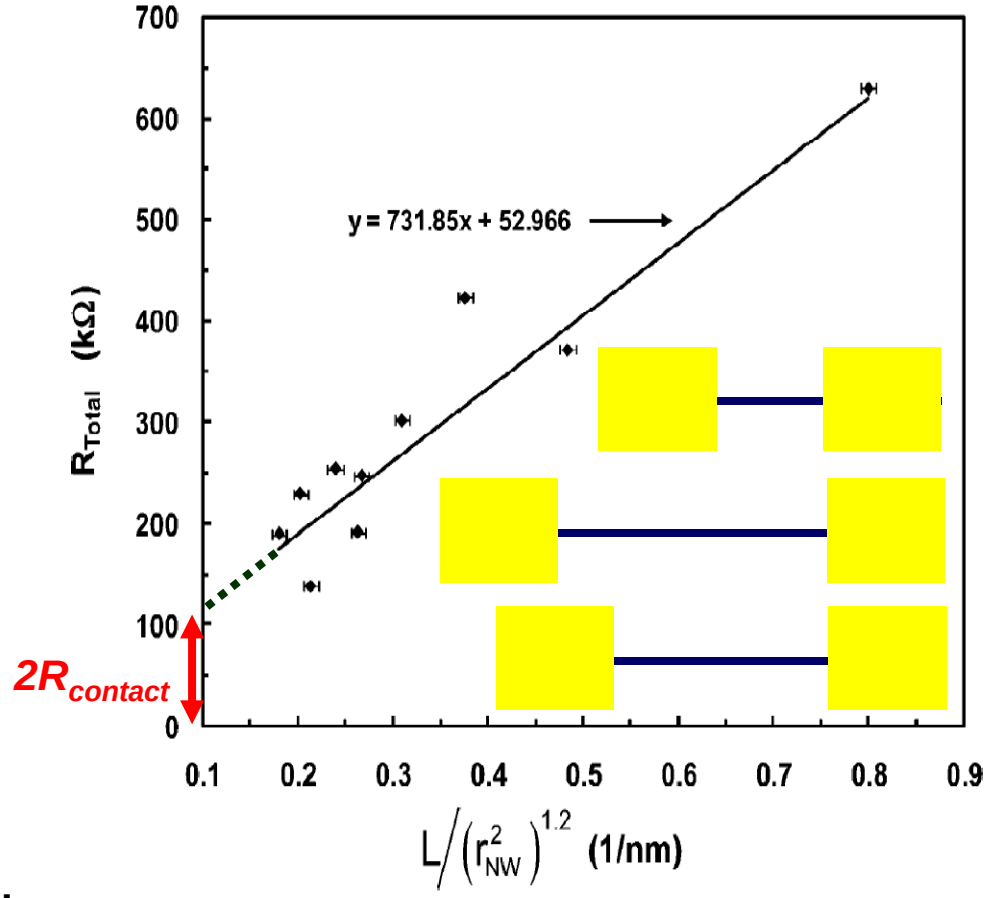
Ultra-Low Contact Resistance of Epitaxially Interfaced Bridged Silicon Nanowires

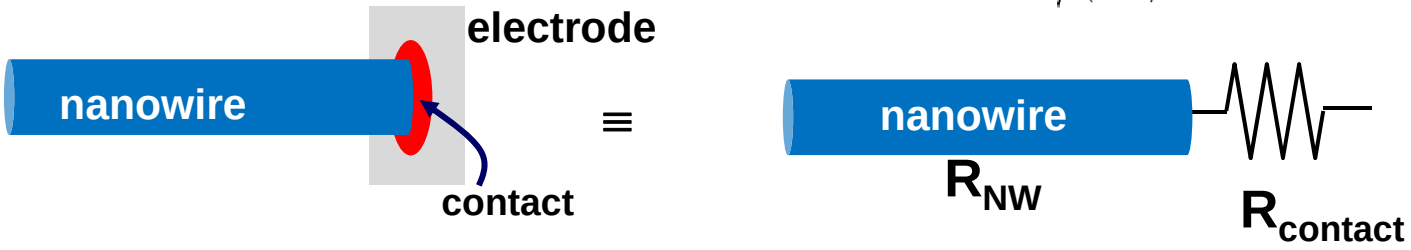
Anurag Chaudhry, Vishwanath Ramamurthi, Erin Forg, and M. Saif Islam*

Integrated NanoDevices and Systems Research, Department of Electrical and Computer Engineering, University of California, Davis, Davis, California 95616



Nano Letters, vol. 7, pp. 1536-1541, 2007





Noise in Si Nanowires

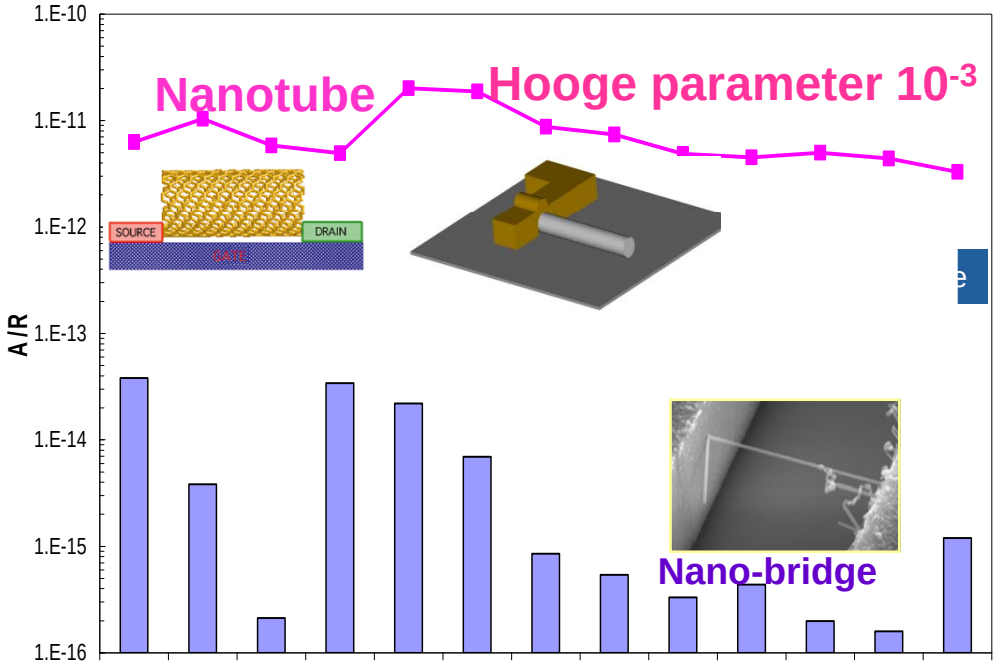
Noise measurement shows

- Carrier **mobility fluctuation**
- Carrier **trapping–detrapping** etc.
- Yield information about m**anufacturing process & inner workings of a device.**
- **Low voltage operation** requires low noise as the signal to noise ratio is critical.

> Two orders of magnitude lower noise than CNT

ZnO, InP etc. on Si are likely have higher noise due to interface resistance

***A* is relative amplitude of 1/f noise and R is the resistance**

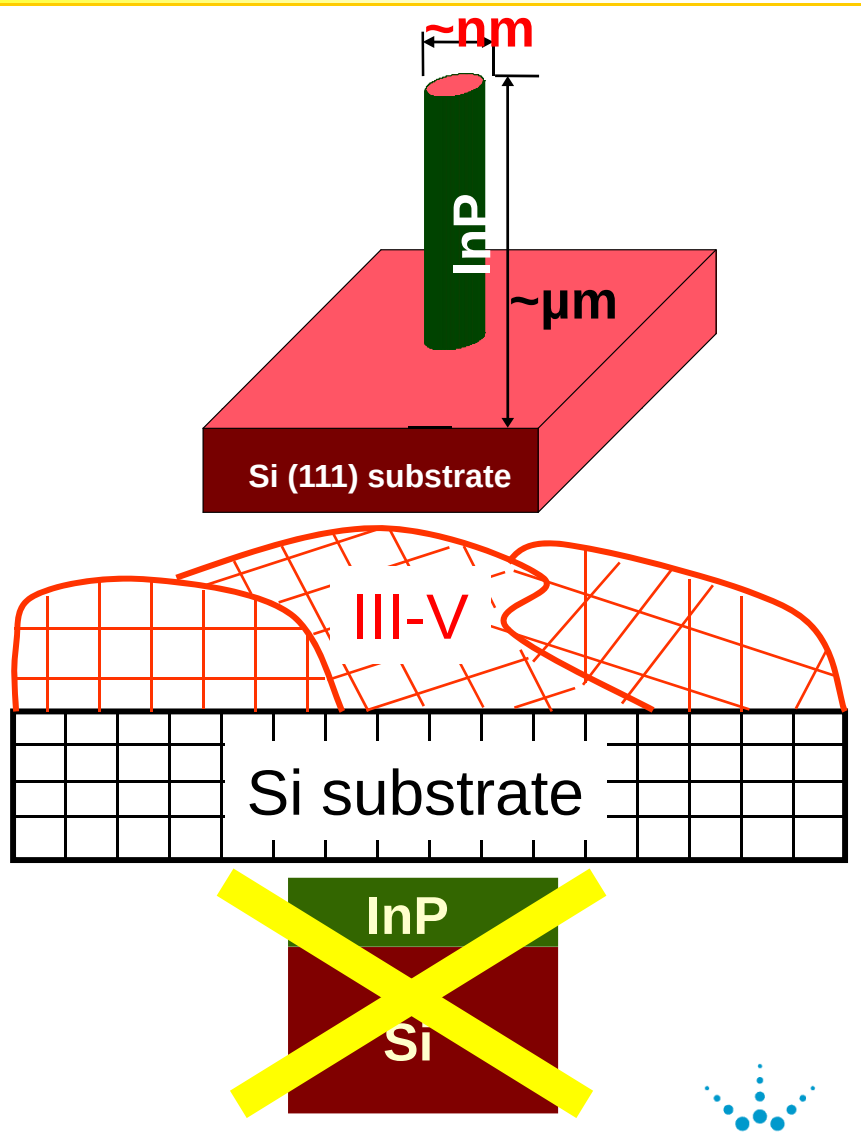


IEEE Trans. Nanotechnology, 5, No. 5, p523 2006

Heteroepitaxial Growth of III-V Nanowires on Silicon surfaces

Issues with planar, epitaxial growth of III-V on Si

- **Large lattice mismatch (~8.06%) causing high-density of misfit dislocations**
- **Large difference in thermal expansion coefficients leading to stress**
- **Difference in crystal structures (polar vs. non-polar) leading to antiphase domains and boundaries**



OPPORTUNITIES

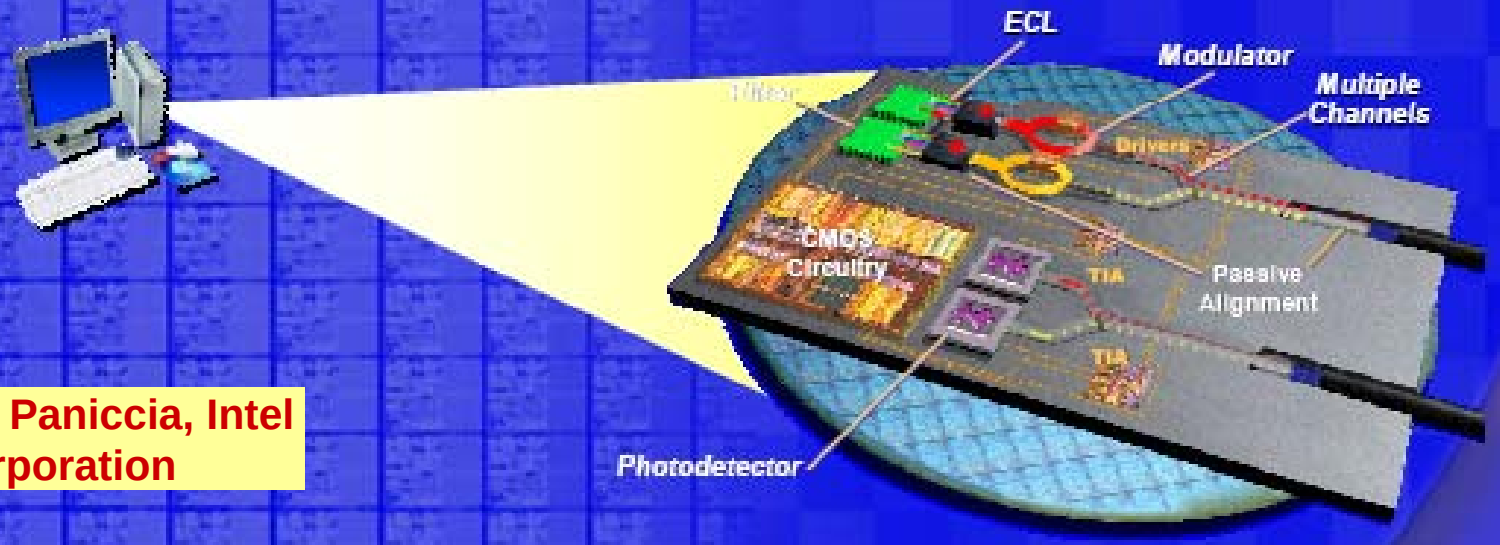
Si Photonics (Lasers, LED, PD, displays etc.)

Ultra-fast III-V devices integrated with Si CMOS (HEMTs, FETs, mixers etc >100GHz speed)

Agilent Technologies
Molecular Technology Laboratory

Intel's Silicon Photonics Research

1. Develop photonic building blocks in silicon
2. Integrate increasing functionality directly onto silicon
3. Long term explore monolithic integration



Dr. Mario Paniccia, Intel Corporation

intel

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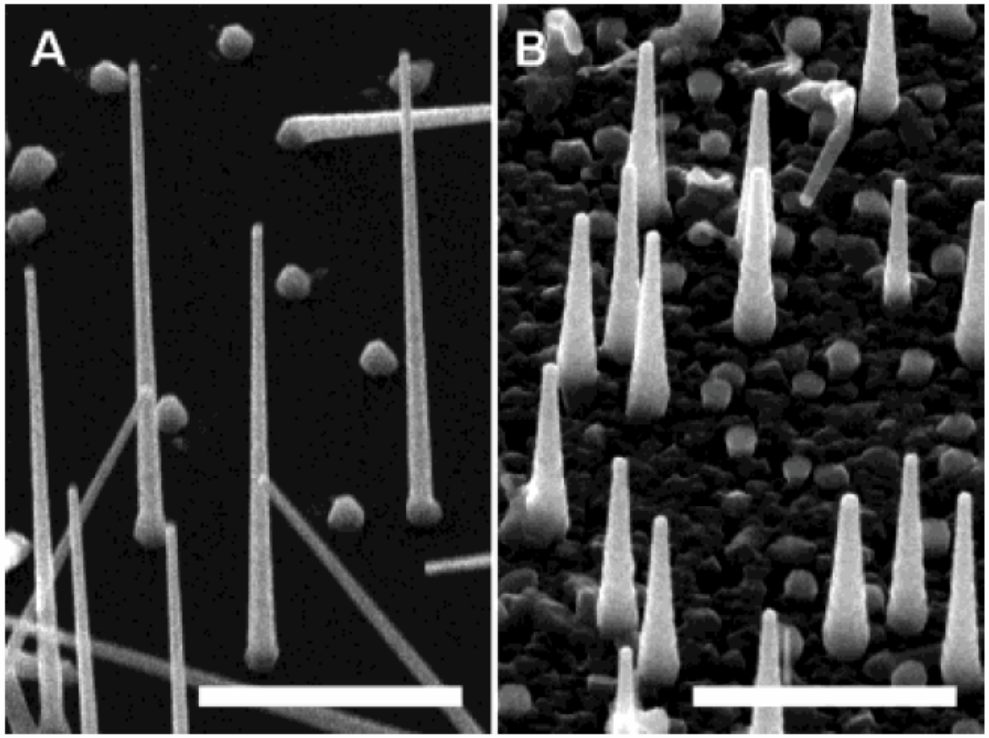
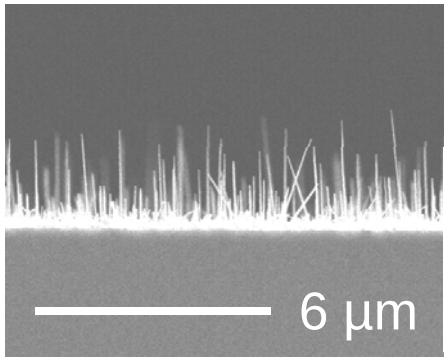
GaAs & InP nanowires grown on Silicon-(111)

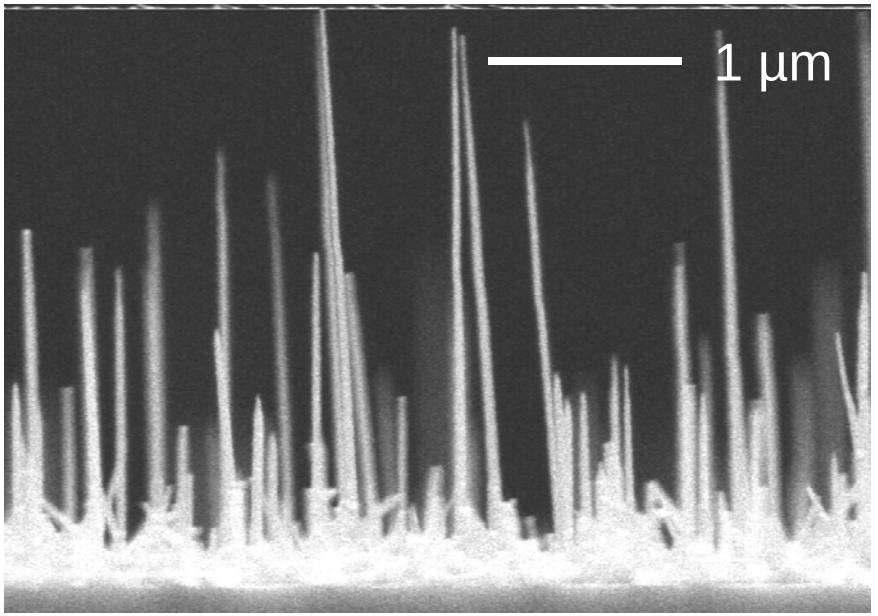


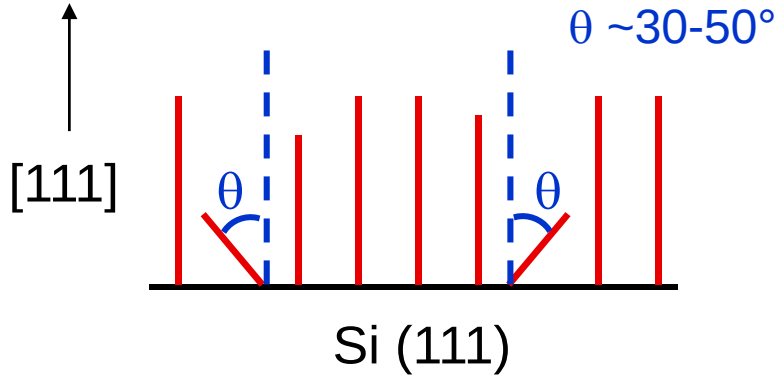
(A) GaAs and and (B) InP nanowires

Samuelson et. al. *NANO LETTERS* 2004 Vol. 4, No. 10 p1987

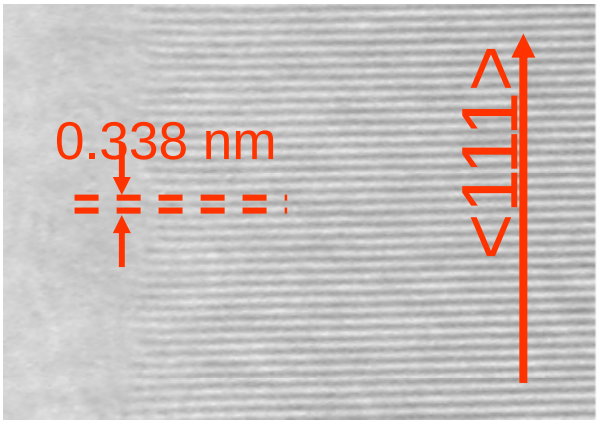
SEM images of vertically aligned InP nanowires grown on Si (111)





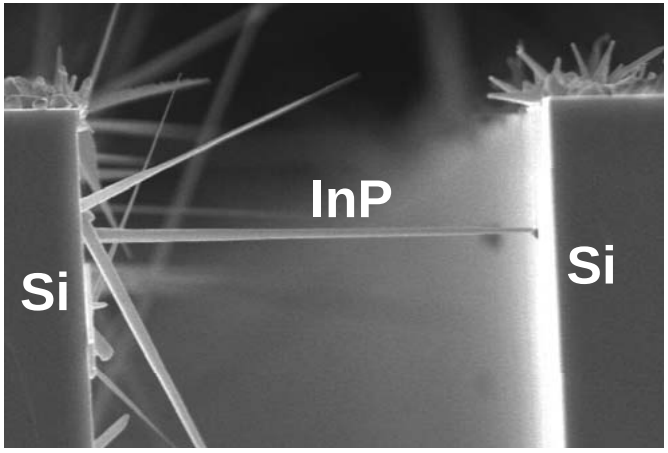


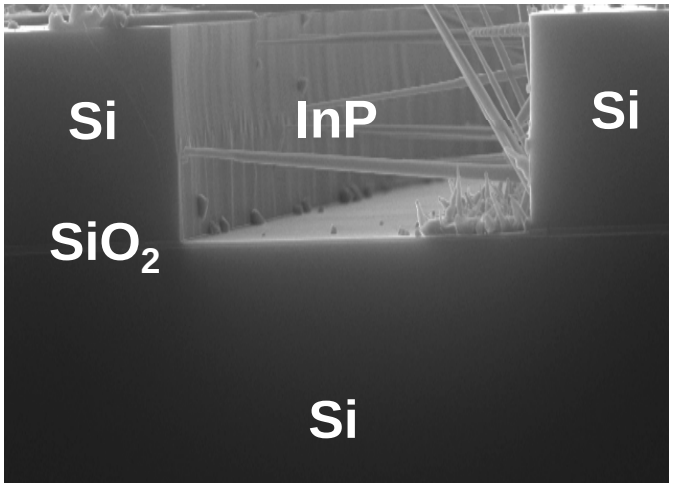
Yi, Girolami, Amano, Sharma, Kamins, Kimukin, Islam, ***IEEE Nano 2005***



Non-epitaxial nanowires are entangled despite perfect crystal quality & uniform diameter

InP Nano-Bridges Between Si Electrodes

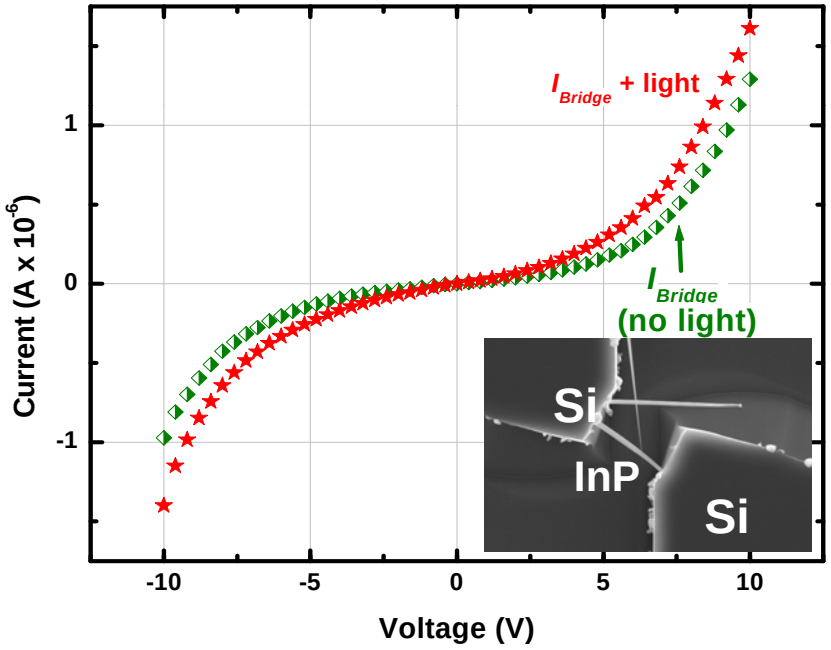




Yi, Girolami, Amano, Sharma, Kamins, Kimukin, Islam, *APL*, 89, 133121, 2006.

Goals:

- Si Photonics (Laser, LED, PD, displays etc)
- Ultra-fast III-V devices integrated with Si CMOS (HEMTs, FETs, mixers etc >100GHz speed)

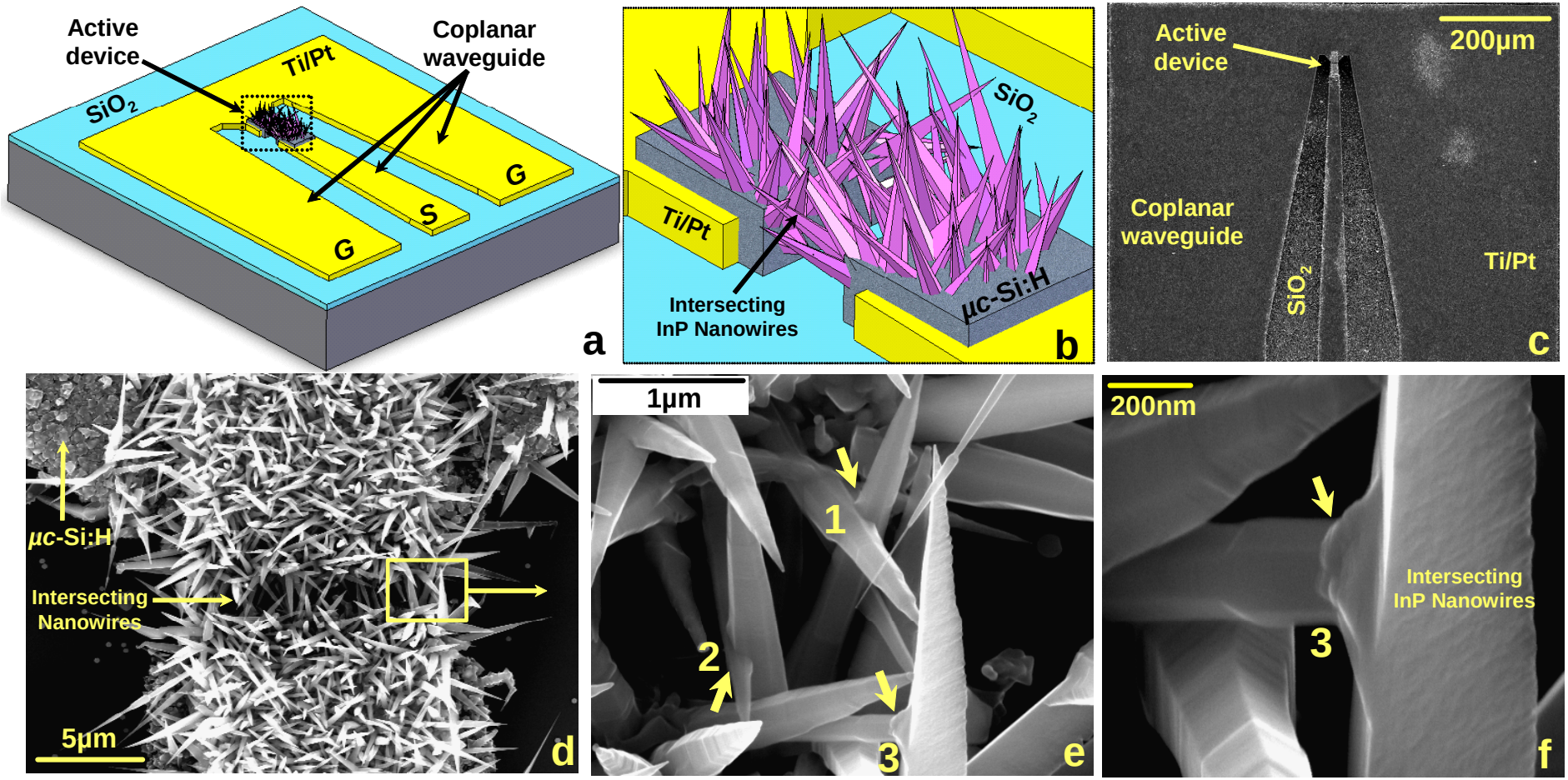


Challenges::

- Interface barrier due to bandgap and workfunction mismatch
- Growth of ternary and quaternary
- Orientation and position of III-V on Si

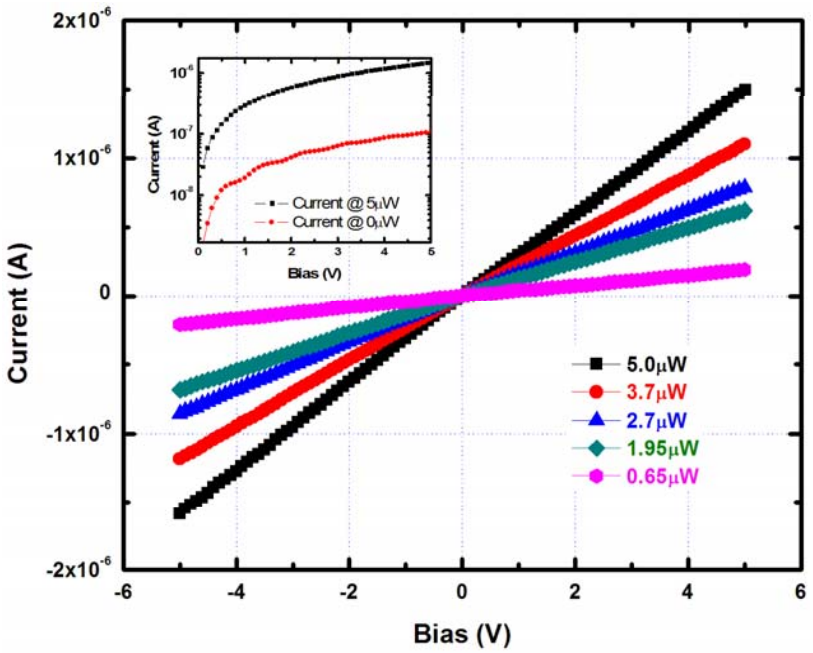
Growth of III-V Nanowires on Amorphous Surfaces

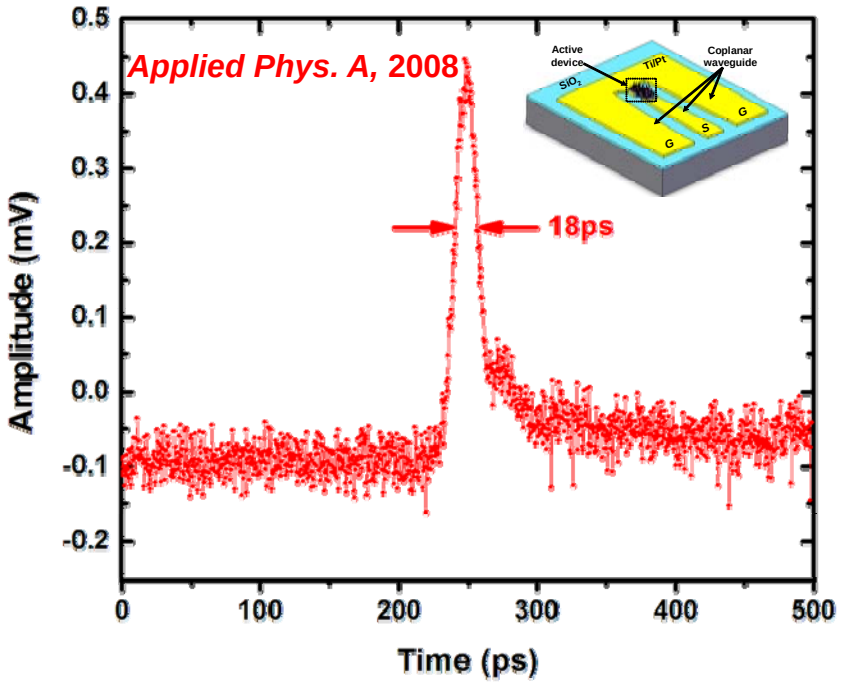
Ultra-fast NW photoconductor on Quartz



Applied Phys. Lett. 91 113116 (2007).

Ultra-fast NW photoconductor on Quartz



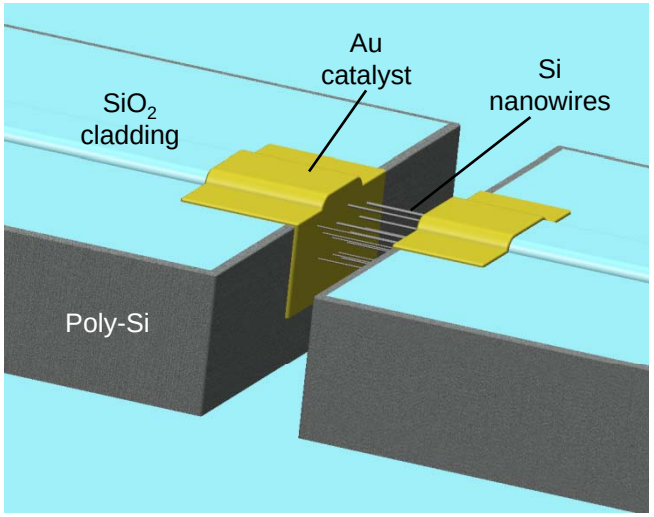


- The measured FWHM from the oscilloscope was 18 ps
- 11.2 ps FWHM response for the 40-GHz oscilloscope and the laser pulse width of 1 ps
- The device temporal response is estimated to be **14 ps** at 780nm

$$\tau_{meas} = \sqrt{\tau_{actual}^2 + \tau_{scope}^2 + \tau_{optical}^2}$$

K. Rush, S. Draving, and J. Kerley, IEEE Spectrum **27**, 38 (1990).

Waveguide-Integrated Nanowire Photoconductors on a Non-Single Crystal Surface



Vertical walls provide

- Mechanical support for bridging NW
- Electrical contact through Poly-Si film
- Optical pathways

Poly-Si film performs as:

- Seed layer for crystalline growth
- Electrical contact

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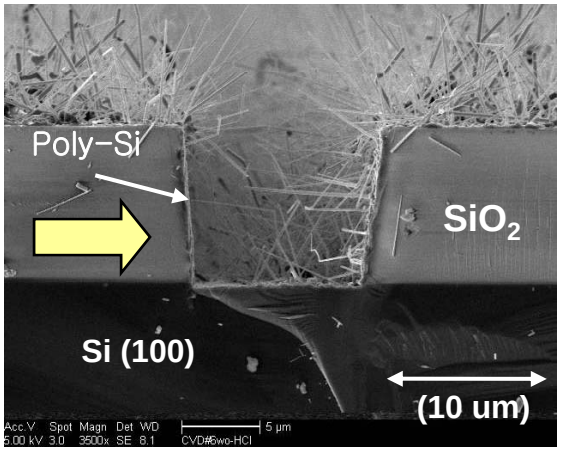
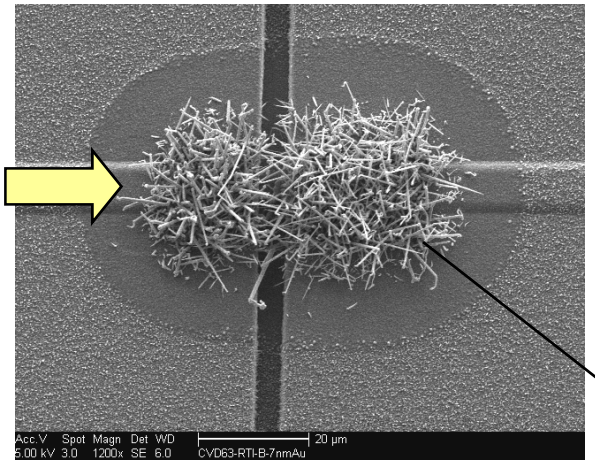
Growth on angle-deposited Au catalyst

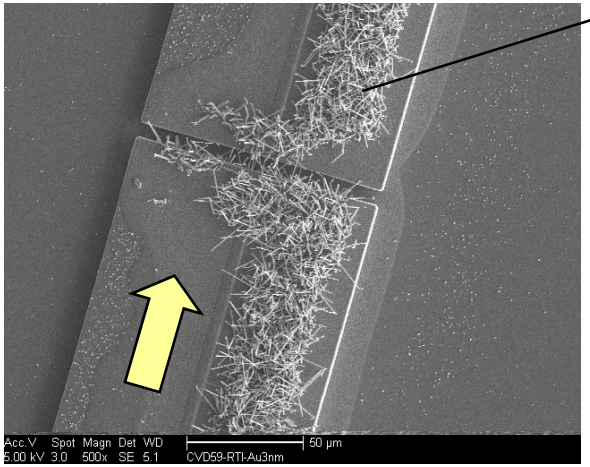


Cross-section of thermal oxide trench device

Waveguide-integrated devices



WG core



Different Au patterns:
A trade-off between growth requirement and electrical signal background.

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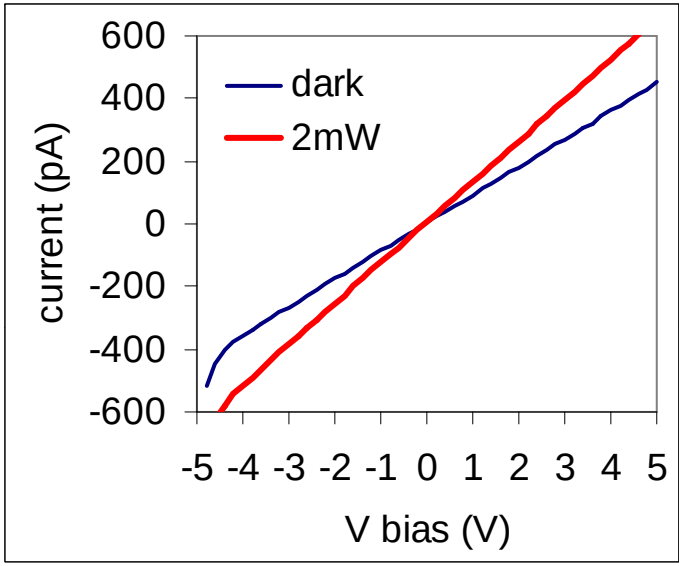
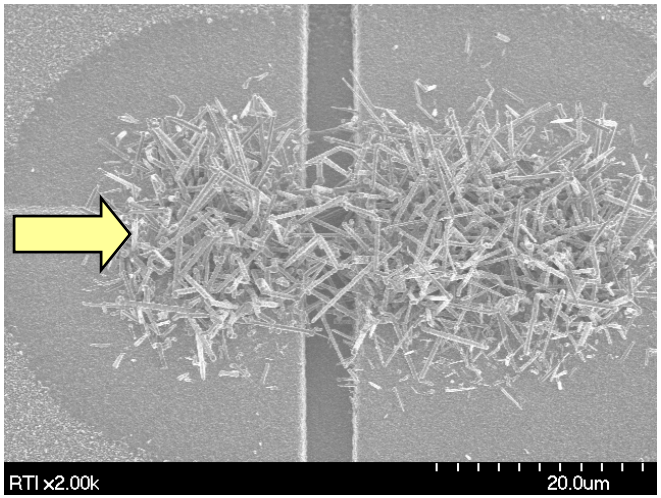
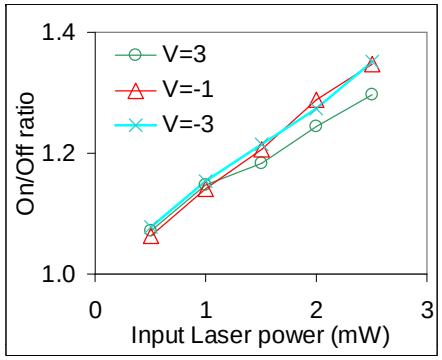
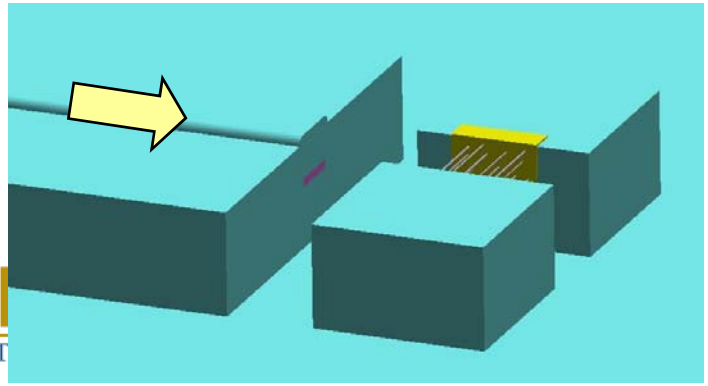
Photoresponse of edge-illuminated nanowires (I)

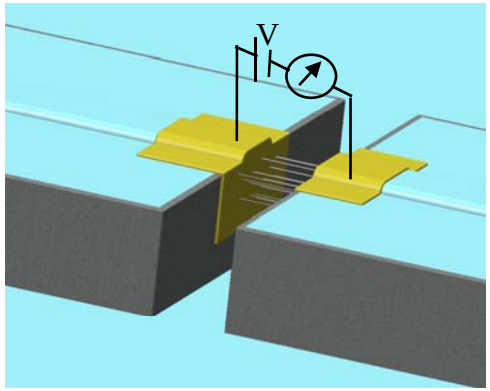


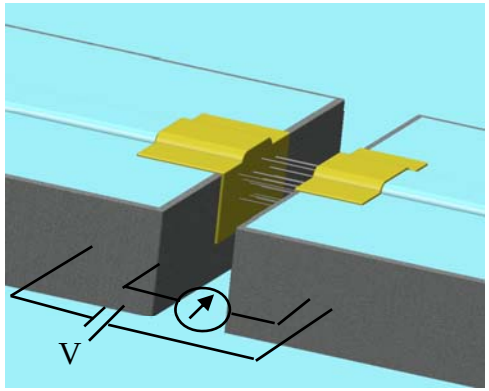




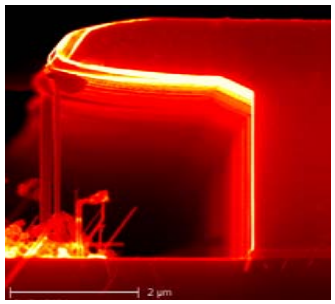
- On/Off Ratio ~ 1.35
- Sample had poor optical transmission due to scattering

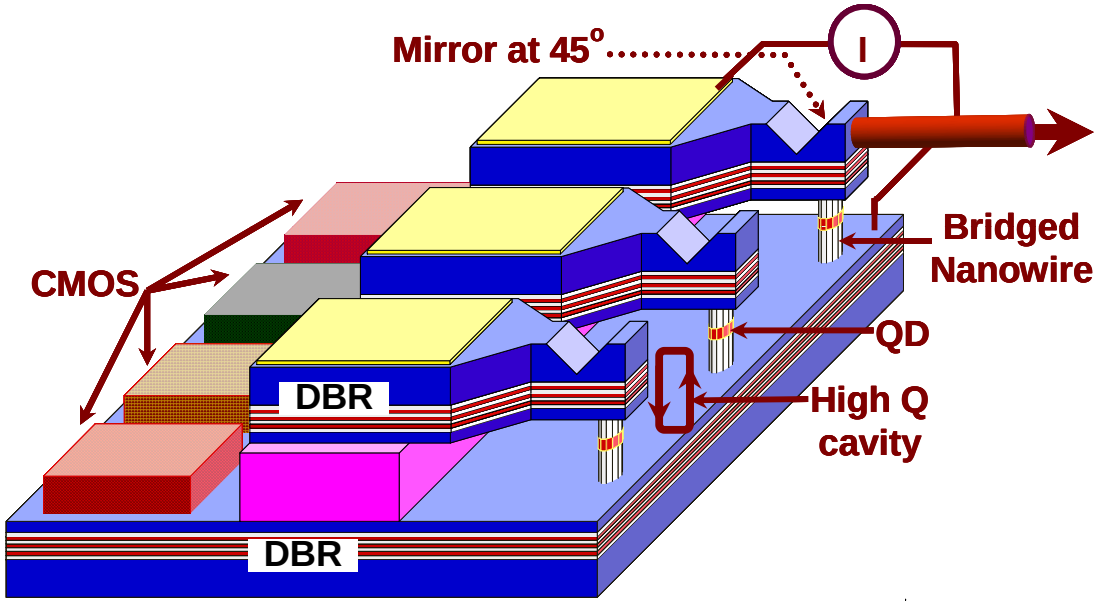


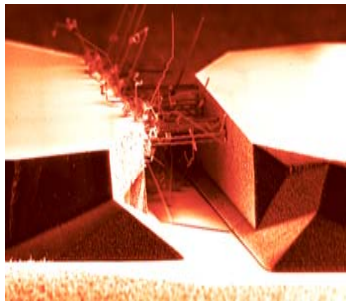


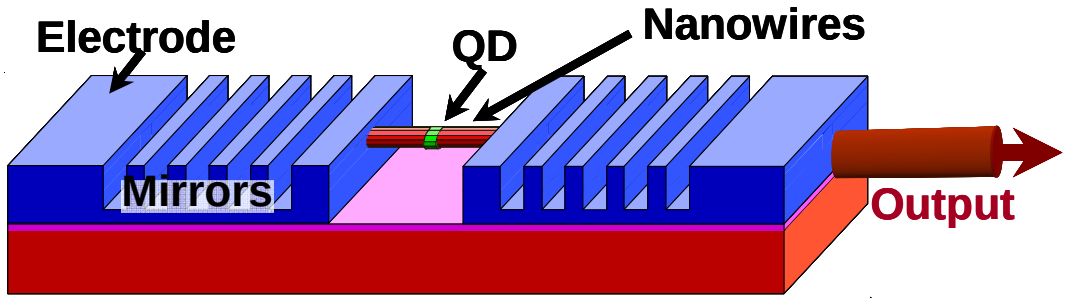


Opportunities for Novel Devices



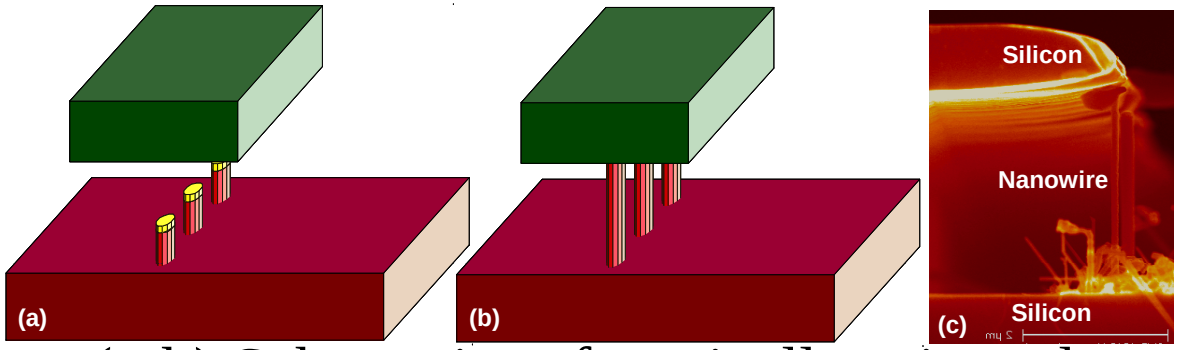




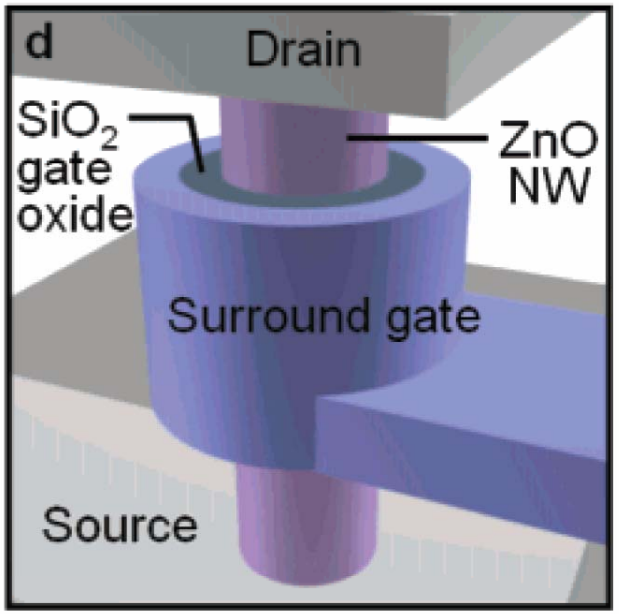


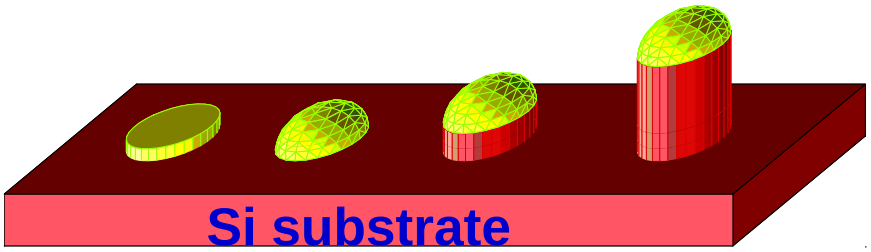
Lateral QD laser on Si and III-V wafer

Nanowires for Massively Parallel Interconnects

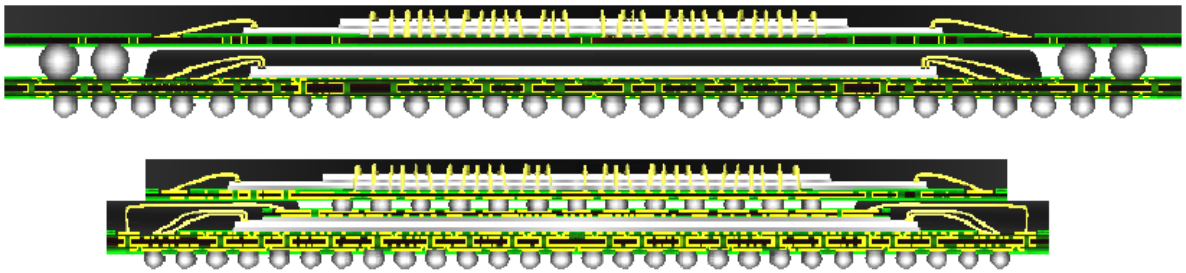


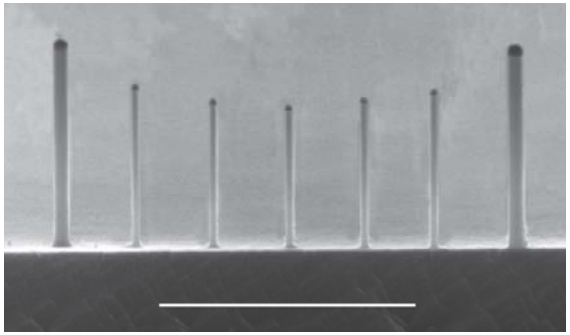
(a-b) Schematics of vertically oriented nanowires grown and bridged between two lateral surfaces. (c) Experimental demonstration with Si nanowires.

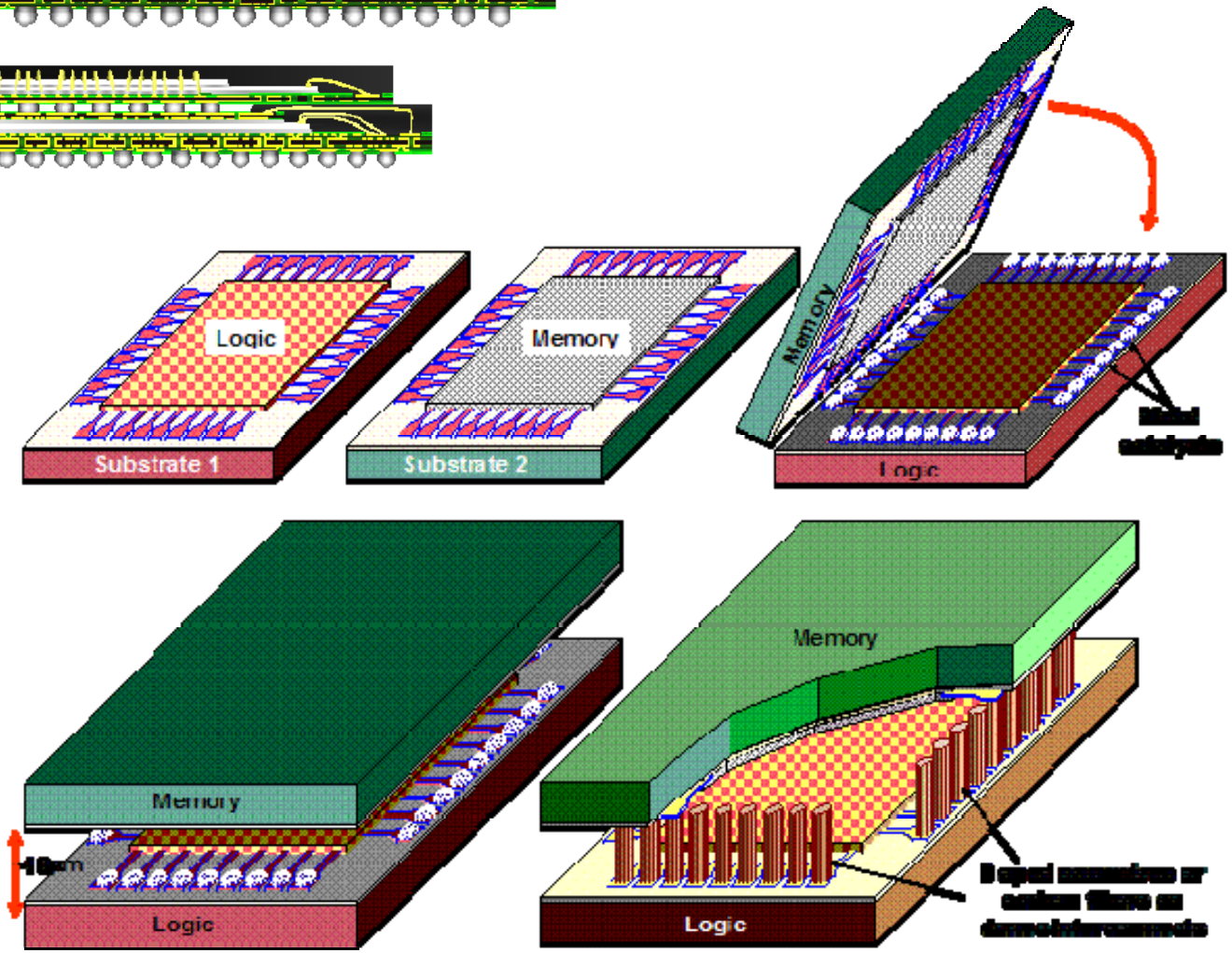




Nanowires for Multi-Layer Chip Stacking

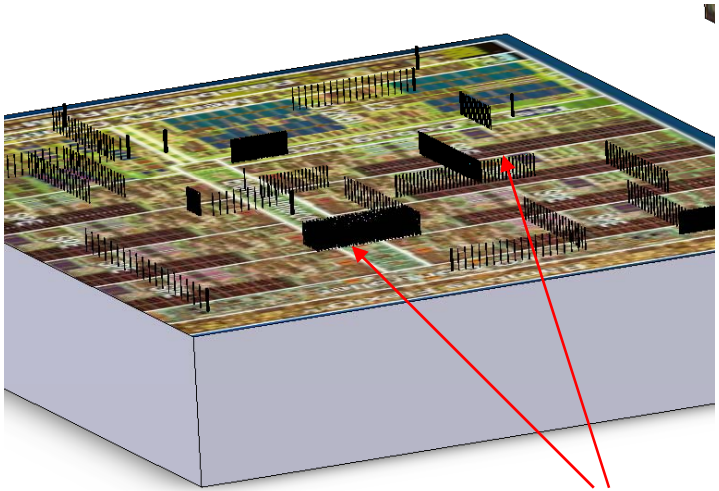


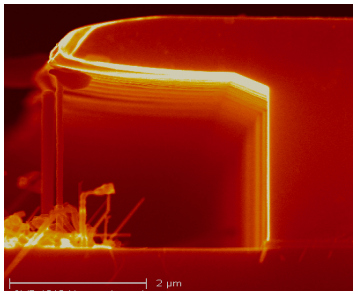


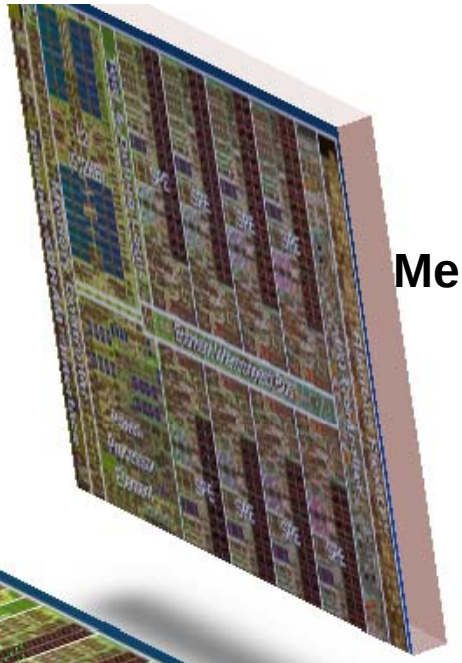


Borgstrom et. al., 2007

Processed Chips Bonded Using Nanaowires



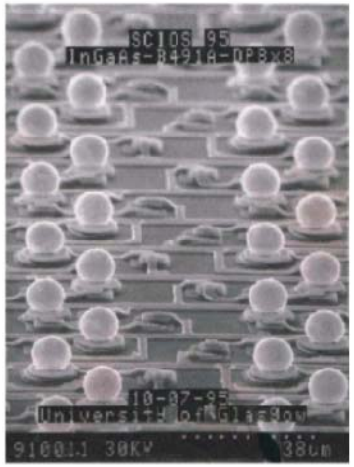


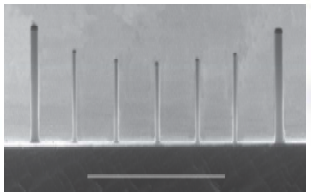


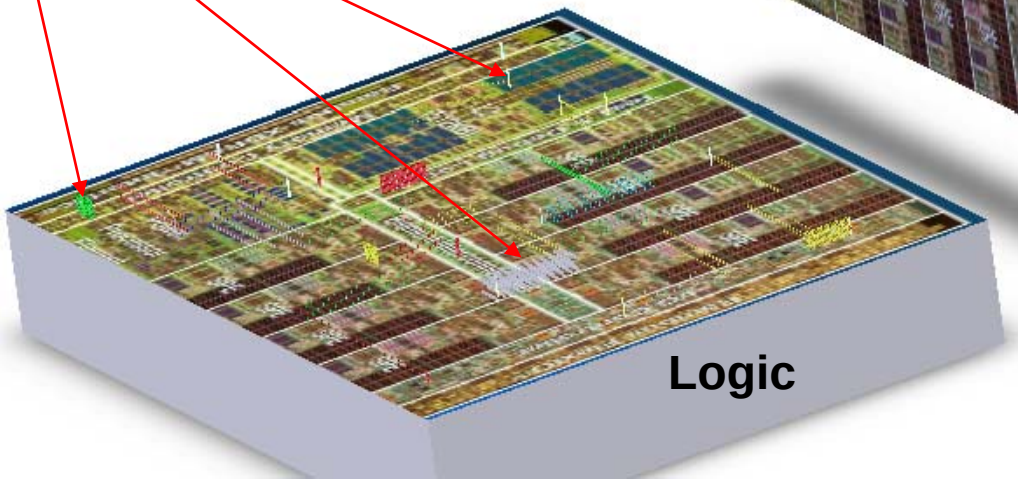
Memory

Nanowires

Solder bumps

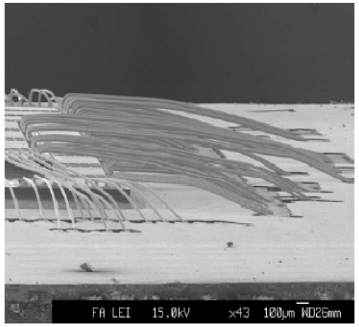


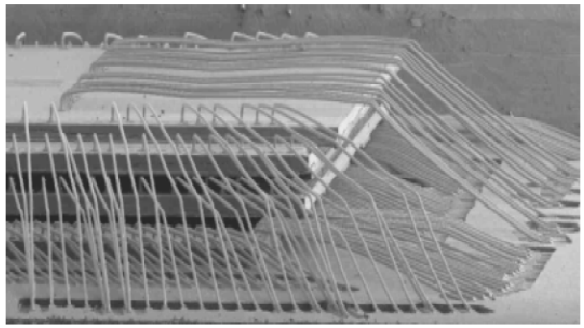


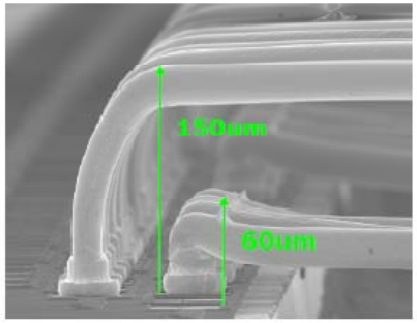


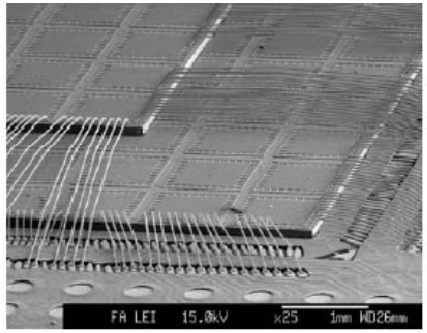
Logic

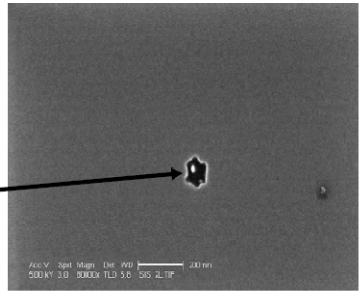
Vertical Interconnects in Vias





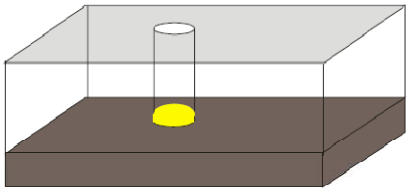




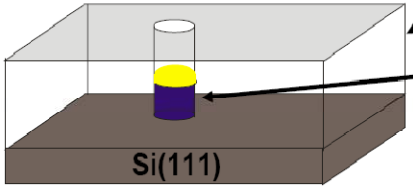


Au catalyst isolated on Si within 25 nm thick SiO_2

Catalyst such as Au/Ge eutectic in via



VLS Growth of Ge or Si



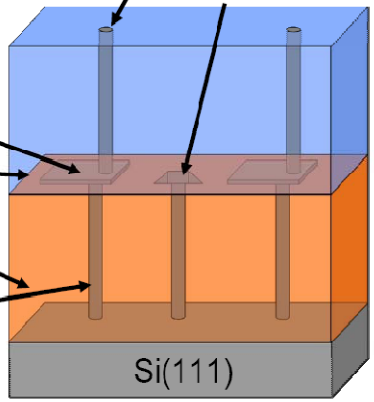
Liquid phase epitaxy of GOI

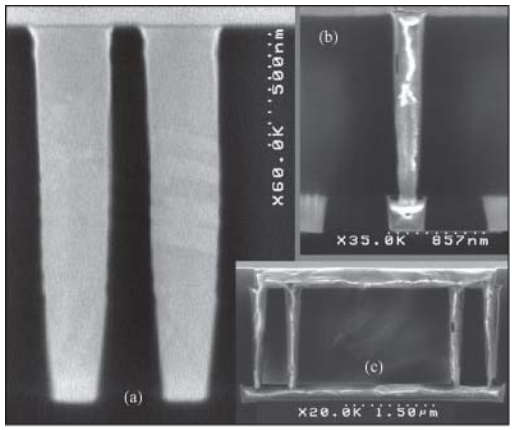
SiO_2

VLS-Grown Ge or Si NW

Single crystalline Ge seed

Ge CVD homoepitaxy



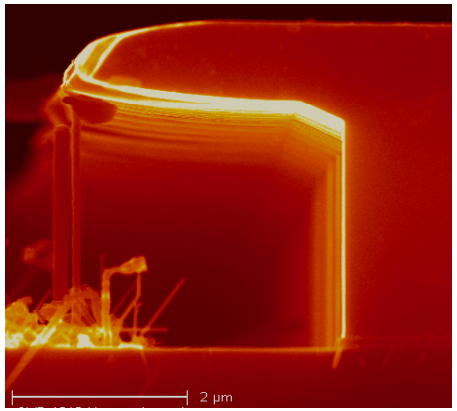


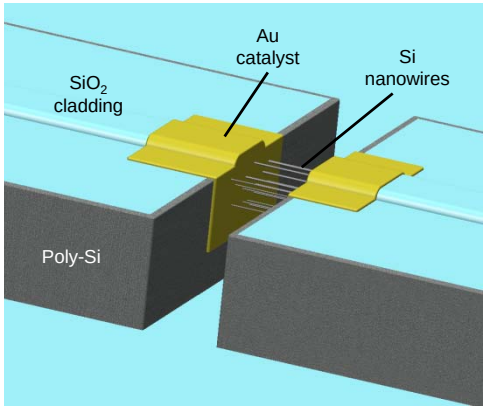
IBM

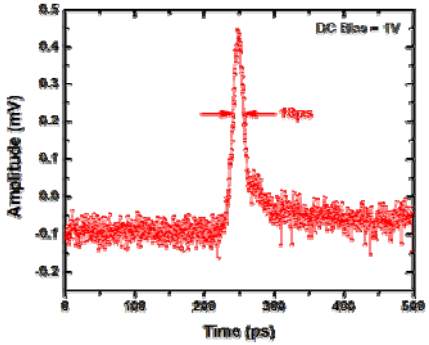
Paul C. McIntyre, Stanford University

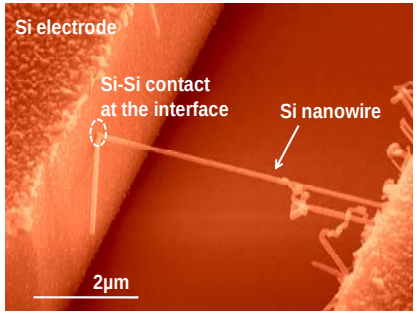
Summary

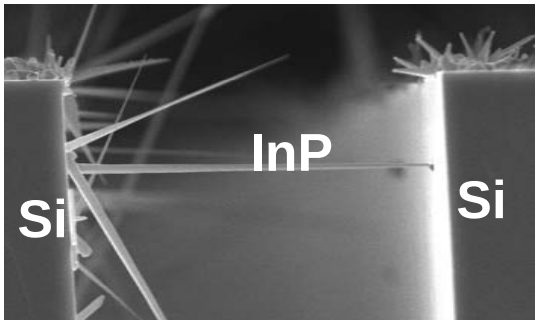
- **Semiconductor nanowires can overcome issues of heteroepitaxy Enabling Devices for Si Photonics**
- **Nanowires can be used as short range electrical interconnects**











Thank You