Optical Proximity Communication for a Silicon Photonic Macrochip

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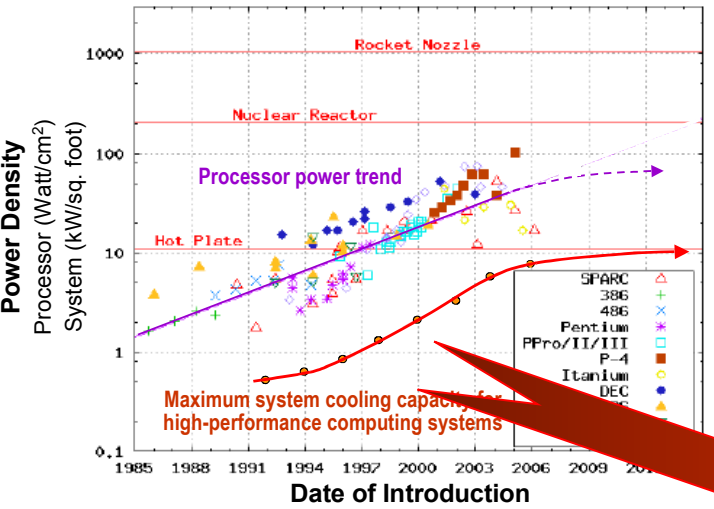
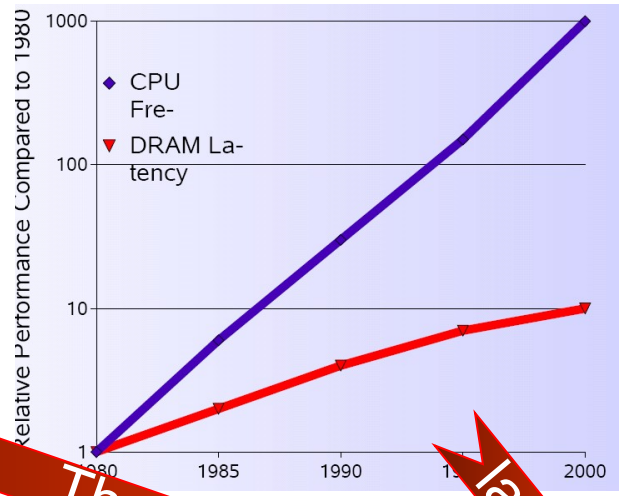
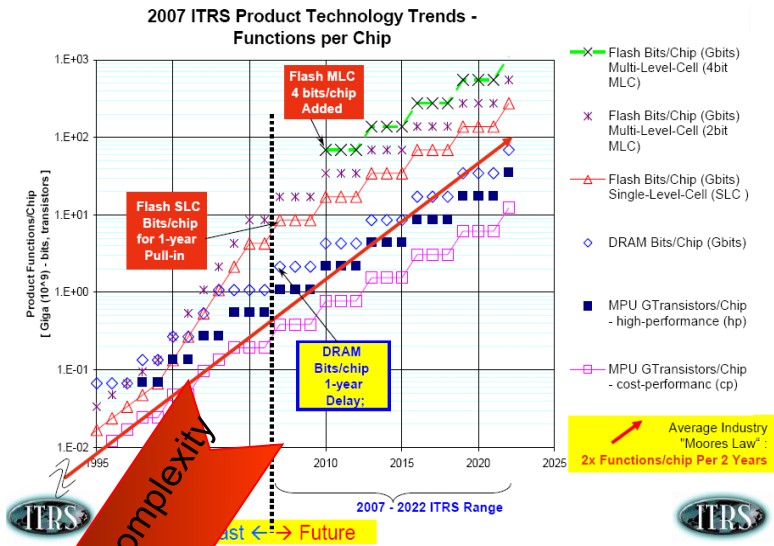
Outline

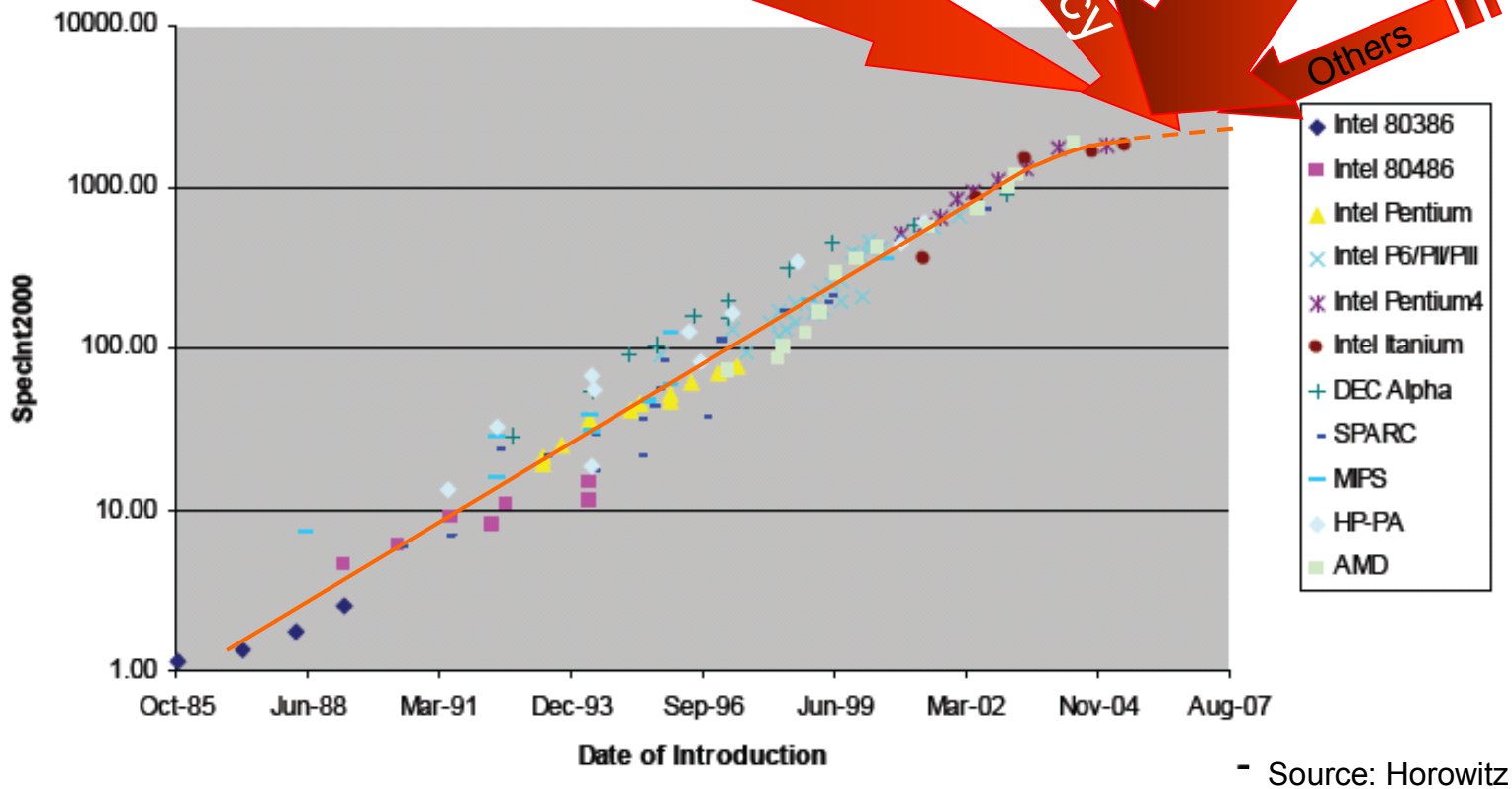
- Background and motivation
- Macrochip
- Optical proximity communication
- Packaging with new chip alignment technology
- WDM point-to-point network for multi-chip interconnects
- Device requirements and consideration
- Summary

Moore's law is leveling off for single core processors…





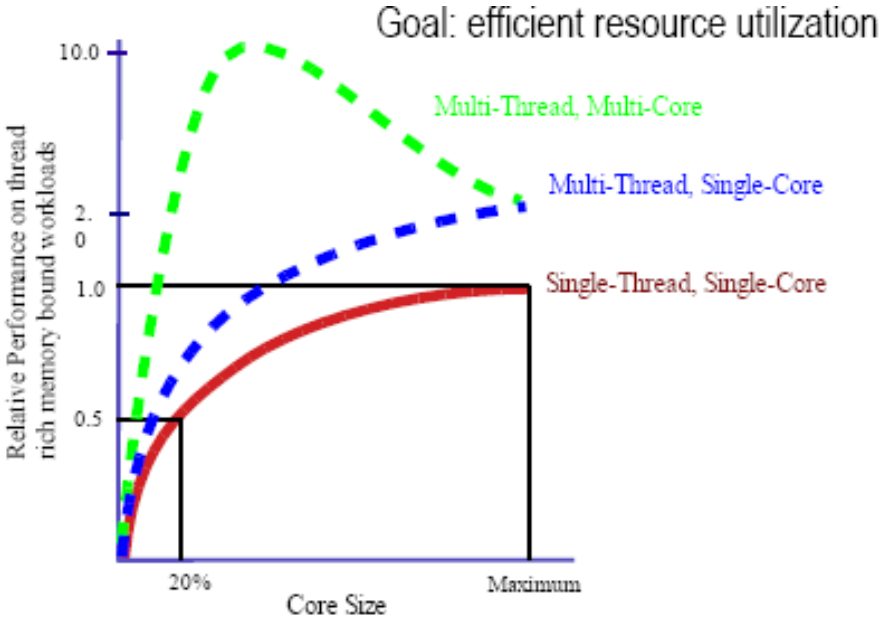




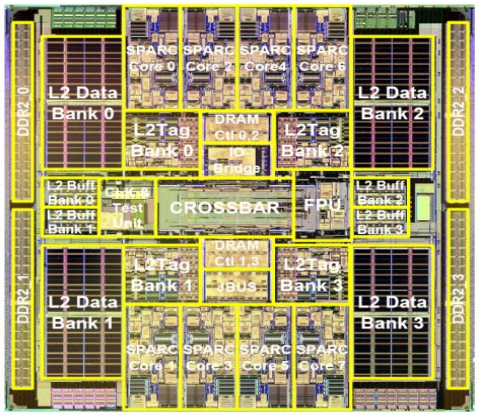
- Source: Horowitz et al., "Scaling, power, and the future of CMOS," IEDM 2005

Continuing Moore's Law scaling

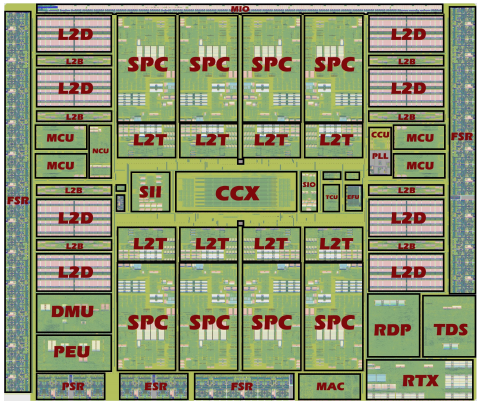
- Multi-core and CMT
  - CMT = chip multi-threading
  - Efficiently use chip area
  - But chip real estate is precious
  - Multicore die at the reticle limit



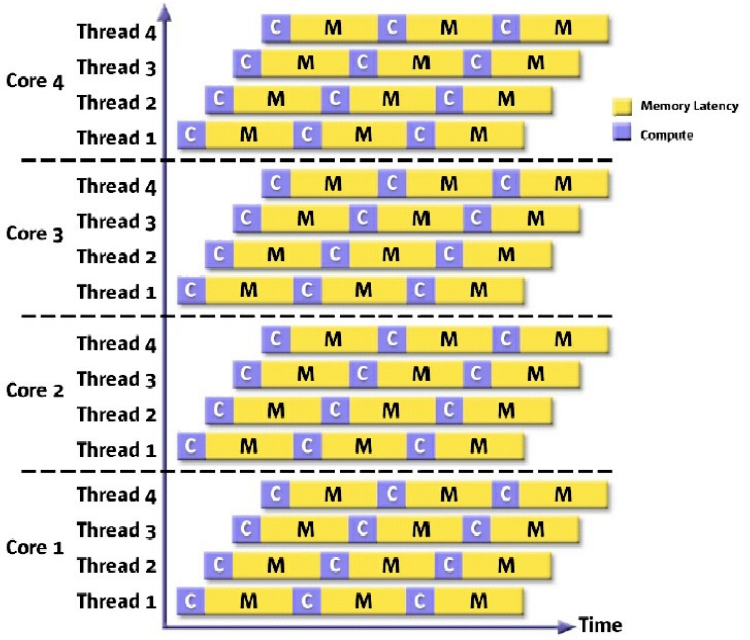
S. Manish et al., ASSCC '07. IEEE Asian 12-14 Nov. 2007



Niagara 1: 8 cores, 32 threads

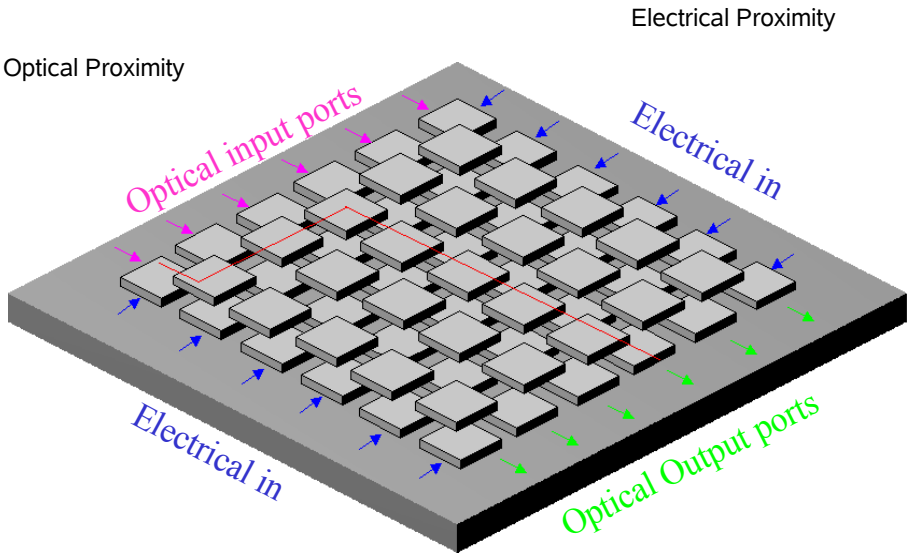


Niagara 2: 8 cores, 64 threads

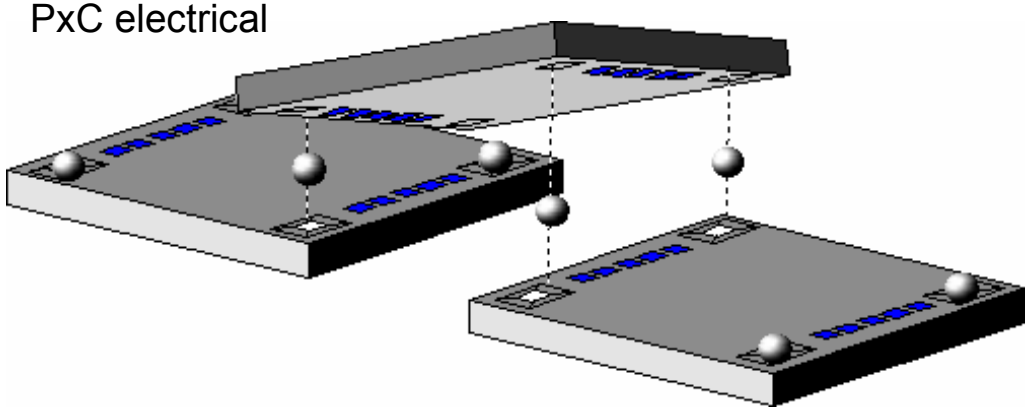


Multichip arrays with optical routing

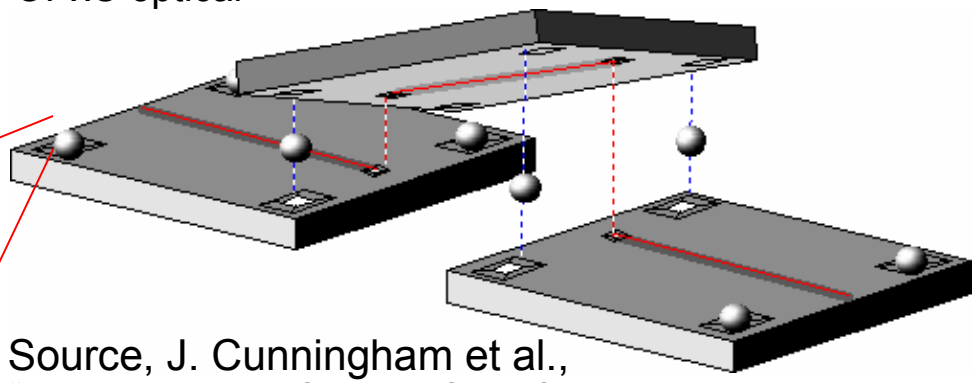
- "Macrochip": a logical big die made of small chips
- Breaks the reticle limit to provide enormous Si real estate
- Transparent optical routing fabrics
  - > Enabled by optical proximity communication (OPxC)



PxC electrical

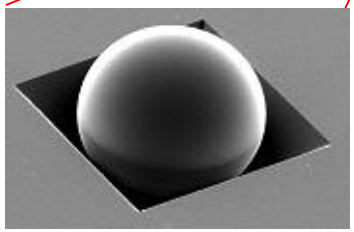


OPxC optical



Bandwidth density projections

- Serdes: 50 Gbps/cm^2
- PxC: 50 Tbps/cm^2
- OPxC: 10 Pbps/cm^2



Spherical ball in pyramidal pit for alignment

Source, J. Cunningham et al., "Aligning chips face-to-face for dense capacitive and optical communication", IEEE TAP, in press

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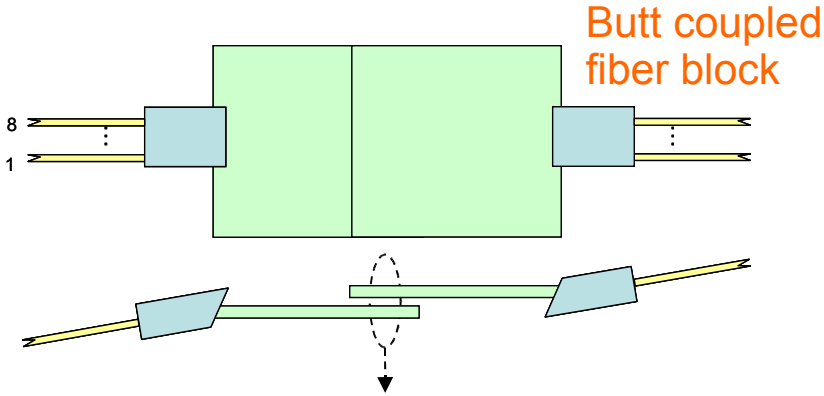
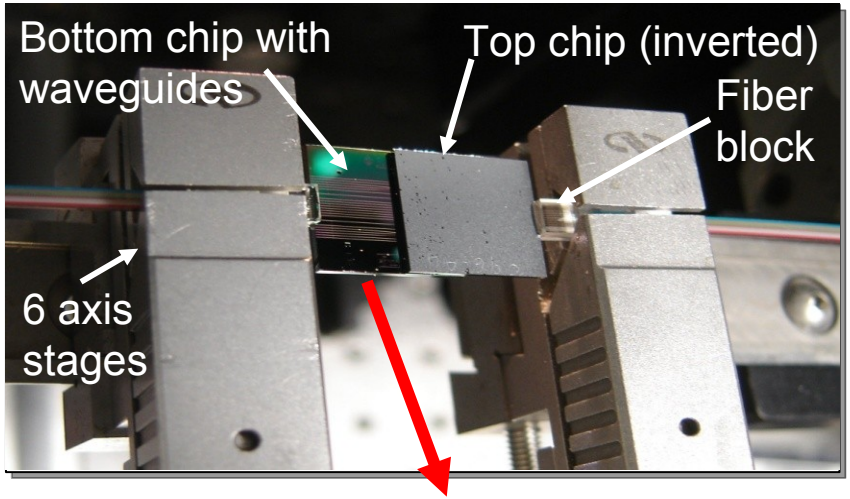
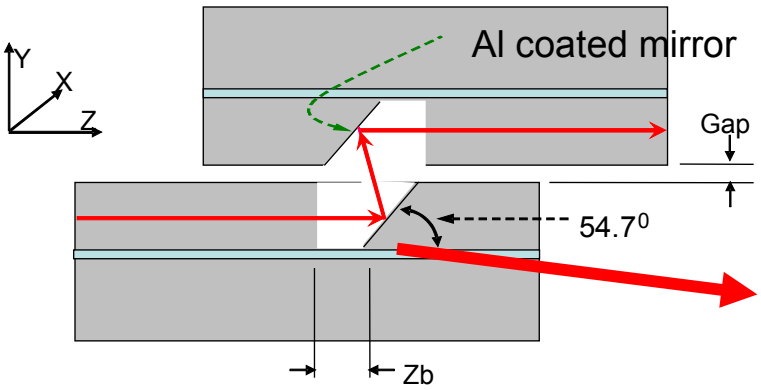
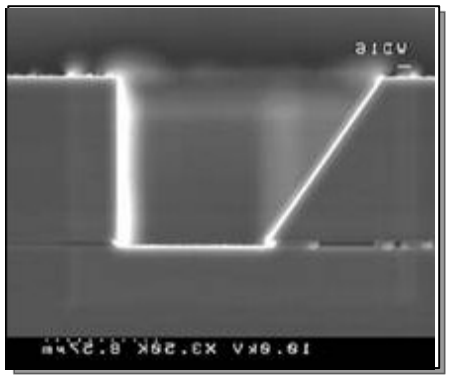
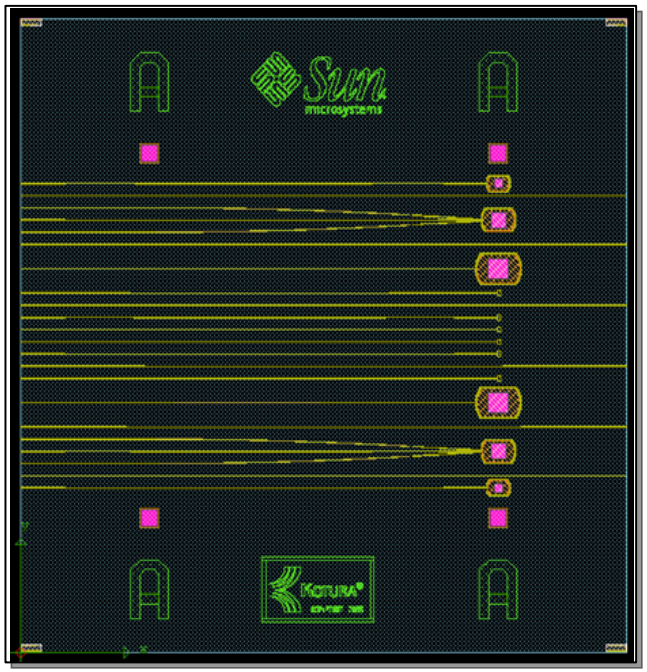
Experimental setup: face-to-face chips











X. Zheng et.al. , Optics Express ,2008

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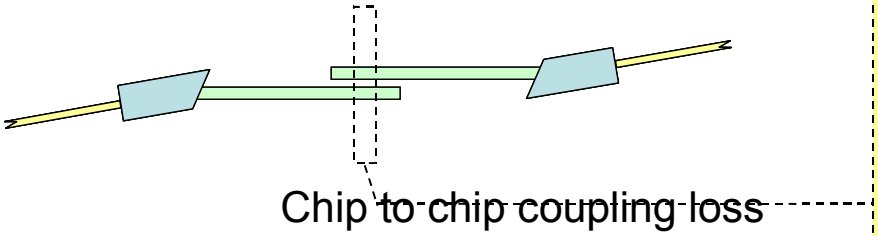
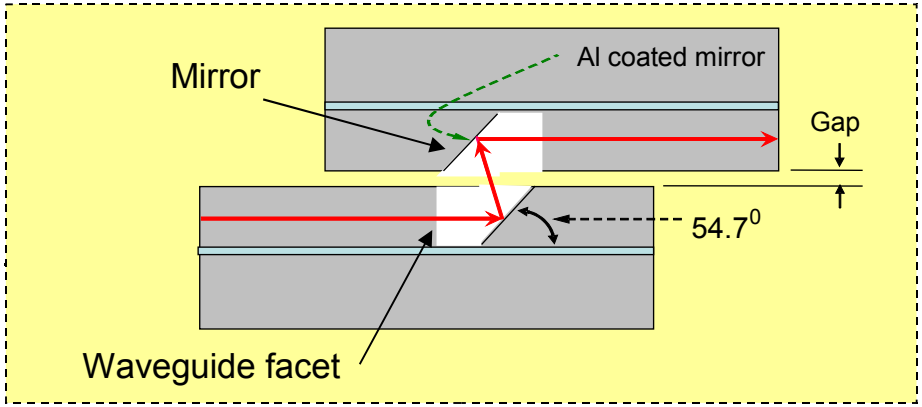
Coupling losses: today vs target





Source of loss	Losses (dB) per chip*		Notes
	Now	Target	
Mirror	0.3	0.2	Metal reflectivity, thin film and roughness improvement
Waveguide facet	0.3	0.25	Roughness facet angle and ARC improvement
Mode mismatch	0.15	0.15	Asymmetric modes, one upside down with respect to the other
Beam divergence	0.75	0.2	Current cavity length is ~66um target to go down to <30um
Total	1.5	0.8	

* Alignment tolerances not included

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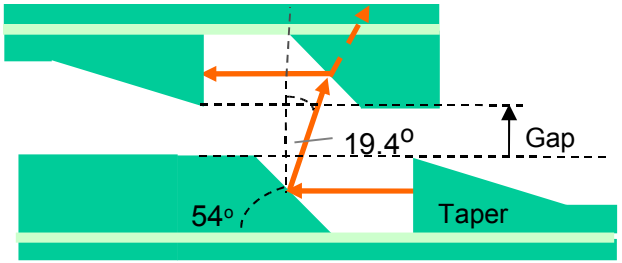
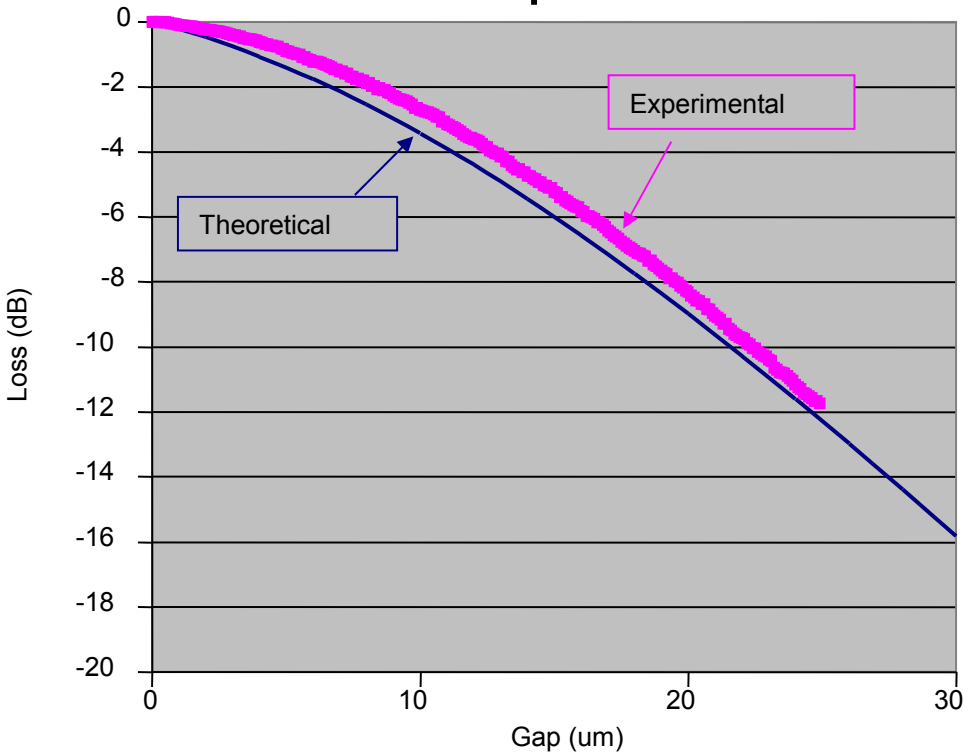
Vertical misalignment tolerance

- Insertion loss increases with chip-to-chip gap
- Depolarized, broadband light source

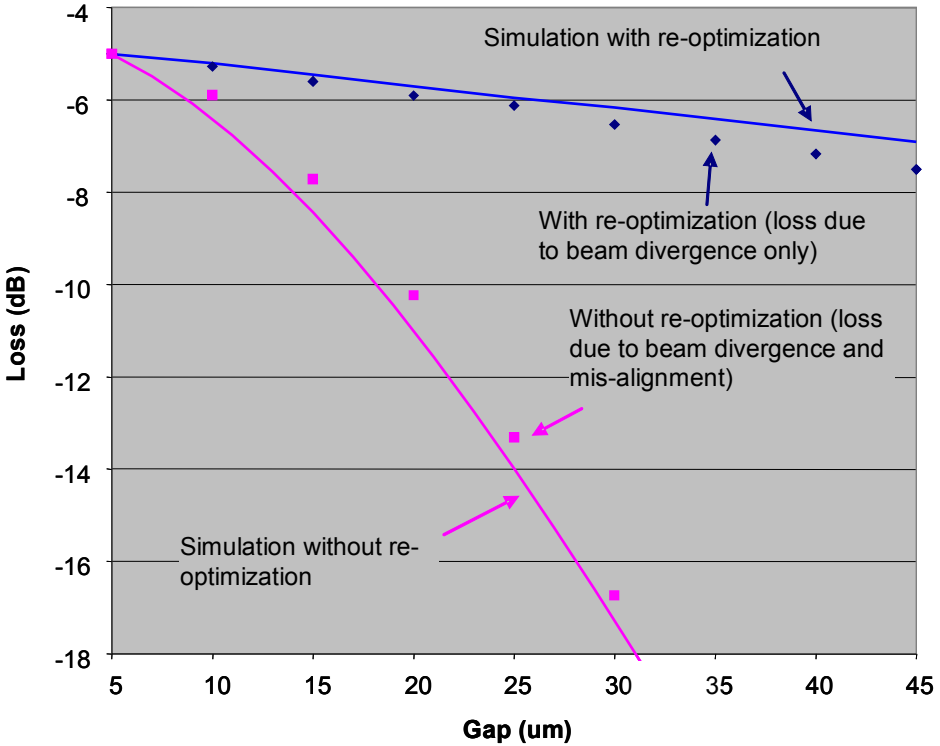


Data normalized to loss at min gap

Un-optimized



Re-optimized



A. Krishnamoorthy et.al., JQE, 2009

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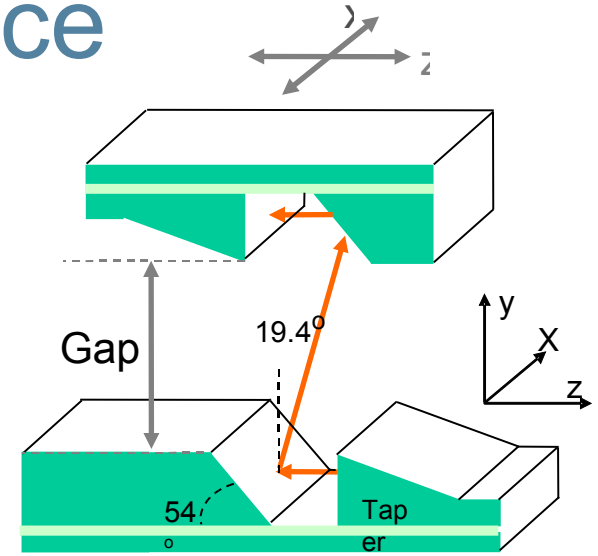
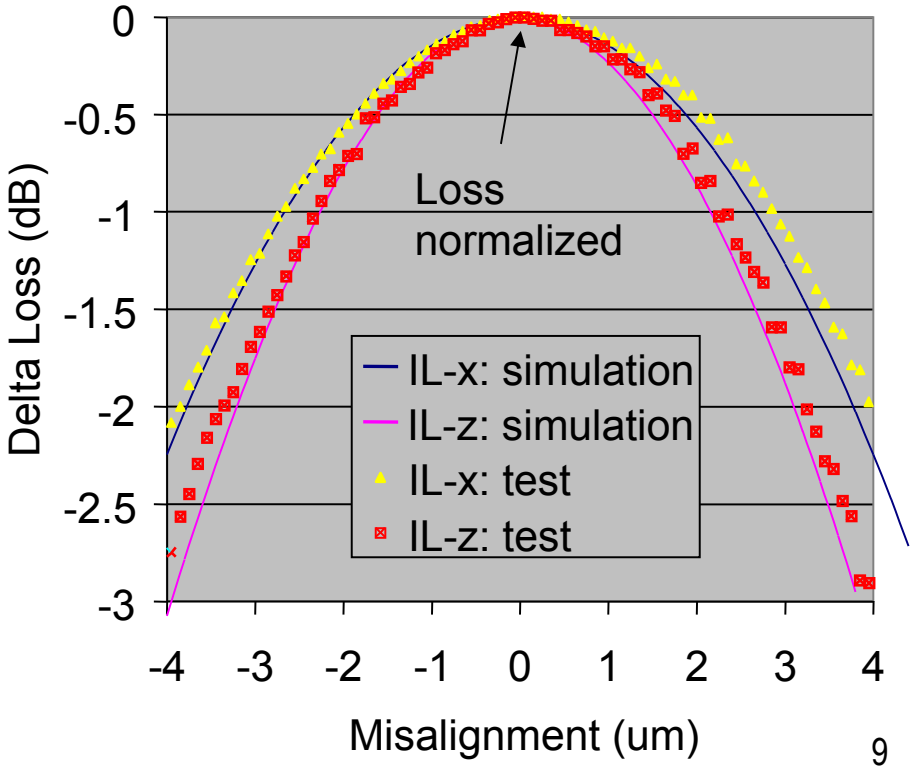
In-plane misalignment tolerance

- Scan chip positions
  - In lateral (in-plane) directions
- Monitor change in the coupling loss
- Results shown at the right, along with simulation
- Simulations assume depolarized broadband light





A. Krishnamoorthy et.al., JQE, 2009

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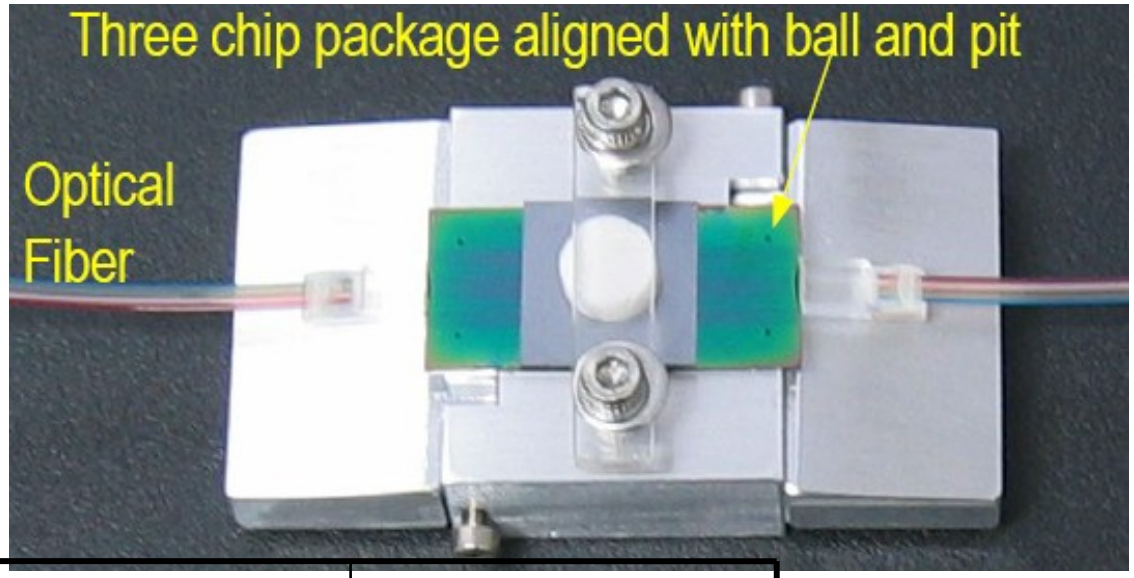
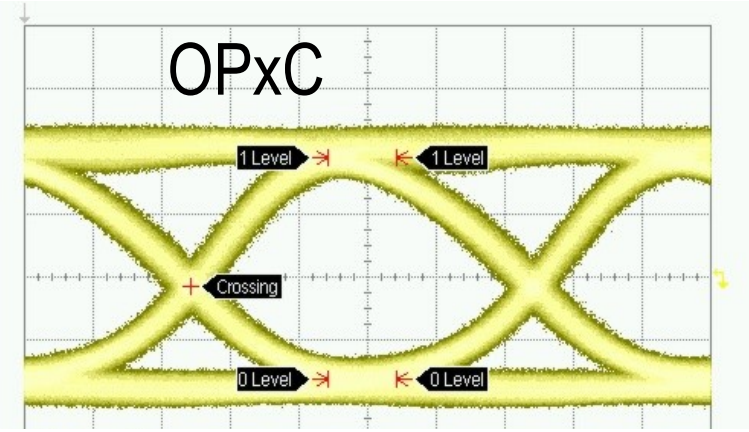
OPxC in a package

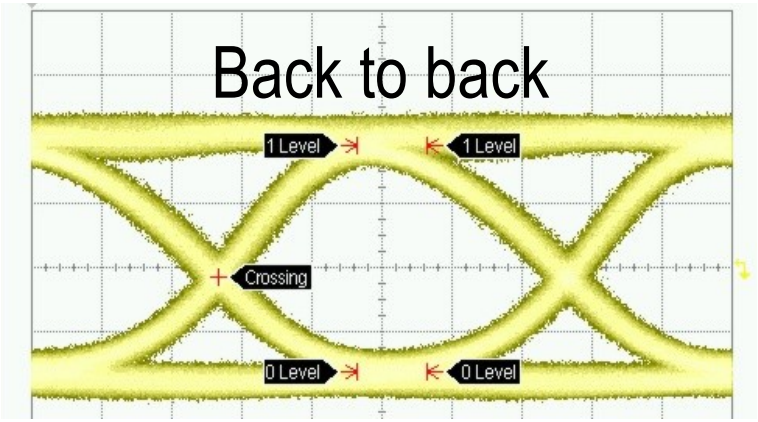
J. Cunningham et.al. Group IV, 2008

- Three aligned chips
  - > Balls in pyramidal pits
- Optical losses 4.0dB
  - > 1 dB more than w/ 6-axis aligner & single OPxC hop



Metric at 10Gbps	Back to back	With OPxC hop
Q (signal to noise)	10.44	10.33
RMS jitter	2.62 ps	2.62 ps





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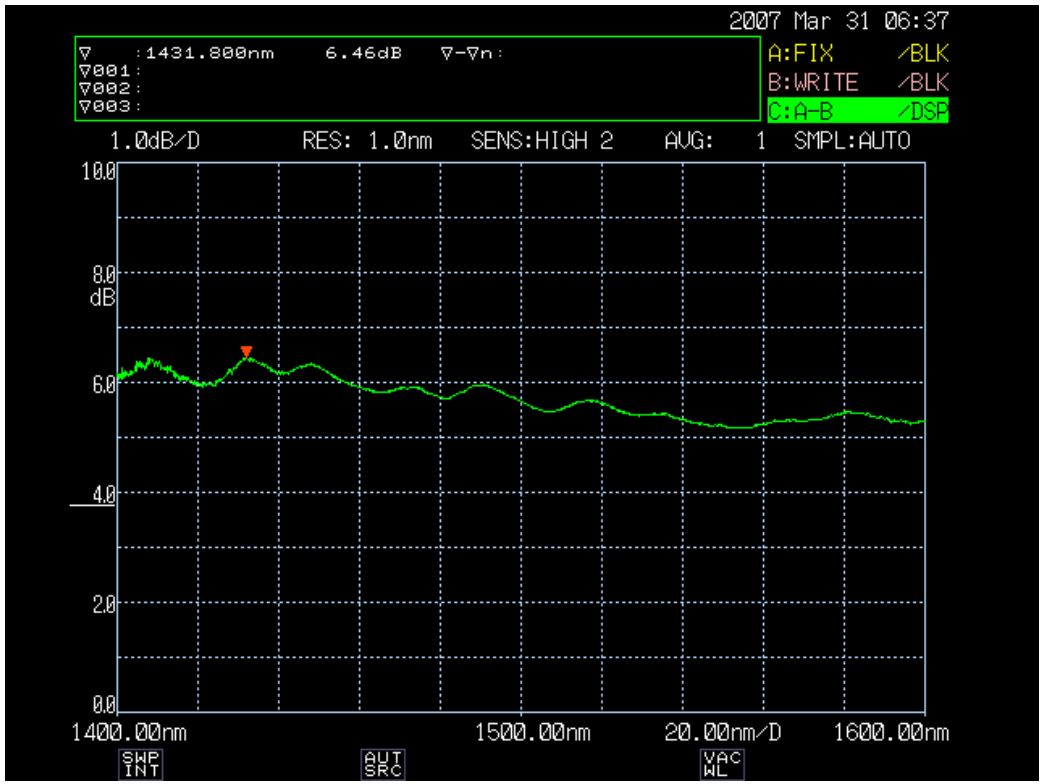
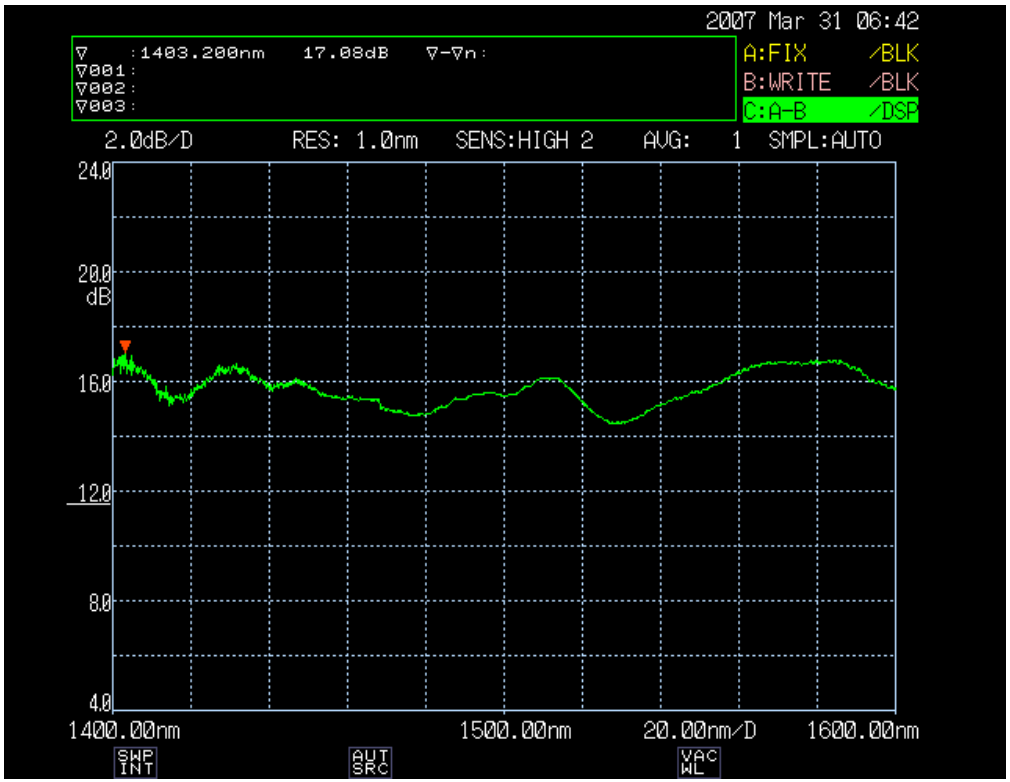
Broadband wavelength coupling

- *Spectral characteristics of OPxC*
- *Transmission versus wavelength*
- *Wavelength Division Multiplexing possible*

One OPxC hop



Two OPxC hops



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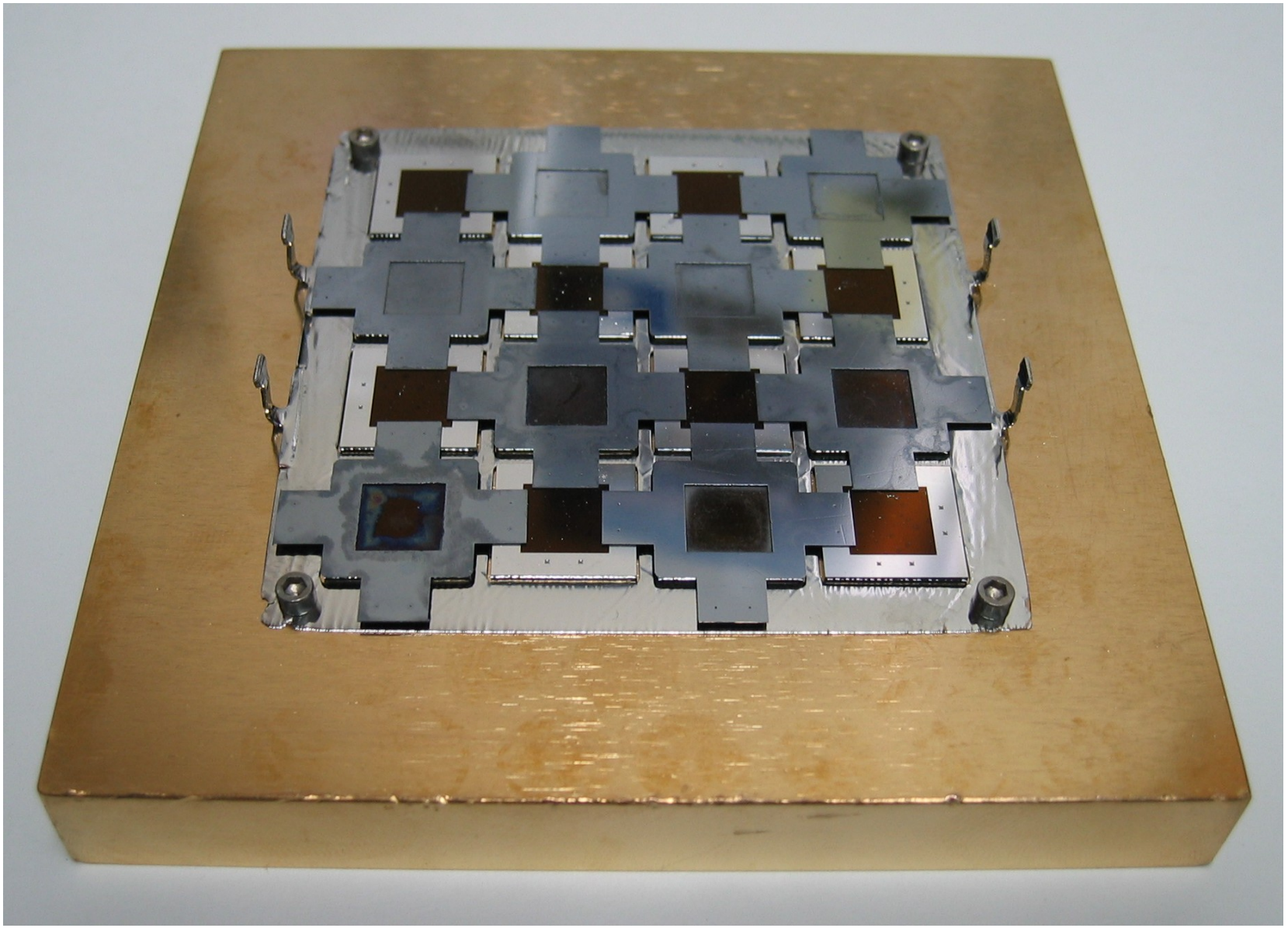
4x4 with 1µm global positioning using ball and pit



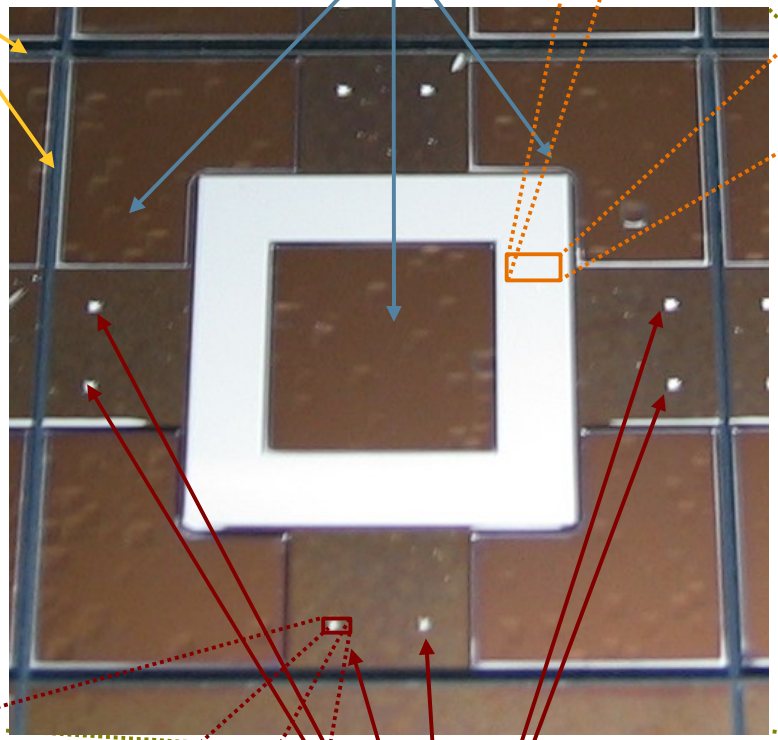
J. Cunningham et al. “Coupled Data Communications”, R. Ho and R. Drost, eds., Springer-Verlag, in press

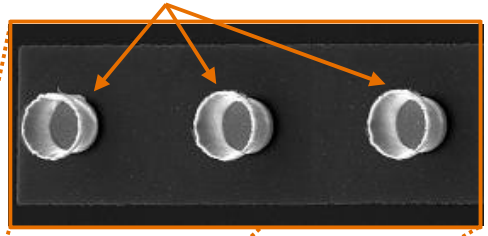
Wafer-scale Fab

micro-bumps

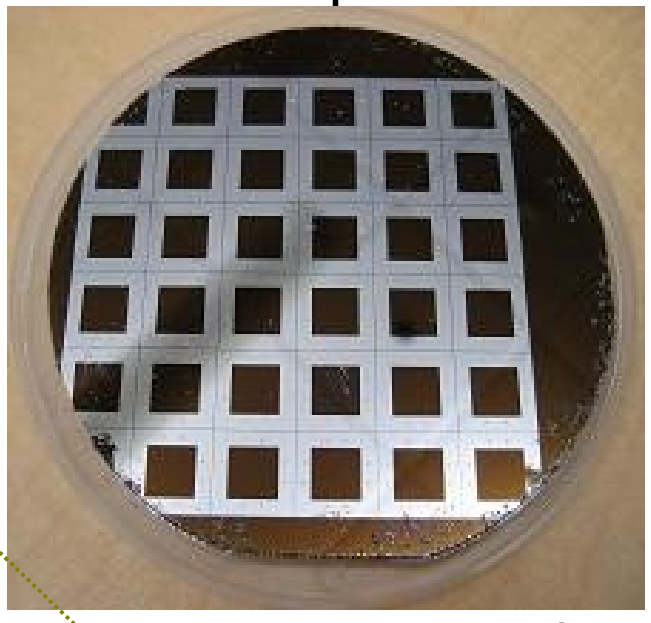
Etched patterns

Saw lanes

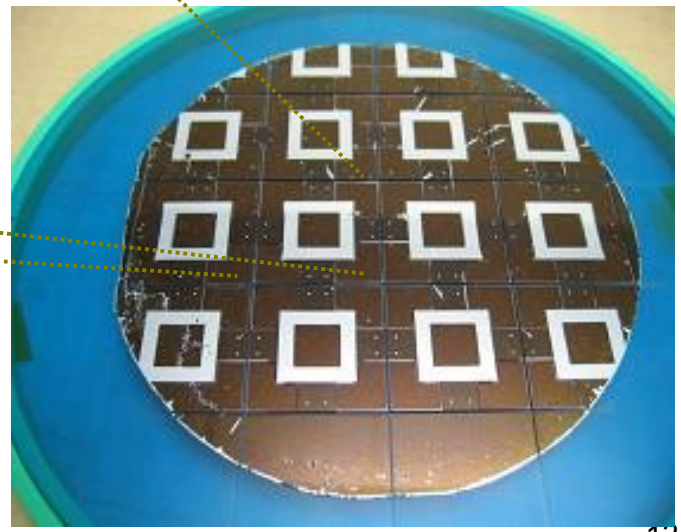


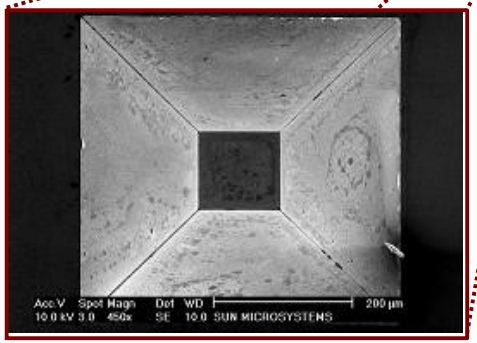


Island Chip Wafer



Sombrero Bridge Wafer

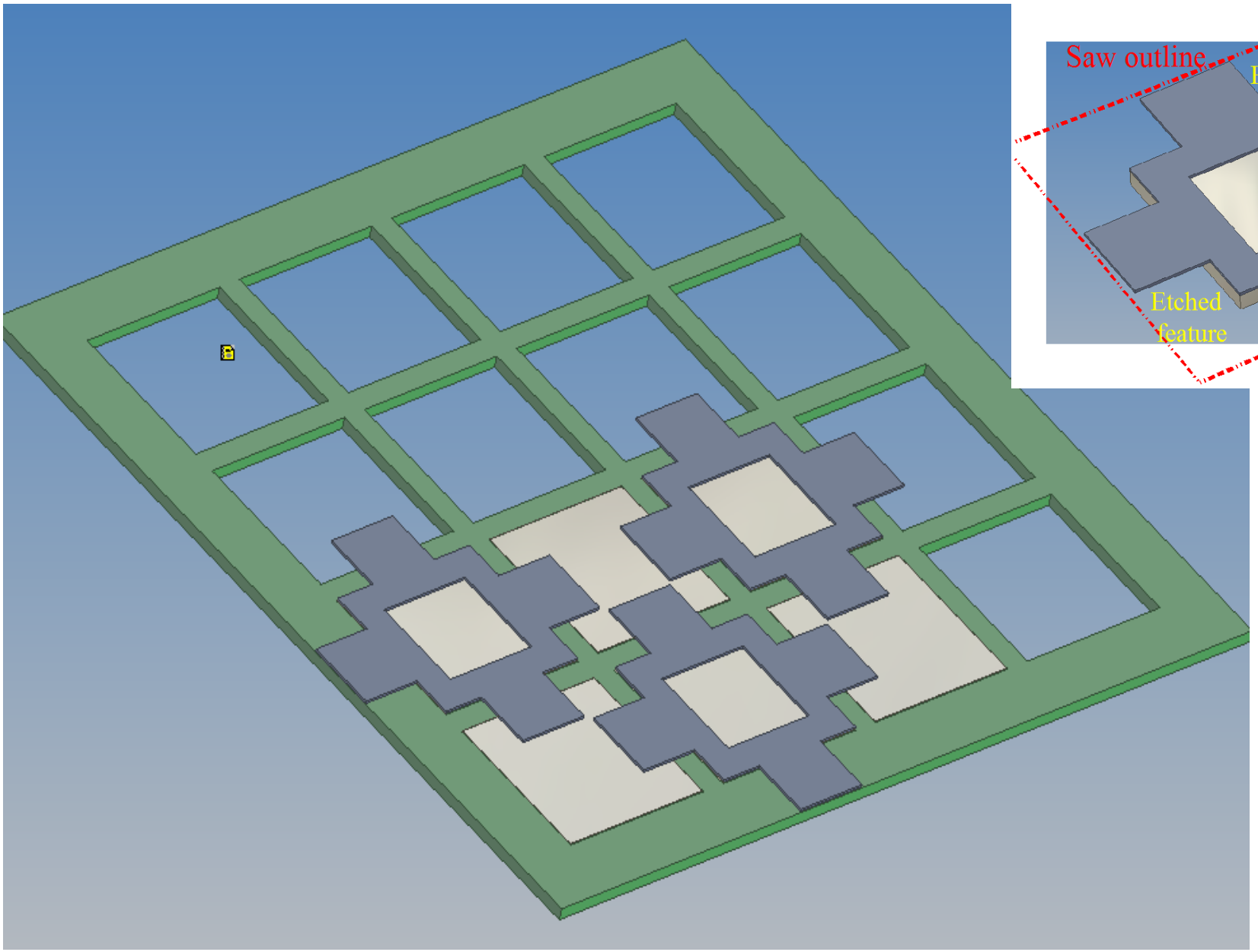


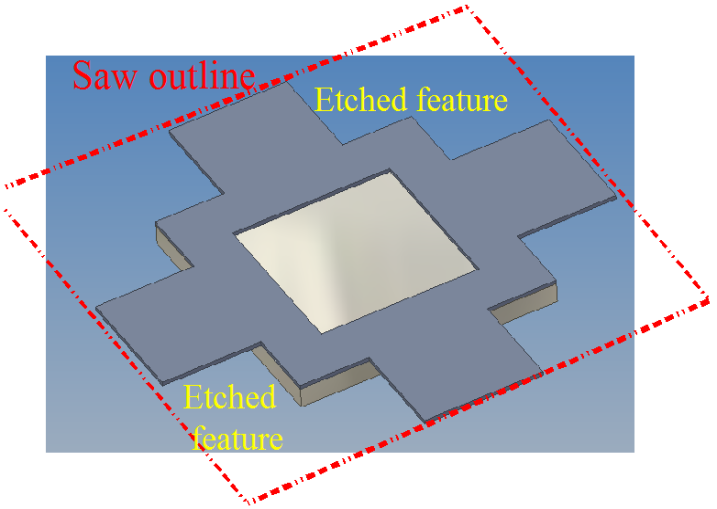


Etch pits

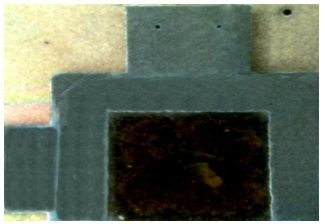
Source, J. Cunningham et al., “Aligning chips face-to-face for dense capacitive and optical communication”,IEEE TAP in press

Chip Lattice for Coarse Alignment

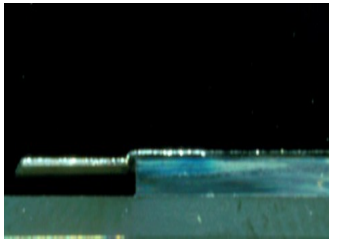




Top View



Side View

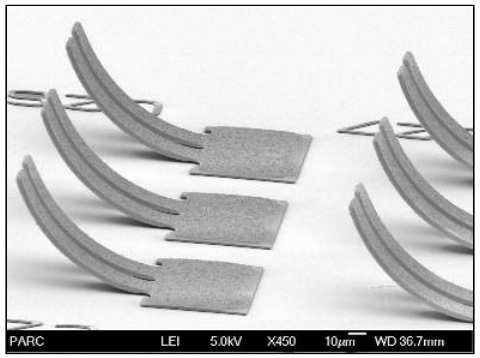


Rematerable Power and Ground: the KGD-MCM problem

PARC Technology

Sacrificial layer etch, spring lift-off and Au-plating

SEM image. Micro-spring interconnects



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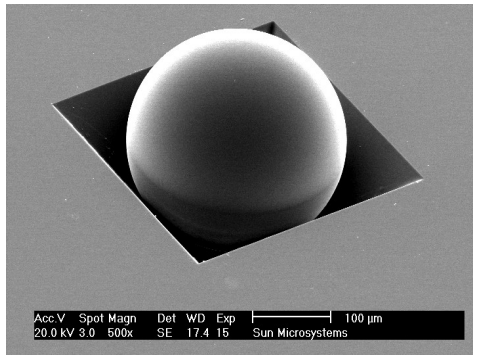
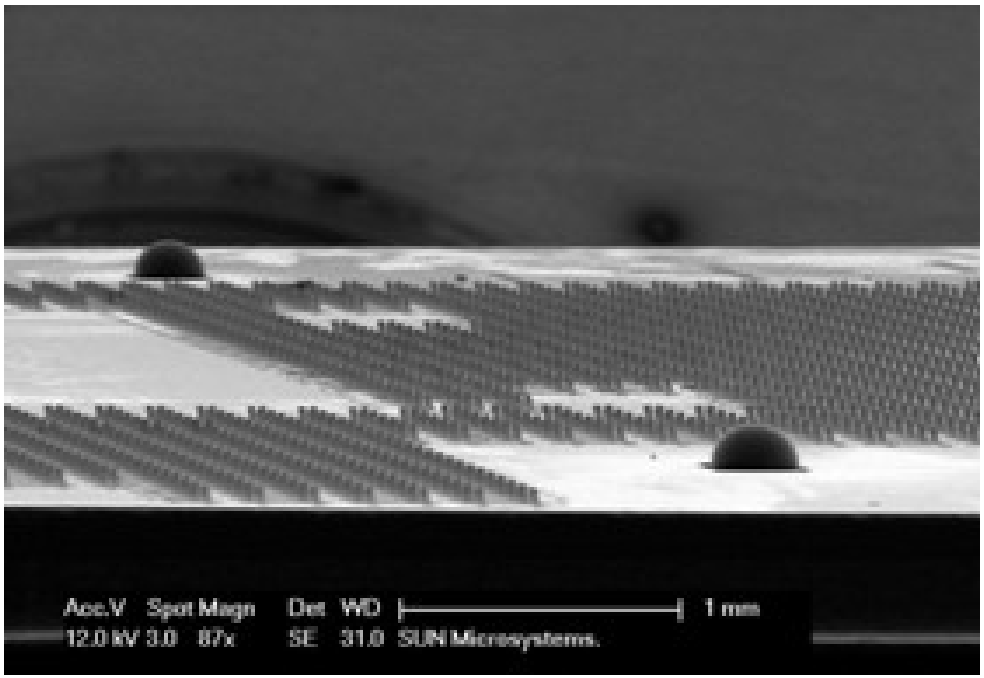
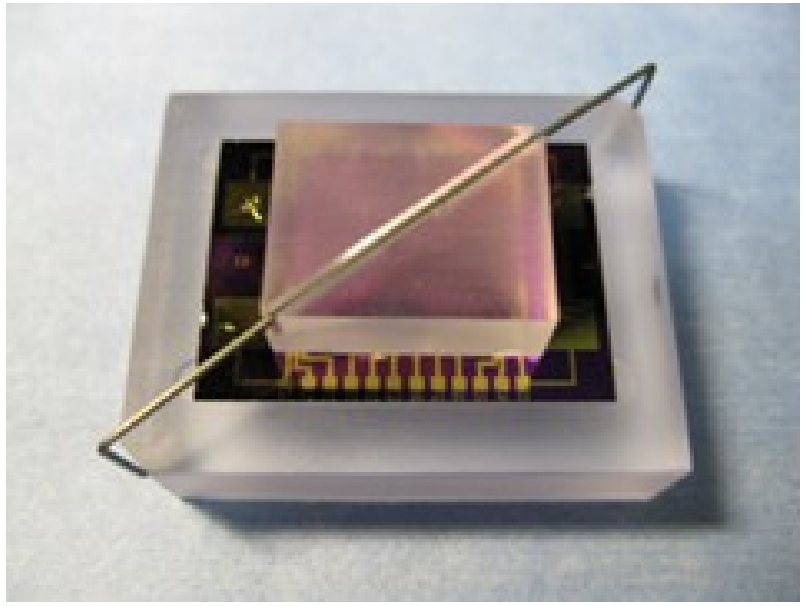
SUN Technology





I. Shubin et al., ECTC 2009

Package to test rematability



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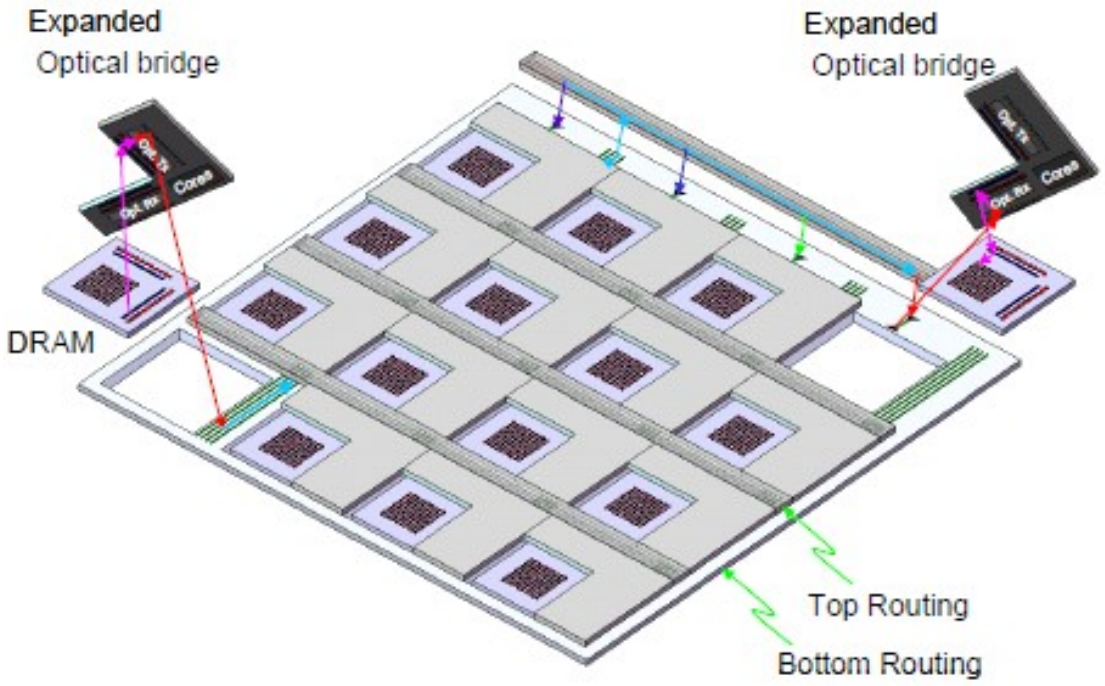
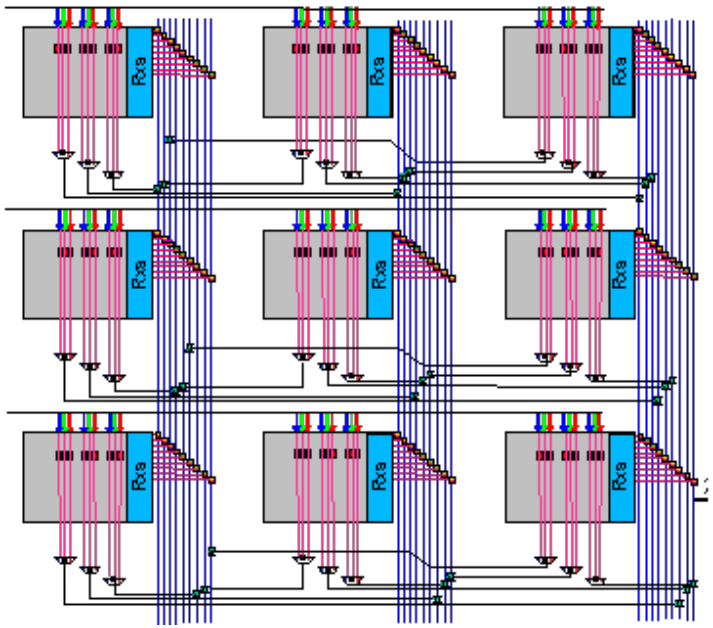
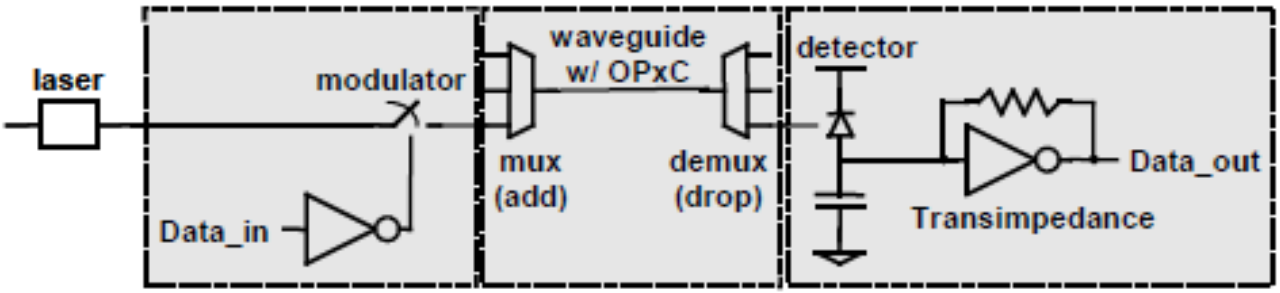
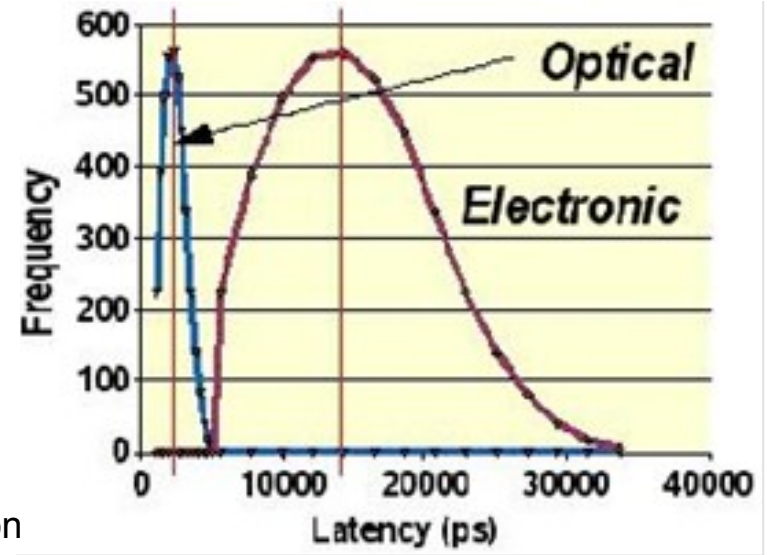
Macrochip with SiPhotonics









Source: A. Krishnamoorthy et al., "Computing microsystems based on silicon photonic interconnects," Proceedings of the IEEE, July 2009.

X.Xheng et al., Group IV, 2008

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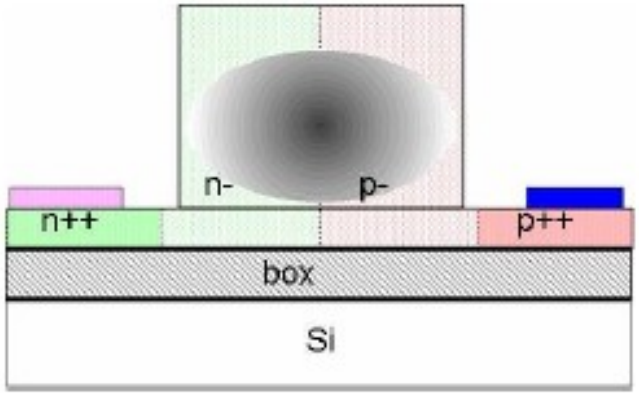
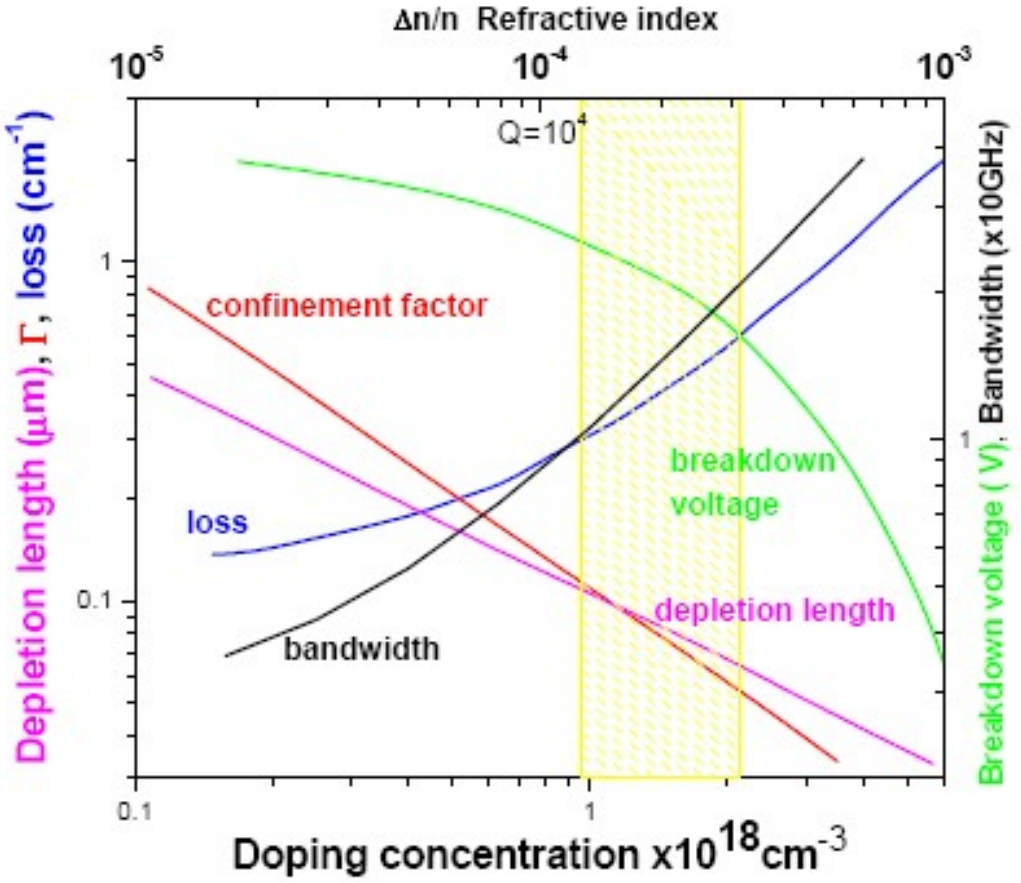
Device considerations modulators

Design space for fast ring modulators





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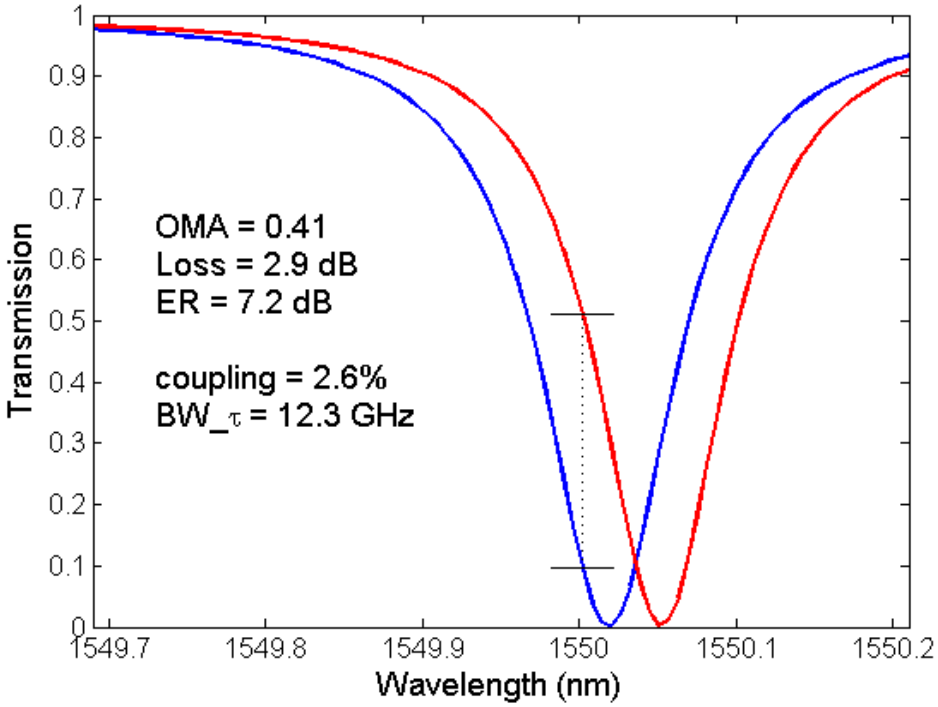
Ring Modulator Analysis

Expected performance with 2V swing in reverse bias



Modulation> 7 dB
Insertion loss <3dB

Use 30 um ring diameter, 60% modulation length.

Doping density 1e18.

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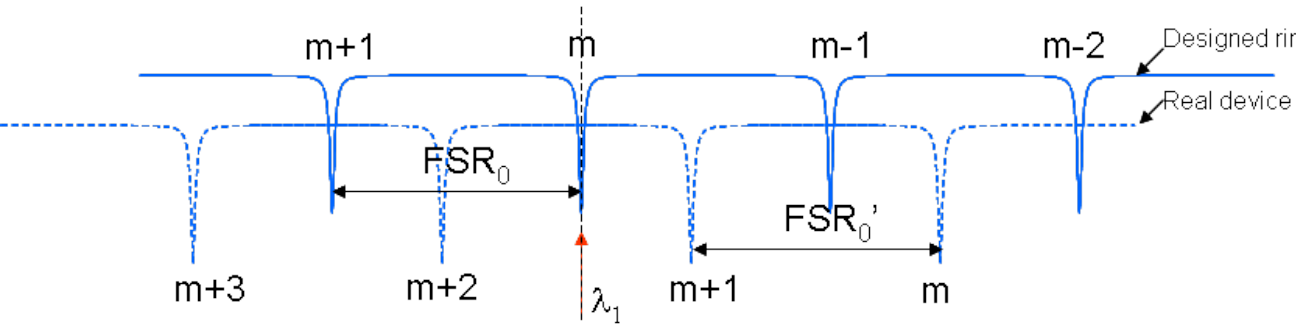
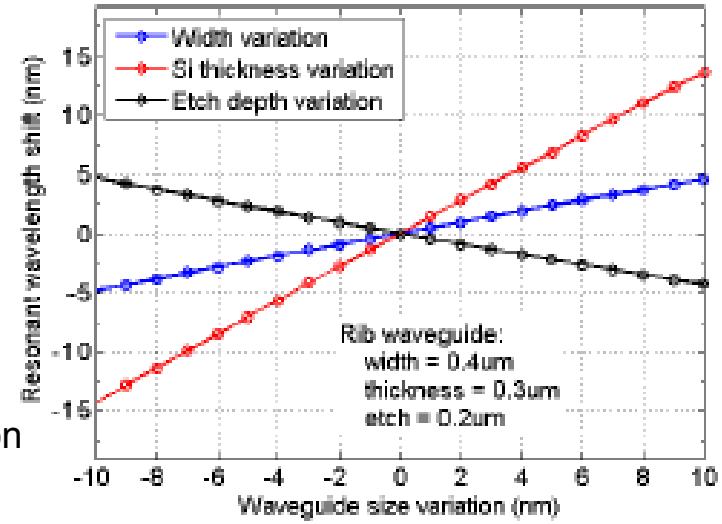
Tuning for WDM devices

- Energy per bit to communicate
- Lots of modulation progress:1/4 CV^2 down to < 100 fJ/bit
- Challenge to tune ring modulators onto ITU grid
- Tuning with forward bias degrades resonantor's Q
- Large thermal energy per bit penalty to tune
- Large error in resonance due to microfab variation





Source: A. Krishnamoorthy et al., "Computing microsystems based on silicon photonic interconnects," Proceedings of the IEEE, July 2009.

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Summary

- Break the single “reticle” limit for performance
- Integrate many chips as a logical large “macrochip”
  - Optically interconnected macrochip enabled by Si photonics
  - Key enabling technology OPxC demonstrated with promising performance and potential packaging solutions
- WDM point-to-point network for macrochip
  - Highly transparent, seamless network w low and uniform latency
  - High sustainable bisection bandwidth insensitive to message size
- New Optical devices
  - Lower energy per bit, smaller footprint
  - Stronger electro-optic effect
- Low Power Devices necessary
  - Roadmap to 300fJ/bit
  - Low power transmitter demonstrated

(X. Zheng et at., "Ultra-Low Power All CMOS Si Photonic Transmitter," OSA Frontiers in Optics, 2009
R. Ho et al., "Circuits for silicon photonics on a 'macrochip," IEEE ASSCC, in press, November 2009.)

Thank you!

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