Scaling and Energy Efficiency in Next Generation Core Networks and Switches

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Sunday Workshop: How much Energy Efficiency Can we Achieve in Next Generation Core Networks and Switches?

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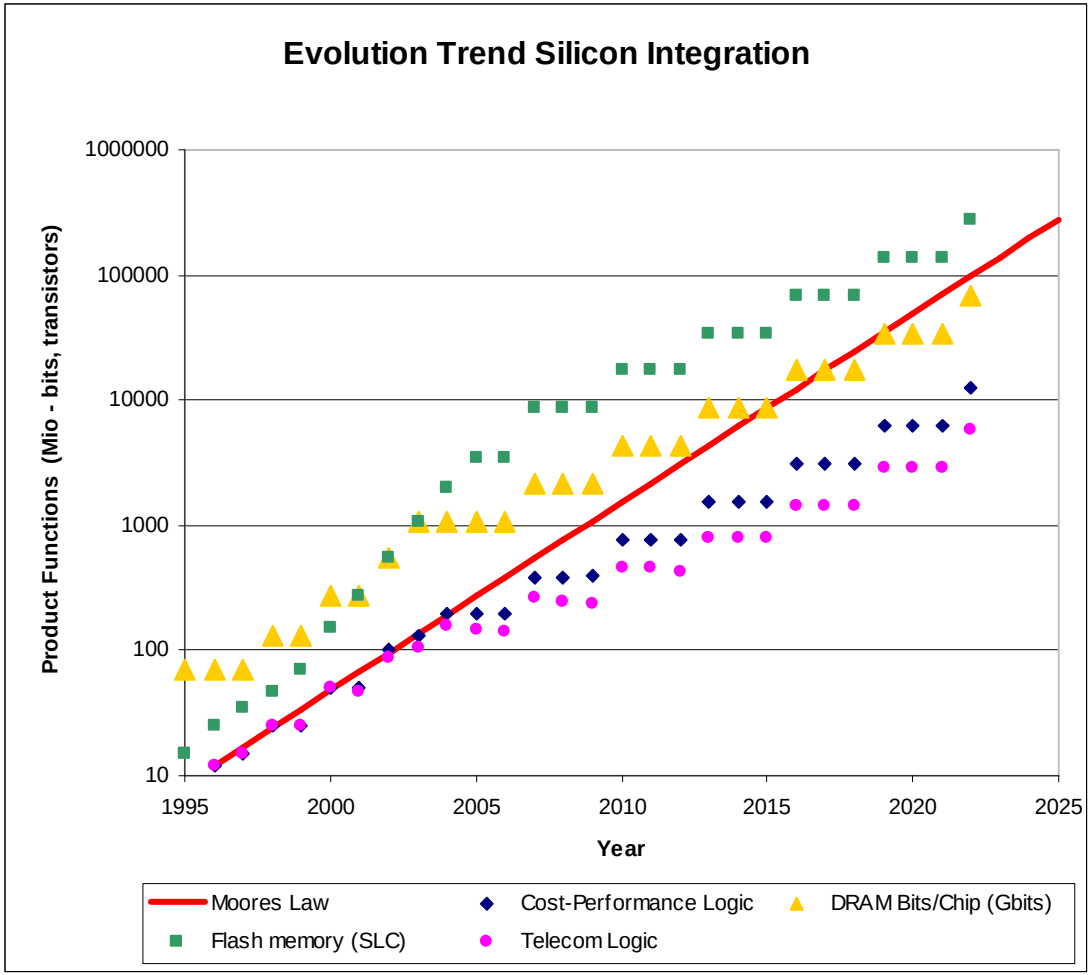
Some Interesting Questions on Power & Eco sustainability

- Will we be able to sustain traffic demand by only scaling today's network architectures as they are?
- Will Silicon / Optics technology evolution lower power-per-bit, along with enough capacity at lower cost-per-bit, to support traffic growth?
- What are the technology boundaries and how to overcome these?
- Is there a need to change our network paradigms due to power / scalability issues?

We'll try to answers with results from an internal study we've performed on Technology Evolution trends

CMOS Technology Density Trend for Telecom Equipment

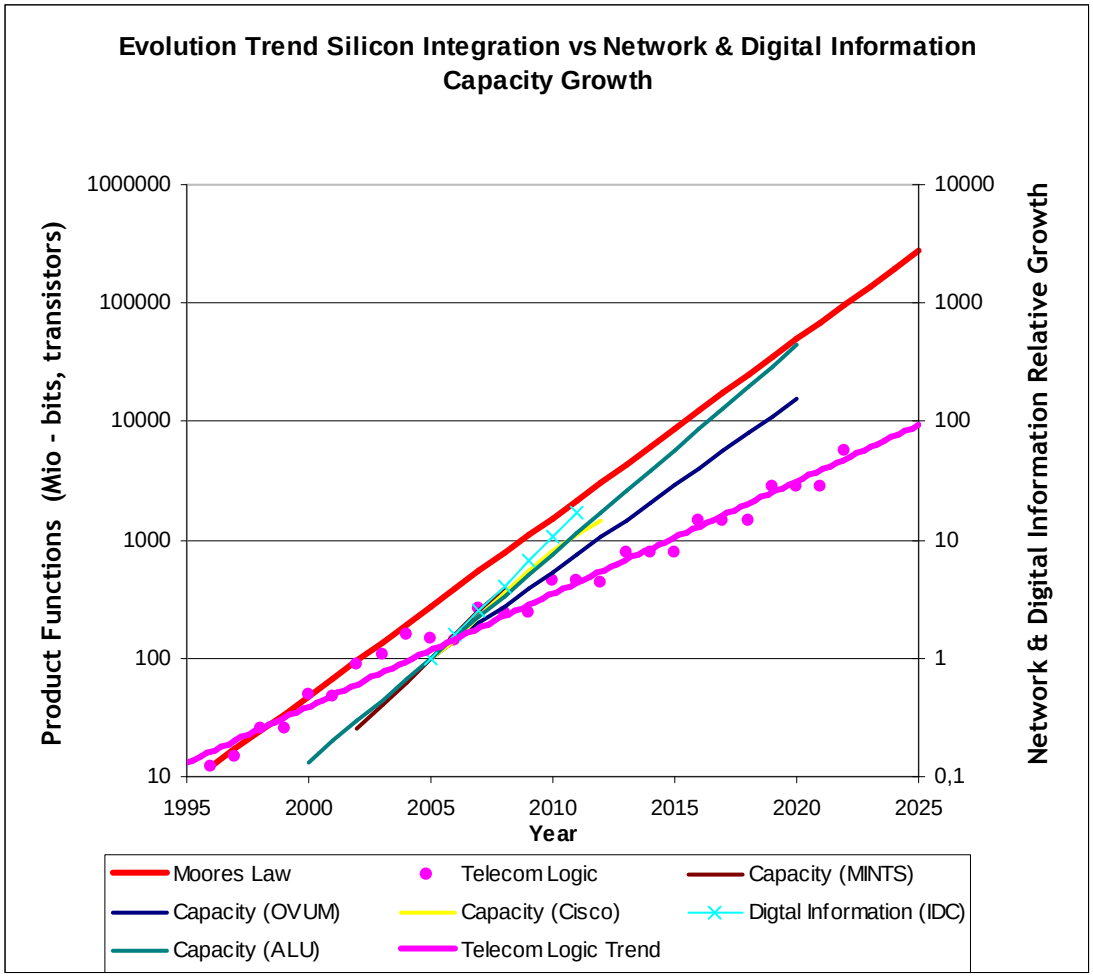


- High end CMOS logic devices in Telecom equipment face one of the most rigorous top power limitations due to shelf architecture, cooling and environmental boundaries
- Power per system volume (Watts per cubic meter) and power per device package are the main limiting factors

Sources: ITRS, ALU

System Power is the limiting factor for density improvements and not how many transistors can be placed on a die

CMOS Technology Density Trend for Telecom Equipment versus Capacity Growth

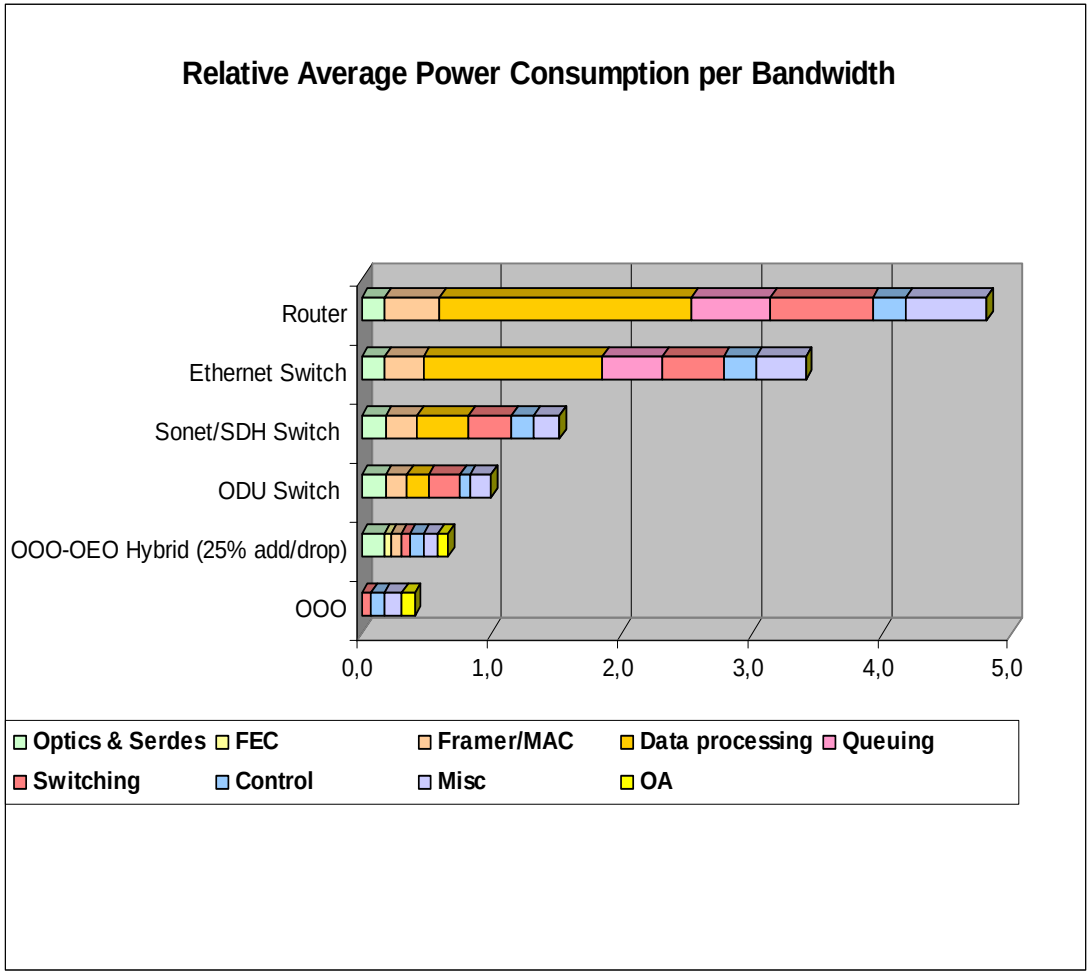


- Traffic Growth & Digital Information Growth is significant higher than CMOS Integration improvement in Telecom Logic
- Performance increase (clock rate) per logic element is saturating in CMOS starting already (40nm, 32nm, ...)
- We will very likely face a situation in which CMOS evolution will not be able to accommodate traffic growth
- Increasing amount of transistors per die doesn't help. The power per transistor would need to go down at the same rate to maintain at least a flat power profile per device to achieve Moores Law

Sources: MINTS, OVUM, Cisco, IDC, ITRS, ALU

Silicon Technology Evolution alone is not sufficient to address traffic growth

Power versus Networking Layer



- Strong dependency between layer and power per bandwidth
- Ratio is quite stable over technology evolution (2005-2020)
- Results in a significant difference of achievable capacity per rack which is roughly the inverse ratio of the power ratio. For example an ODU switch can achieve roughly 5 times the capacity of a router using same CMOS technology.

Source: ALU

Strong need to move traffic to lower layers as far as possible

Conclusions

- Silicon technology will make significant steps into higher integration but power dissipation is not reduced by the same amount the amount of transistors is being increased
- Power per system/shelf needs to be kept flat due to cooling capability limits
- The higher the layer a system is operating at the lower is the maximum achievable capacity per shelf
- If the traffic projections come true then silicon technology evolution itself will not be able to accommodate for such
- Too low dense shelves result in multi shelf interconnections which demands further capacity which is mainly an issue for systems operating at high layers
- There is a strong need to move capacity to lower layers to reduce power
- Intelligent hybrid transport networks which are able to keep the traffic as far as possible at the lowest layer are a potential path to overcome the issue
- Without keeping the power profile flat new cooling schemes (e.g. liquid cooling) and high power feeding schemes including all surrounding infrastructure need to be introduced (Can we effort and maintain such ?)

Thank You

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