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« Silicon ecosystems in Europe: the key to competitiveness »

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Agenda
- SCs: a true « Key Enabling Technology »
- Political Moves and societal needs
- Europe’s stand point in applications/systems
- CMOS technology challenges
- Equipment: Lithography R&D in Europe
- Silicon ecosystems in Europe
- The Grenoble-Crolles success story
- Conclusions

Electronics leverage competitiveness and added value

Source: Decision, 2009
Economic imbalances generate Market potential

Source: International Labour Office, Estin & Co, ST

Key Enabling Technologies (KETs)

- European Commission communication (30 September 2009):

The Conclusions of the Competitiveness Council of 20 May 2009 pointed out “that it is of particular importance to maximize strong R&D investments in high-tech industries in Europe. They provide the most important manufacturing sectors with indispensable technologies” and looked forward to the Commission’s initiative to develop a pro-active policy for cultivating high-tech industries”.

Based on current global research and market trends the following could be regarded as the most strategically relevant KETs, given their economic potential, contribution to solving societal challenges and knowledge intensity:

- Nanotechnology
- Photonics
- Advanced materials
- Biotechnology

New applications

New customers

'plus'

'more'

Active population (in thousands)

Monthly salaries (incl. charges)

0 500 000 1 000 000 1 500 000 2 000 000 2 500 000

0 10 20 30 40 50 60 70 80 90 100

0 50 100 150 200 250

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New opportunities for Electronics in Europe

- Tremendous applications of electronics in front of us: energy savings, healthcare technologies, digital identity
- Life will never be the same as before!

- Innovation still very active in the ‘old continent’. One issue: Transforming swiftly scientific firsts into market successes

- Electronics ideally positioned to enable a Sustainable World

- Perfect fit between components and systems manufacturers: Portfolio of technologies, Geographic proximity. Used to work together, a >400 M people market to experiment new standards

- All the building blocks are here.
- We need a strong European industrial policy

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Global challenges for Europe

- Low cost Areas competition
- R&D Costs explosion
- Technology and value chain Evolution
- Society Evolution

Europe still healthy in Electronics!

Worldwide Electronic equipment manufacturing
Split by Regions, 2008

- Europe: 22%
- Asia Pacific: 18%
- Americas: 15%
- Japan: 10%
- Others: 29%

in 2008 = 1,140 B€

Source: Decision, 2009

European Semiconductor Industry fueled by European Market Leadership

- European Leadership in key industry sectors: Automotive, Industrial, Medical, Power & Wireless Communication
- Electronic systems OEM rankings

Key challenges for Electronics in Europe

- Maintain innovation at the highest level (incremental & disruptive) with better university-industry transfers and R&D tax credits
- Maintain a solid manufacturing infrastructure whenever possible (despite the overall environment making too often delocalisation the easiest and cheapest solution)
- Leverage the advantage of the close coupling in Europe of demand / design / technology & innovation / manufacturing = build up and maintain solid « ecosystems »
- Exchange rates: $ vs. € ! Competitiveness risk
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**Lithography roadmap for Logic ICs**

- **2010**: 32/28 nm (1.35 NA Immersion)
- **2011**: 22/20 nm (1.35 NA Immersion, Double Patterning)
- **2012**: 10/7 nm
- **2013**: 5 nm
- **2014**: 3 nm
- **2015**: 2.5 nm

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**Cooperative R&D: Continuity, Coherence, from core Technology to System**
European R&D cooperation in lithography

**IMMERSION LITHOGRAPHY : LIQUID (MEDEA+) and LENS (ENIAC)**

  - Immersion lithography to produce 45nm feature with optical lithography.
  - First extension towards the 38nm node.

- **LENS** : Lithography Enhancement towards NanoScale (2009-2011)
  - Started in 2009. Effort = 158 Persons Years.
  - Two alternative approaches, both based on existing immersion scanners, for the patterning of 32nm and 22nm technology:
    - Double exposure
    - Pitch doubling

European cooperation in EUV litho

**EXEPT project within CATRENE programme**

**EXEPT : 1326 Persons Years (the largest CATRENE project)**

Previous complementary activities

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Advanced CMOS challenges

R&D and manufacturing costs are exploding!

The answers:
1. Alliances for R&D and production
2. Robust Technologies, first-time silicon success and fast ramp-up in volume
From R&D to Markets: Silicon Ecosystems in Europe

- Markets
- Academia
- Device Providers
- Equipment/System Providers

Source: I. Malier, Catrene Forum, Nov. 09

Industry Competitiveness: high again on the political agendas in Europe?

- Silicon Saxony in Germany,
- Point one in the Netherlands,
- Minatec-Minalogic in France,
- Catania cluster in Italy,
- Eindhoven/Leuven/Aachen triangle...

- Competitive clusters mixing science, education and high-tech industry
- All aiming at better efficiency through focusing and political visibility through impact on added value and jobs created

A scenario for SC manufacturing in 2012?

- NO. OF LOGIC IDMS WITH FABS

Changes in the European SC landscape

- A world wide ‘economic war’ for mastering the micro-nanoelectronics industry
- Transistors count: + 30% per year
- Transistor cost: -20% per year
- Heavy R&D and industrial investment
- 2 sites only in Europe for general purpose
- SC manufacturing on 300mm wafers: Grenoble-Crolles and Dresden
- Crolles has the ingredients for success:
  - IBM alliance
  - Cooperation with LETI-MINATEC
  - National and local support: ‘Nano2012’
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Microelectronics in Grenoble area
since the early ages

60’s-70’s 80’s 90’s 00’s

1st Startup
from LETI
1st French MOS Technology
LETI/EFCIS
Common Program with LETI
100 mm Wafers
CMOS and BICMOS

Thomson SC
With LETI+CNET + Philips sc
9 µm Technology
200 mm Wafers
MOS and BICMOS

SGS-Thomson
200 mm Wafers
0.5 µm Technology
SGS-Thomos and BICMOS

STMicroelectronics
300 mm Wafers
Submicron Technology
Grenoble-Crolles 2 Alliance
with NXP and FISL (2003-2007)
IBM (2008-)

Employment impact in Rhone-Alpes area

ST Crolles 4000
+ Direct 4000
+ Indirect 8000

Total Rhône-Alpes - 16,000 jobs
plus 9,000 in France

In addition, ST:
#1 employer in the area
#1 exporter in the area

Yearly expenses ~900 MC
incl > 500 MC in Rhone-Alpes
Yearly local tax >100 MC

The loop to deliver value to the customers

Customer

DESIGN
SPECIFICATIONS SYSTEM LEVEL

BACK END

Malaysia,
Philippines,
China

FINAL TEST
PACKAGING
WAFFERS TEST

SUBCONTRACTING

SILICON WAFERS
MANUFACTURING
CMOS 32-22 nm and derivative technologies

IBM Ecosystem

Basic CMOS technolo

STMicroelectronics – LETI Ecosystem

Above CMOS
- Additional functionalities (RF, imaging,...)

Integrated to CMOS
- Information design (embedded memories)

Below CMOS
- Performance relaxing (SOI with SOITEC)

Integration
- of innovative differentiated technologies

Production
- ST-Crolles

Plus foundries in accordance with volume and 2nd source needs

New applications, chip design
- ST-Grenoble

Advanced CMOS and Derivative Options offer Performance and added features

GPS WIFI
- BlueTooth
- FM radio

Base Band / Multimedia Processor

Energy Management

RF Transceiver

Integration of more features in handheld devices
- Battery voltage compatibility to allow easy add-on features

ST Crolles products and customers

Communications
- Computer Peripherals
- Digital Consumer
- Automotive

ST Crolles

Cleanroom C300
- 300 mm Wafers down to 22 nm
- actual 2 800 w/w
- future 4 500 w/w

Cleanroom C200
- 200 mm Wafers down to 120 nm
- 7200 w/w

Cumulated investment ~4 B$

5000 direct jobs on site
**Volume in 65/55nm**
- Wireless
- Consumer
- Automotive

**Mix change in 45/40 nm**
- Wireless
- Computer

- Setting tools for 32/28/22 nm
- High K Metal Gate
- Capacity ~ 2800 wafers per week in 2009,
  3600 w/w end 2010, up to 4500 w/w at full built-out

**Labor Cost**: High Productivity via Full Automation

**Direct Labor Productivity**: via Operator Tasks Elimination (eg lot dispatching by computers) and Integrated WIP Management (MES, AMHS)

**Labor Productivity and Flexibility**: via Computer Integrated Wafer Manufacturing

**Dimension of Scale**: via competitive Fab sizing

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**Teaming up talents**:
- 200mm and 300mm Manufacturing
- Advanced CMOS and Derivatives Technology development
- Advanced CAD and Design Solutions
- Labs for characterization, qualification and failure analysis
- Process to Design Interface and Coordination
- Process and Platform Qualification
- Equipment to Process capability

**Attracting partners**:
- IBM on derivative value-added processes
- ASML on immersion lithography and OCP
- MENTOR Graphics on CAD close to process
Partnerships in research and thesis

- EMLC 2010, G. Matheron

World wide Competitiveness Cluster
« Pôle de compétitivité mondial »

- EMLC 2010, G. Matheron

Microelectronics geographic focus

- EMLC 2010, G. Matheron

Summary

- Europe still awake and wealthy in Electronics
- Plenty of opportunities for successful applications of CMOS technologies
- In Europe, and particularly at Grenoble-Crolles, competitive clusters ensuring:
  - Top-class silicon process development via local and worldwide alliances
  - On-site platform expertise for complex system-on-chip development, with service-oriented manufacturing
  - Completed with close contacts with design teams

NO, designing and manufacturing advanced semiconductors in Europe is not an Utopia! It’s happening HERE and NOW!!