27th EUROPEAN SYMPOSIUM ON RELIABILITY OF ELECTRON DEVICES, FAILURE PHYSICS AND ANALYSIS

ESREF 2016 Halle, Germany

September 19 – September 22, 2016
Händel-Halle, Halle (Saale)
www.esref2016.org

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A Word From The General Chair

ESREF 2016, 27th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, takes place from September 19th to September 22, 2016. For the first time the conference is held in Halle (Saale), in the heart of the Central German Metropolitan Region, organized by VDE e.V. in close collaboration with Fraunhofer IMWS-CAM.

The ESREF symposium belongs to the most internationally recognized and globally leading scientific conferences within the field of electronics reliability and failure analysis. The conference covers different topics of reliability research for integrated circuits, for semiconductor devices, for packaged and assembled electronic systems, for defect physics and failure analysis methods, but addresses also further aspects of quality and robustness management during development and manufacturing. Looking back on a longstanding history, the ESREF conference is a well-established meeting place for the electronics reliability and failure analysis community, annually attracting the leading reliability specialist from academia and industry as well as equipment manufacturers for failure diagnostics and quality control.

For the field of electronics, there is no doubt that reliability and defect avoidance aspects have recently very much gained in practical significance and will be even more important in future. This trend is to some extent due to further IC shrink and the rapidly rising interest in new (e.g. wide bandgap) semiconductor materials as well as by the increasing material and design complexity of homogenously or heterogeneously integrated electronics systems. Today, however, one of the most important drivers for research in reliability and quality assurance comes from new automotive electronics applications. In view of the recent developments towards electrical powertrains and in particular, advanced driver assistance systems on the way to autonomous driving current electronic system developments have to balance a recently much accelerated innovation rate and very high demands on quality and reliability. The current debate around safety and reliability issues of automated cars gives evidence to this fact. Against this backdrop, ESREF 2016 has chosen to give a certain focus on reliability aspects in automotive applications, e.g. electronic control units or power electronics for e-mobility.

ESREF 2016 is subdivided into 8 topical tracks with 20 sessions accompanied by integrated tutorials and invited papers. The automotive electronics reliability aspects are, in addition to the regular papers, in particular reflected in the three key notes coming from leading industrial companies and in the presentations of the CAM workshop jointly organized with EUFANET that in 2016 was integrated into ESREF as a topical track. As in the past, also the European FIB User Group, EFUG, will contribute to the oral conference programme as well as a well-attended exhibition including flash presentations, a student's workshop and further industrial satellite user meetings.

As in the past years, the selected 134 papers have passed a two-step peer-review process that was performed by the Technical Programme Committee – a body of, altogether, 205 international specialists from both industry and academia. It is their commitment and diligence, which form the foundation for the internationally renowned quality of both the ESREF conference. We would thus like to express our gratitude and appreciation to all the members of those eight sub-committees for their expertise and their time made available for the selection of the contributions and for the critical reviewing and mentoring of the presented papers.

Allow me to welcome you all here in Handel's hometown Halle – make the most of your visit by joining us at the social events, organized specifically for you.

Matthias Petzold

Fraunhofer Institute for Microstructure of Materials and Systems (IWMS)

Center for Applied Microstructure Diagnostics (CAM)

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W. Kanert, Infineon AG (DE)

Session B — **Semiconductor Reliability and Failure Mechanisms**
M. Bafleur, LAAS (FR)
O. Aubel, GLOBALFOUNDRIES Inc. (DE)

Session C — **Reliability and Failure Mechanisms in Packaging and Assembly**
H. Fremont, IMS, University of Bordeaux (FR)
R. Rongen, NXP (NL)

Session D — **Progress in Failure Analysis Methods**
I. De Wolf, IMEC (BE)
W. Mack, Infineon AG (DE)

Session E — **Power Devices Reliability**
M. Ciappa, ETH Zurich (CH)
R. Bayerer, Infineon AG (DE)

Session F — **Reliability and Failure Mechanisms of Wide Bandgap Devices**
H-J. Würfl, FBH (DE)
S. Delage, III-V Lab, (FR)

Session G — **Reliability and Failure Mechanisms of Special Photonics and LED Devices**
G. Mura, University of Cagliari (IT)
H. Brunner, Osram Licht AG (DE)

Session H — **Reliability and Failure Mechanisms of MEMS and Sensor Systems**
M. Paulasto-Kröckel, Aalto University (FI)
U. Hansen, Robert Bosch GmbH (DE)

Session I — **Reliability of Automotive Electronics from a Systems Perspective (CAM-EUFANET Industry Workshop)**
S. Klengel, Fraunhofer IMWS-CAM (DE)
W. Wondrak, Daimler AG (DE)

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Jürgen Wilde
Bernhard Winkler
Eric Woirgard
Eckhard Wolfgang
Wolfgang Wondrak
Hei Wong
Xin Wu
Hans-Joachim Würfl
Thomas Zahner

Keynote Speeches

Monday, September 19, 14:00 – 14:40, Room: Einstein

22FDX and it's application in Energy Efficient Designs, Automotive and IoT – from foundry perspective

Manfred Horstmann,
Senior Director of Products and Integration GLOBALFOUNDRIES Inc (DE)

We were used to execute according to Moore's Law over the last decades. This road leads the semiconductor industry into highly scaled technologies: 14, 10 and 7 nanometer. However, economically a foundry should look towards the next hype building up, the Internet of Things. It is critical to offer the right technology to market at competitive cost with high performance, low power consumption and with build in connectivity. This automatically leads to Fully Depleted technologies with optional embedded RF capability as well as 28/22 nm patterning, with no need of extensive use of double patterning or new light sources for lithography. 28nm is known as the "sweet spot" in Foundry Industry for yield/performance AND cost. This node is in high volume production and will be the basis to add technology features like embedded RF, Flash, High Voltage (HV) or other value add solutions and is already predicted to have a long lifetime in our industry. In particular embedded RF and HV are key to communicate with the outside analog world in a power efficient and user-friendly way.

Technology-wise, 22FDX is reusing proven 28 nm processes, while adding new features. Devices on Fully Depleted SOI substrates can operate at voltages down to 0.4 V with outstanding performance. This technology meets the desire of IOT products to be ultra mobile and enables small form factors. In addition, the technology setup is much simpler, requires a lower number of mask layers and is ideal for a broad range of low power devices for automotive and IOT applications at lower cost. 22FDX makes "Faster, cooler, simpler" a reality and delivers FinFET performance at 28 nm costs.

Monday, September 19, 14:40 – 15:20, Room: Einstein

Automotive electronics roadmap and the wish list on electronics

Berthold Hellenthal,
Head Progressive SemiConductor Program AUDI AG (DE)

Piloted driving, always connected, artificial intelligence and digitization are necessary ingredients for the mobility of tomorrow. The automotive industry, its applications, use cases and customer expectations are changing at a progressively faster speed. Already more than 80 % of all automotive innovations are directly or indirectly enabled by semiconductors. How to resolve the conflicts between the latest semiconductor technologies and the stringent automotive quality and reliability requirements? How to solve the future automotive challenges towards autonomous driving and an always on 24/7 operation? How to ensure a mission critical robustness? The presentation will deduce a roadmap and a wish list on tomorrow's automotive electronics from the new challenges.

Wednesday, September 21, 11:10 – 11:50, Room: Einstein

Power and industry electronics – future perspectives for Europe

Sabine Herlitschka,
Chief Executive Officer Infineon Technologies Austria AG (AT)

The European Union has identified Micro- and Nanoelectronics as one of the key enabling technology of our times. Specific program lines were initiated in order to support research and development activities throughout the entire value chain. "Pilot Line" projects are intended to close the gap between research and commercial availability of technologies for customers. Infineon Technologies with its core competencies in power and industry electronics, together with its partners in academia and industry uses these programmes actively to enable new technologies contributing to providing solutions to societal challenges such as energy efficiency, mobility and security. The presentation will give an overview on respective strategies and activities contributing to a strong knowledge-based Europe in the global competition.

Exchange Papers

ISTFA 2015 – Outstanding Paper:

Monday, September 19, 16:20 – 16:40, Room: Einstein

Corrosion Mechanisms of Cu Bond Wires on AlSi Pads

Wantao Qin, George Chang, Harold Anderson, Tom Anderson and Denise Barrientos
ON Semiconductor (US)

Abstract: Cu wires were bonded to AlSi (1%) pads, subsequently encapsulated and subjected to uHAST (un-biased Highly Accelerated Stress Test, 130 °C and 85 % relative humidity). After the test, a pair of bonding interfaces associated with a failing contact resistance and a passing contact resistance were analyzed and compared, with transmission electron microscopy (TEM), electron diffraction, and energy dispersive spectroscopy (EDS). The data suggested the corrosion rates were higher for the more Cu-rich Cu-Al intermetallics (IMC). The corrosion was investigated with factors including electromotive force (EMF), self-passivation of Al, thickness and homogeneity of surface oxide on the IMC, ratio of the Cu-to-Al surface areas exposed to the electrolyte for an IMC taken into account. The preferential corrosion observed for the Cu-rich IMC is attributed to the high ratios of the surface areas of the cathode and anode that were exposed to the electrolyte, and degradation of the passivation of the surface oxide. With the understanding of the corrosion mechanisms, prohibiting the formation of Cu-rich IMCs is expected to be an approach to improve the corrosion resistance of the wire bonding, which is actually consistent with Pd-coating of the wire that is nowadays widely adopted in the industry.

IPFA 2016 – Best Paper For Reliability:

Monday, September 19, 16:00 – 16:20, Room: Einstein

Asymmetric Low Temperature Bonding Structure Using Ultra-Thin Buffer Layer Technique for 3D Integration

Hao-Wen Liang, Ting-Yang Yu, Yao-Jen Chang and Kuan-Neng Chen
National Chiao Tung University (TW)

Abstract: Wafer-level Sn/In-Cu bonding structure with Ni ultra-thin buffer layer is investigated to achieve a reduction in solder thickness, bonding temperature and duration. Furthermore, the asymmetric bonding structure is able to separate the manufacturing process of solder and electrical isolation layer. It is a promising approach for the application on hybrid bonding of three-dimensional integration.

IRPS 2016 - Best Paper:

Monday, September 19, 15:40 – 16:00, Room: Einstein

Quantitative Model for Post-program Instabilities in Filamentary RRAM

R. Degraeve, A. Fantini, G. Gorine, P. Roussel, S. Clima, M. Chen, B. Govoreanu, L. Goux, D. Linten, M. Jurczak, A. Thean*
*imec, *University of Pavia (IT)*

Abstract: This paper discusses and models the program instability observed in filamentary Hf-based RRAM devices in the context of the Hourglass model. It is demonstrated that two variability sources can be distinguished: (i) number variations of the amount of vacancies in the filament constriction and (ii) constriction shape variations. The shape variations are not stable in time and show a log(time)-dependent relaxation behavior after each programming pulse. This makes program/verify schemes, aiming at widening the resistive window, highly ineffective. We develop a quantitative, mathematical description of the instability using an auto-correlated step process of the shape parameters of the QPC conduction model.

Invited Talks

Tuesday, September 20, 09:30 – 10:10, Room: Einstein

Reliability Management – the central Enabler for Advanced Technologies in Automotive

Andreas Aal, Volkswagen AG (DE)

Abstract: Mobility is in a transition phase from individual human controlled to assisted and autonomous driving. Also, new roles add to car manufacturers being now forced to adapt to digital service providers as cars become the ultimate mobile office. Today, functional automotive requirements start to exceed on what's on the market accompanied with huge reliability assurance process gaps along the supply chain. Standards are out dated, research data unavailable and activities to change this strongly bound to market dynamics and mass volume requirements. This is why reliability engineering and management becomes a leading role in product design and business model formation. Transparency about technological gaps and how they are being handled determine market positions. To create industry awareness, we demonstrate two examples out of an OEM driven study on mechanical induced parametric deviations which relate to corresponding product verification/ validation issues that can end up in real, but which are mostly classified as no fault found (NFF) issues.

Wednesday, September 21, 08:30 – 09:10, Room: Planck

Device to circuit reliability correlations for Metal Gate / High-k transistors in scaled CMOS technologies

Andreas Kerber, GLOBALFOUNDRIES Inc. (US)

Abstract: Metal Gate / High-k stacks are in CMOS manufacturing since the 45nm technology node. To meet technology performance and yield targets gate stack reliability is constantly being challenged. Assessing the associated reliability risk for CMOS products relies on a solid understanding of device to circuit reliability correlations. In this paper we summarize our findings on the correlation between device reliability and circuit degradation and highlight areas for future work to focus on.

Tuesday, September 20, 08:30 – 09:10, Room: Fraunhofer

Laser Voltage Probing – its value and the race against scaling

Dr. Ulrike Ganesh, Qualcomm Technologies Inc. (US)

Abstract: After providing a brief introduction to Laser Voltage Probing (LVP), along with useful information and further reading suggestions, this paper provides a deep dive into current benefits and challenges of LVP applied to 16/14 nm FinFET technology and discusses the issues that arise from scaling of technology nodes according to the International Technology Roadmap for Semiconductors.

Tuesday, September 20, 09:30 – 10:10, Room: Planck

Reliability aspects of copper metallization and interconnect technology for power devices

Frank Hille et al, Infineon Technologies AG (DE)

Abstract: The introduction of thick copper metallization and topside interconnects as well as a superior die attach technology is improving the performance and reliability of IGBT power transistor technologies significantly. The much higher specific heat capacity and higher thermal conductivity increases the short circuit capability of IGBTs, which is especially important for inverters for drives applications. This opens the potential to further optimize the electrical performance of IGBTs for higher energy efficiency. The change in metallization requires the introduction of a reliable barrier against copper diffusion and copper silicide formation. This requires the development of an efficient test method and reliability assessment according to a robustness validation approach. In addition, the new metallization enables interconnects with copper bond wires, which yield, together with an improved die attach technology, a major improvement in the power cycling capability.

Thursday, September 22, 09:30 – 10:10, Room: Fraunhofer

GaN devices: millimeter wave applications challenges

Sylvain Delage, III-V Lab (FR)

Abstract: GaN-HEMT technology has been commercially available for several years and is a disruptive technology for high frequency RF power applications. GaN semiconductor offers wide band and high power capabilities thanks to its high saturation electron velocity, chemical stability and high breakdown voltage. GaN technology has been first developed and made available for base station applications for L-Band. Fierce competition does exist against well installed Si-LDMOS technology for saturated output power up to 1kW at frequencies below 4GHz. The landscape is more open for higher frequency bands as silicon devices have intrinsic physical limitations. Actually GaAs devices are the current existing solid-state competitor for high power microwave applications and occupy strong positions in various applications. GaN devices are allowing higher output powers, denser circuits and wider bandwidths. Products are coming in the market for Ka-Band applications. It is foreseen that circuits will be developed for up to 90GHz for applications such as E-Band data backhauling. Material and technological challenges will be presented with a particular focus on reliability aspects.

Wednesday, September 21, 09:50 – 10:30, Room: Fraunhofer

LED Degradation: From component to system

Benoit Hamon, Philips Lighting (NL)

Abstract: Human civilization revolves around artificial light. Since its earliest incarnation as firelight to its most recent as electric light, artificial light is at the core of our existence. It has freed us from the temporal and spatial constraints of daylight by allowing us to function equally well night and day, indoors and outdoors. It evolved from open fire, candles, carbon arc lamp, incandescent lamp, fluorescent lamp to what is now on our door step: solid state lighting (SSL). SSL refers to a type of lighting that uses semiconductor light-emitting diodes (LEDs), organic or polymer light-emitting diodes (OLED / PLED) as sources of illumination rather than electrical filaments, plasma (used in arc lamps such as fluorescent lamps), or gas. SSL applications are now at the doorstep of massive market entry into our offices and homes. This penetration is mainly due to the promise of an increased reliability with an energy saving opportunity: a low cost reliable solution. An SSL system is composed of a LED engine with a micro-electronics driver(s), integrated in a housing that also provides the optical, sensing and other functions. Knowledge of (system) reliability is crucial for not only the business success of the future SSL applications, but also solving many associated scientific challenges. In practice, a malfunction of the system might be induced by the failure and/or degradation of the subsystems/interfaces. This paper will address the items to ensure high reliability of SSL systems by describing LED degradation from a component and a system perspective.

Thursday, September 22, 08:30 – 09:10, Room: Planck

Application of high frequency scanning acoustic microscopy for the failure analysis and reliability assessment of MEMS sensors

Dr. Stefan Oberhoff et al, Robert Bosch GmbH (DE)

Abstract: We successfully applied high frequency scanning acoustic microscopy (SAM) as a tool for the analysis of MEMS sensors. Using state of the art transducers with frequencies up to 300 MHz, we evaluated the achievable resolution and performed case studies: we localized a contamination-induced delamination on the ASIC surface and studied failure modes after mechanical stability tests, showing that a combination of SAM and infrared microscopical evaluation provides information about the course of cracks on a micrometer length scale.

Tutorials

Tuesday, September 20, 08:30 – 09:30, Room: Einstein

Fast Wafer Level Reliability Monitoring as a tool to achieve automotive quality for a wafer process

Andreas Martin, Infineon Technologies AG (DE)

After any process reliability qualification some tool is needed which verifies the stability of the process throughout mass production. A continuous "fast Wafer Level Reliability" (fWLR) Monitoring is essential especially for stringent product reliability specifications of automotive, medical or space applications. "Zero Defect" programs are well known and manifest the implementation of fWLR Monitoring on product wafers. However, often used quarterly reliability re-qualification cannot achieve this quality goal and is inappropriate. Therefore, fWLR Monitoring must be employed, covering reliability topics such as dielectric quality, plasma induced damage, device degradation and metallisation reliability. Additionally, fWLR can support a fast assessment of reliability during process development, split investigations, process tool changes and process qualifications.

In this tutorial an overview will be given on dedicated fWLR test structures, highly accelerated stress measurements, data analysis and sampling. Further, the challenges and limitations of the fWLR methodology will be pointed out as well as benefits will be highlighted. The topics of an out of control action plan, the scrapping of wafers with fWLR and defect density monitoring will be addressed.

This tutorial is suited for engineers and scientists who start in the area of reliability monitoring. But also experts who already work on this topic will benefit since also advanced methods are described. Valuable details and literature citations can be picked up.

Thursday, September 22, 08:30 – 09:30, Room: Einstein

Creeping Corrosion of Copper on Printed Circuit Board Assemblies

Gert Vogel, Siemens AG (DE)

The mechanism of creeping corrosion of copper will be explained. Creeping corrosion of copper occurs when low concentration of hydrogen sulfide (< 1 ppm H2S) in combination with a relative humidity greater than 60% meets with bare copper on the bottom of a crack or pinhole. The forming copper sulfide is immobile but can be attacked by oxidizing gases and will diffuse as mobile copper oxide out of the pinhole. There it is retransformed by attacking hydrogen sulfide to copper sulfide.

Tuesday, September 20, 08:30 – 09:30, Room: Planck

10 Years Robustness Validation

Eckhard Wolfgang, ECPE e.V. (DE),
Werner Kanert, Infineon Technologies (DE)

It is a truism that reliability is related to applications requirements. Robustness Validation (RV) is a methodology to provide data demonstrating that a product is "fit for use". The ZVEI working group Robustness Validation was initiated 10 years ago. The concept has received increasing attention over this period, also beyond the automotive qualification procedures it initially originated from. The tutorial gives an overview of the basic concept of RV and experiences made in applying it to development and qualification. Two examples are discussed in detail: qualification of power modules and of thin-film DC-link capacitors. It also discusses difficulties in applying the concept.

Thursday, September 22, 08:30 – 09:30, Room: Fraunhofer

Field- and time-dependent degradation of GaN HEMTs

Enrico Zanoni, University of Padova (IT)

For both microwave and power switching applications, Gallium Nitride (GaN) devices offer significant advantages with respect to their silicon and GaAs counterparts: high carrier mobility and carrier density, outstanding breakdown fields and the possibility of operating at very high temperature are reflected into the possibility of designing high efficiency and high frequency power amplifiers and power conversion systems. According to the targeted application and market, these devices are epitaxially grown on Si or SiC substrates, the option of GaN bulk substrates being still limited and expensive. Material defectivity, related with lattice mismatch between GaN and substrate, and the extremely high electric field values may cause potential reliability issues which are under intense investigation worldwide. This tutorial will review most recent works concerning the study of defects-related parasitic effects and of physical failure mechanisms of GaN devices.

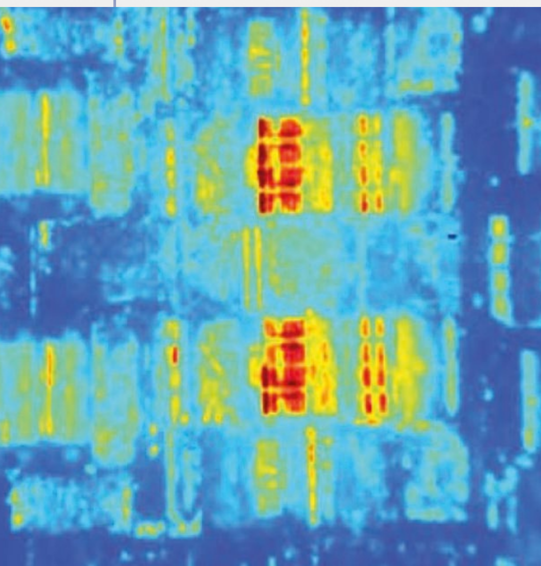
After a short overview on the reliability of GaN HEMTs for microwave applications, the analysis will focus on the characterization of deep level effects in enhancement- and depletion-mode power GaN devices for switching applications. Threshold voltage instabilities in MISHEMT structures and their dependence on dielectric properties will be reviewed. Subsequently, it will be shown how the extremely high electric field values may lead to time dependent breakdown phenomena, affecting not only dielectric layers but also the GaN semiconductor itself. Recent data on the reliability of p-gate devices will be presented. Finally, breakdown mechanisms limiting the maximum device operating voltages will be reviewed.

Wednesday, September 21, 08:30 – 09:30, Room: Einstein

Failure mechanisms and precautions in plug connectors and relays

Peter Jacob, EMPA Swiss Fed Labs for Materials Testing and Research (CH)

Plug connectors are one of the frequent failure causes when regarding at electronic systems. Since connectors had to keep pace with ongoing miniaturization on PCB level, current and voltage capabilities and specifications are frequently sportive or even overestimated. The tutorial focuses on the interfaces between connector and PCB as well as on connector-to cable and the connector contact itself, showing various failure mechanisms and precautions. Environmental conditions may also severely impact the connector reliability. The tutorial sensitizes the failure analyst to this underestimated topic and offers a deeper understanding and precaution measures against connector-related failures. Since many aspects considering plug connectors also apply for relays, the most important relay failure aspects are included in a small chapter of this tutorial.



Isolate electrical issues that affect yield, performance, reliability

Shrinking technologies, new materials, and more complex structures are driving defectivity. Failure-inducing defects have more places to hide—making characterization more difficult, and more critical, than ever.

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Workshops

CAM / EUFANET – Industry Workshop

The CAM / EUFANET- industry workshop (Wednesday, September 21, 2016, 09:30 – 18:10) will focus on the important topic of automotive electronics from the system perspective. Future challenges arising from autonomous driving and the increased market performance of electric cars will be highlighted. Presentations this year include talks from car OEMs and leading component and system suppliers.

Wednesday, September 21, 2016 – Room Einstein

09:30 – 10:50 **EUFANET/CAM-Workshop "Automotive Electronics Systems Reliability" (Part 1)**

Georgia Tech's automotive electronics ecosystem
Klaus-Jürgen Wolter, Georgia Tech Atlanta, 3D Systems Packaging Research Center (US)

77Ghz Automotive RADAR in eWLB package: from consumer to automotive packaging
Gerhard Haubner, Infineon Technologies AG (DE)

Reliability of automotive LED systems
Wolfgang Pohlmann, Hella KGaA Hueck & Co (DE)

14:50 – 16:30 **EUFANET/CAM-Workshop "Automotive Electronics Systems Reliability" (Part 2)**

Automotive Memory Trends and System Reliability Concepts
Reinhard Weigl, Micron Semiconductor GmbH (DE)

Powertrain electronics reliability
Mihai Nica, AVL Deutschland GmbH (DE)

Requirements for Reliability and new Solutions for Transmission Control Units
Michael Novak, Conti Temic microelectronic GmbH (DE)

Capability of Cu wire bonding for automotive electronics
Rene Rongen, NXP Semiconductors (NL)

16:50 – 18:30 **EUFANET/CAM-Workshop "Automotive Electronics Systems Reliability" (Part 3)**

Si IGBT reliability for HVs
Satoshi Yasuda, Toyota Motor Corporation (JP)

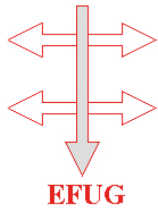
Power modules, qualification and test
Martin Rittner, Robert Bosch GmbH (DE)

Reliability of inverters and DC Link capacitors for e-mobility
Tim Langer, Volkswagen AG (DE)

Reliability of electronics for starter electronics
Amelie Thionville, Valeo (FR)

Batteries and their reliability with special respect to traction applications
Marcel Held, EMPA Swiss Fed Labs for Materials Testing and Research (CH)

EFUG-Workshop



Focused Ion Beam is one of the key preparation techniques for failure analysis at microelectronic and microsystem devices. There are multiple applications e.g. for defect screening and site specific preparation on integrated circuits and packaged devices, circuit edit, mask repair and many more. EFUG Workshop (Tuesday, September 20, 2016, 15:10-18:10) will provide a platform to exchange new information and practical experiences regarding the following Topics:

- New instruments : HIM, Plasma-FIB, Laser preparation Tools
- Efficient preparation workflows : automated TEM preparation, Plasma-FIB, Laser milling, Atom probe sample preparation
- Circuit edit : application procedures, new gas chemistries
- Nanoprobing
- Process monitoring for wafer manufacturing, in-line FIB and wafer return
- Failure analysis case studies : Si devices, wide bandgap, solar cells

Tuesday, September 20, 2016 – Room Fraunhofer

15:10 – 16:50 **EFUG Workshop (Part 1)**

Ga contamination in silicon by focused ion beam milling: Atom Probe Tomography and simulation with dynamic model
Jin Huang, TU Dresden (DE)

Micro mechanical robustness tests of 28nm BEOL layer stack
Eckhard Langer, GLOBALFOUNDRIES Inc. (DE)

Laser based sample preparation for advanced packaging applications
Thomas Höche, Fraunhofer IMWS-CAM (DE)

Planar FIB Milling of Copper by using the Novel Rocking Stage Technology
Sharang Sharang, TESCAN ORSAY HOLDING a.s. (CZ)

Fast, Reliable, Intuitive TEM Sample Preparation using a Load-Lockable Platform Combined with Smart Control Software
Stephan Kleindiek, Kleindiek Nanotechnik GmbH (DE)

16:50 – 17:10 **Coffee Break sponsored by**

17:10 – 18:10 **EFUG Workshop (Part 2)**

Imaging and Analysis Solutions for 3D Devices
Ingo Schulmeyer, Carl Zeiss Microscopy (DE)

Innovative TEM sample Preparation on Helios G4 platform
David Donnet, FEI Company (NL)

FIB and P-FIB assisted sample preparation for in-situ TEM characterization
Remy Berthier, CEA-LETI (FR)

Exhibitor Flash Presentations

We are offering all exhibitors the opportunity to have a flash presentation (10 min, without journal publication) on their focus topics during the conference.

Tuesday, September 20, 2016 – Room Fraunhofer

09:50 – 10:50 **Session 5 – Exhibitor Workshop: Defect Localization and Nanoprobing**

3D LIT calibration tool development
Thijs Kempers, MASER Engineering

Improvements on localisation techniques for high power devices
Mr. Minh Vo, Hamamatsu Photonics Deutschland GmbH

New phase Laser Voltage Imaging technique
Antoine Reverdy, Sector Technologies

Micromanipulators in Reliability Testing Environments:
Fault Localization, Nanoprobing, and TEM Sample Preparation
Andrew Jonathan Smith, Kleindiek Nanotechnik

Versatile probers for micro and nanoprobing
Karl Boche, Imina Technologies SA

EBIC and EBAC/RCI techniques
Dr. G Moldovan, point electronic GmbH

Tuesday, September 20, 2016 – Room Einstein

11:50 – 12:50 **Session 7 – Exhibitor Workshop: Sample Preparation**

Sample Preparation with the X-Prep
Chris Richardson, Allied High Tech Products

Laser Decap: the sample prep Swiss Army Tool
Yvan Pfeffer, Sector Technologies

SELA Sample Preparation Tools
Vladimir Zheleznyak, John P. Kummer GmbH

Curtaining-Free Top-Down TEM Lamella Preparation from a Cutting Edge Integrated Circuit
Tom Jaepel, Tescan / EO Elektronen-Optik-Service GmbH

Helios G4: Enabling breakthrough failure analysis for 7 nm design nodes
David Donnet, FEI Company

Preliminary Idea for Preparing 1000's of TSV's
Roland Ries, Gatan Inc.

Tuesday, September 20, 2016 – Room Planck

15:50 – 16:50 **Session 10 – Exhibitor Workshop: Failure Analysis**

Introduction of MA-tek total solution FA
Dr. Shih-Hsin Chang, Materials Analysis Technology Inc.

Failure Analysis and Failure Prevention on Ceramic Capacitors
Jürgen Gruber, RoodMicrotec GmbH

New technology approaches in scanning acoustic microscopy for advanced failure analysis
Dr. Peter Czurratis, PVA TePla Analytical Systems GmbH

Multiple Pass/Fail Detection Scheme
Romain Stomp, Zurich Instruments AG

Below 10nm technology analysis solution
Ching Yu Tai, MESOSCOPE Technology Co., Ltd.

High Resolution Cathodoluminescence for Defect Inspection and Failure Analysis
David Gachet, Attolight

Wednesday, September 21, 2016 – Room Planck

15:30 – 16:30 **Session 17 – Exhibitor Workshop: Reliability Testing and Failure Analysis**

Reliability Testing
David Sulyok, Mentor Graphics

Fault Isolation at 5um Resolution using Electro-Optical TDR with 6ps Rise Time
Atsushi Konno, Advantest Corporation

Use of Lock-in Thermography and Magnetic Current Imaging as complemetary techniques for localization of shorts in GaN transistors
Fulvio Infante, Intraspec Technologies

TBC
TBC, Digit Concept

Solutions for semiconductor failure analysis with SEM
Simon Burgess, Oxford Instruments

TBC
NN, NN

Student Research Speed Dating

Following the successful introduction in the last year's conference in Toulouse, a "speed dating" event for students based on 6 – 8 minutes pitch presentation on any topic strongly related to quality and reliability of electronics will be organized on **Wednesday, September 21, from 08:30 to 10:00, in Room Fraunhofer** to foster the exchange between the academic world and the ESREF community of international experts.

For a detailed outline of the talks, please refer to the ESREF App or see the supplementary sheet in this brochure.

Panel Discussion

"Reliability – getting the key factor for electronics in Europe today?"

Wednesday, September 21, from 11:50 to 13:50. in Room Fraunhofer

For the field of electronics, there is no doubt that reliability and defect avoidance aspects have recently very much gained in practical significance, and will be even more important in future. This trend is only to some extent due to further IC shrinking with only four competitors left for the race towards the 7 nm technology node. In contrast, the major part of the European semiconductor industry is working on topics like smart systems and heterogeneous systems integration, on application of wide bandgap materials, and on providing superior components for market segments like automotive, industry, energy and power, and the IoT.

Without any doubt, one of the most important drivers for research in reliability and quality assurance comes from new automotive electronics applications. In view of the recent developments towards electrical powertrains and in particular, advanced driver assistance systems on the way to autonomous driving, current electronic system developments have to balance a recently highly accelerated innovation rate on the one hand, and very high demands on quality and reliability on the other. The current debate around safety and reliability issues of automated cars gives evidence to this fact. This will have significant consequences for future research in electronics reliability and the required ecosystem.

Will a high reliability, superior quality and proven robustness continue to be a strength and asset of the European industry? Are quality, reliability and robustness factors we need to pay even more attention to, and what do we have to do to prepare for the developments and demands coming up in the future? Within this context, the panel involving experts from car and electronics industry, from academia and from the ECSEL joint undertaking will discuss topics like:

- the asset of superior reliability and robustness for European electronics
- resulting future demands on supply chain and ecosystem
- the related demands on scientific research and developments
- needs in industry-academy cooperation
- future governmental/European strategies for research and funding
- consequences for university education.

Panelists:

Berthold Hellenthal, AUDI AG (DE)

Sabine Herlitschka, Infineon Technologies Austria AG (AT)

Mervi Paulasto-Kröckel, Aalto University (FIN)

Yves Gigase, ECSEL Joint Undertaking

Klaus-Juergen Wolter, Georgia Tech Atlanta, 3D Systems Packaging Research Center (US)

Special Sessions in the framework programme

Workshop: “Extend analysis capabilities with Omniprobe solutions”

Fraunhofer IMWS-CAM and Oxford Instruments will present and discuss recent developments in failure analysis and characterization including TEM sample preparation, nanowire analysis and EBIC/EBAC analysis. A range of investigation cases will be discussed with the inputs of experts in both domains. The event will end with a hands-on analysis at Fraunhofer's lab.

The workshop will take place on Thursday, September 22, 2016 at Fraunhofer CAM, Heideallee 19, Halle.

Schedule:

15:45 – 16:30	Pickup and transfer from ESREF convention center to Fraunhofer
16:30 – 18:00	Presentations
18:00 – 18:40	Live demo: Backside sample preparation using the OmniProbe 400
18:40 – 20:00	Dinner and socializing

Presentations :

Welcoming remarks, *Frank Altmann, Fraunhofer IMWS-CAM (DE)*

Omniprobe Solutions, *Cheryl Hartfield, Oxford Instruments (UK)*

EBIC and EBAC applications for IC failure analysis, *Frank Altmann, Fraunhofer IMWS-CAM (DE)*

Registration:

Participation is free of charge, but participants need to register. Please see registration desk for details.

Workshop: “Failure Analysis with Nanoprobing, EBIC and EBAC”

The workshop brings together Fraunhofer IMWS-CAM, Imina Technologies SA and Point Electronic GmbH to present and discuss recent developments in EBIC/EBAC characterization in combination with Nanoprobing. A range of investigation cases will be discussed with the inputs of experts in both domains. The event will end with a hands-on analysis at Fraunhofer's lab.

The workshop will take place on Friday, September 23, 2016 at Fraunhofer CAM, Heideallee 19, Halle.

Schedule:

09.00 – 12.00	Presentations
12.00 – 13.00	Lunch
13.00 – 15.00	Tool Demos

Presentations:

Microprobing to Nanoprobing workflow in FA using versatile probing platforms
Guillaume Boetsch, Imina Technologies SA (CH)

Quantitative EBIC and EBAC/RCI techniques
Dr. Grigore Moldovan, point electronic GmbH (DE)

Applications of nano-probing and SEM based current imaging for IC failure analysis
Jörg Jatzkowski, Fraunhofer IMWS-CAM (DE)

Application of nanoprobing techniques to support 28nm foundry production
Eric Paul, Globalfoundries Inc. (DE)

Registration:

Participation is free of charge, but participants need to register. Please see registration desk for details.

Special Sessions in the framework programme

Fraunhofer Lab Tour

Come and join us on a tour of the Fraunhofer labs here in Halle. The tours will give you an insight into our work and our facilities.

The tours will take place on Thursday, September 22, 2016, 16:30, at Fraunhofer CAM, Heideallee 19, Halle.

Participation is free of charge, but participants need to register. Please see registration desk for details.

1. Stop: Failure Diagnostics at Integrated Circuits

Si-based integrated circuits are used in almost all electronic equipment today. Securing the reliable functionality is a key especially for automotive electronics, safety and medical applications. Fraunhofer IMWS-CAM supports manufacturers by advanced process characterization and failure analysis introducing innovative technologies, improving process steps, optimizing manufacturing yield as well as securing reliable field use of the devices. We help customers understand root causes for malfunctions in the context of electrical, thermal, mechanical or moisture treatment.

Presented research fields:

- Nano-probing and electrical characterization of IC structures
- SEM based defect localization by EBAC, EBIC techniques
- FIB/ SEM screening for nm defects
- Physical failure analysis by TEM

2. Stop: Micromechanical Testing for MEMS

We experimentally investigate mechanical properties of MEMS devices and materials using a wide variety of methods ranging from optical and mechanical micro deformation analysis and customized small-scale strength testing, residual stress analyses and nano-indentation up to standardized material testing and thermos-physical characterization of MEMS packaging materials. In addition, non-destructive microstructure and electrical device characterization, functional parameter analysis, reliability testing and high-resolution failure analysis for MEMS sensors and actuators are applied to support securing optimum manufacturing quality and long-term operational behavior.

Presented research fields:

- Si MEMS customized mechanical testing regarding deformation, strength and life time properties
- Characterization of wafer bonding technologies
- Microstructure, fractography and high-resolution failure analysis of MEMS devices

3. Stop: FA techniques for 3D Packaging and Systems Integration

Within semiconductor packaging and system integration, semiconductor chips are electrically interconnected to their environment, encapsulated for protection and assembled onto substrates forming either electronic components, modules, board assemblies or even complex 3D integrated micro- and subsystems. The design, process steps and materials used in packaging significantly affect the reliability properties of any semiconductor component. Fraunhofer CAM develops advanced techniques of physical failure analysis and material diagnostics ranging from non-destructive testing, high-precision and efficient site specific preparation to cutting edge electron microscopy, surface and trace analysis, optical and IR spectroscopy as well as mechanical and thermos-physical material characterization.

Presented research fields:

- High resolution delamination and crack detection by GHz Scanning Acoustic Microscopy
- Lock-In-Thermography for 3D localization of resistive defects
- new patented laser-micromachining tool and combined ion beam milling techniques

4. Stop: Characterization of Power Electronic Components

Power electronic devices and modules are gaining importance as they significantly determine the efficiency of generation, conversion, allocation and utilization of electrical energy within various applications ranging from mobile phones to hybrid cars and wind power parks. Fraunhofer IMWS-CAM provides customized mechanical testing, life time prediction and failure analysis for power devices developed for operating in standard and harsh environments. In addition to Si-based systems, we analyze the behavior and performance characteristics of novel SiC and GaN based devices including related dielectrics, metallization layers and contact systems. Particular attention is paid to a fundamental understanding of interface material properties and mechanisms relevant for new interconnection and packaging approaches. Current activities cover the characterization of heavy wire bonding materials, Ag-sintering, diffusion soldering, new substrates and housing materials.

Presented research fields:

- Microstructure and failure analysis of power semiconductors on wafer and chip level
- Characterization of encapsulation and housing materials
- Characterization of interconnection materials like heavy wire bonding contacts/materials (e. g. Al, Cu, Al / Cu clad wires/ribbons)
- Material characterization of high temperature-stable metallization and conducting systems
- Development of tools and methods for failure diagnostics and quality assessment specifically adapted to power electronics

Innovation in Failure Analysis and Material Diagnostics of Electronics Components

CAM / EUFANET INTERNATIONAL INDUSTRY WORKSHOP AND TECHNOLOGY EXHIBITION

APRIL 26th AND 27th, 2017
HALLE (SAALE) | GERMANY

See www.cam.fraunhofer.de for details

Time	Room: Planck	Room: Einstein	Room: Fraunhofer
Monday, 19th September 2016			
11:00 – 13:00	**Registration**		
13:30	Opening Session with Keynotes 1+2		
15:20	Coffee Break		
15:40	Opening Session - Exchange Papers		
16:40	Exhibition Opening / Get-together / Drinks Reception		
Tuesday, 20th September 2016			
08:30	**Session 3B:** Power Devices Reliability: Tutorial	**Session 3A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Tutorial	**Session 3C:** Progress in Failure Analysis Methods: Laser probing techniques
09:30 / 09:50	**Session 4B:** Power Devices Reliability: Metallization and Interconnects	**Session 4A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories – Part 1	**Session 5:** Exhibitor Workshop: Defect Localization and Nanoprobing
10:50	**Coffee Break / Exhibition**		
11:10	**Session 6B:** Power Devices Reliability: SiC Devices	**Session 6A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories – Part 1 (continued)	**Session 6C:** Progress in Failure Analysis Methods: Nanoscale failure analysis
11:50		**Session 7:** Exhibitor Workshop: Sample Preparation	
12:50	**Session 8:** Poster Session for Tracks B / D / E /G		
13:50	**Lunch Break / Exhibition**		
15:10	**Session 9B:** Power Devices Reliability: Passives	**Session 9A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories – Part 2	**Session 9C:** EFUG - Workshop (Part 1)
15:50	**Session 10:** Exhibitor Workshop: Failure Analysis		
16:50	**Coffee Break / Exhibition**		
17:10	**Session 11B:** Power Devices Reliability: Testing Methods	**Session 11A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Space and Radiation	**Session 11C:** EFUG - Workshop (Part 2)
18:30	**Drinks Reception – Castle Moritzburg**		
Wednesday, 21st September 2016			
08:30	**Session 12A:** Semiconductor Reliability & Failure Mechanisms: FD-SOI and RRAM	**Session 12B:** Failure mechanisms and precautions in plug connectors and relays: Tutorial	**Session 12C:** Students Workshop
09:30 / 09:50		**Session 13:** EUFANET/CAM-Workshop "Automotive Electronics Systems Reliability" (Part 1)	**Session 14:** Reliability and Failure Mechanisms of special photonics and LED Devices: LED systems
10:50	**Coffee Break / Exhibition**		
11:10	**Session 15:** Panel Discussion + Keynote 3		
13:50	**Lunch Break / Exhibition**		
14:50	**Session 16A:** Semiconductor Reliability & Failure Mechanisms: BTI	**Session 16B:** EUFANET/CAM-Workshop "Automotive Electronics Systems Reliability" (Part 2)	**Session 16C:** Reliability and Failure Mechanisms of special photonics and LED Devices: LED; laser diodes and VCSELs
15:30	**Session 17:** Exhibitor Workshop: Reliability Testing and Failure Analysis		
16:30	**Coffee Break / Exhibition**		
16:50	**Session 18A:** Semiconductor Reliability & Failure Mechanisms: Miscellaneous	**Session 18B:** EUFANET/CAM-Workshop "Automotive Electronics Systems Reliability" (Part 3)	**Session 18C:** Progress in Failure Analysis Methods: Novel non-destructive testing
19:00	Concert / Ulrichskirche		
20:00	Gala Dinner / Hotel Rotes Ross		
Thursday, 22nd September 2016			
08:30	**Session 19A:** Reliability & Failure Mechanisms of MEMS and sensors	**Session 19B:** Reliability & Failure Mechanisms in Packages and Assembly: Tutorial	**Session 19C:** Reliability & Failure Mechanisms of Wide Bandgap Devices: Tutorial
09:30		**Session 20A:** Reliability & Failure Mechanisms in Packages and Assembly: Moisture and corrosion related studies	**Session 20B:** Reliability & Failure Mechanisms of Wide Bandgap Devices: Microwave devices
10:50	**Coffee Break / Exhibition**		
11:10	**Session 21A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Miscellaneous	**Session 21B:** Reliability & Failure Mechanisms in Packages and Assembly: Reliability and Modelling	**Session 21C:** Reliability & Failure Mechanisms of Wide Bandgap Devices: GaN power devices and deep level transient spectroscopy
12:50	**Session 22:** Poster Session for Tracks A / C / F / H and Exhibition		
13:50	**Lunch Break / Exhibition**		
15:10	**Closing Ceremony**		

Poster Presentation

The Poster Presentation is one more instrument to contribute to a satisfying networking opportunity at the conference. It adds the chance of intense exchange and discussion.

Poster presentations will take place at the exhibition area on the first floor and are scheduled as follows:

Tuesday, September 20, 2016 at 12:50

Poster Session for Tracks:

- Semiconductor Reliability & Failure Mechanisms
- Progress in Failure Analysis Methods
- Power Devices Reliability
- Reliability & Failure Mechanisms of Special Devices (Photonics, anorganic and organic LED)

Thursday, September 22, 2016 at 12:50

Poster Session for Tracks:

- Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems
- Reliability & Failure Mechanisms in Packages and Assembly
- Reliability & Failure Mechanisms of Wide Bandgap Devices
- Reliability & Failure Mechanisms of MEMS and sensors

Author's Gallery

The Author's Gallery is an additional communication and exchange offer for oral presenters. In the break after the respective session, the presentation slides will be pinned to a movable wall like a poster in the exhibition/catering area. The organizers will take care of printing the slides and putting them up. The oral presenters should attend to their wall after the session is ending. Those participants of the audience who want to discuss topics of the presentations in more detail than the discussion during the session allows, may approach the presenter in the break for more intense exchange.

The authors corner is located at the exhibition area on the first floor.

Room: Einstein

Session 1: Opening Session with Keynotes 1+2

13:30	**Welcome to ESREF 2016** *SPEAKER: Matthias Petzold, Fraunhofer IMWS-CAM (DE)*
14:00	**22FDX and it's application in Energy Efficient Designs, Automotive and IoT - from foundry perspective** *SPEAKER: Manfred Horstmann, Globalfoundries (DE)*
14:40	**Automotive Electronics Roadmap and the Wish List on Electronics** *SPEAKER: Berthold Hellenthal, AUDI AG (DE)*

Room: Einstein

Session 2: Opening Session – Exchange Papers

15:40	**Quantitative model for post-program instabilities in filamentary RRAM** *SPEAKER: Robin Degraeve, IMEC (BE)*
16:00	**Asymmetric Low Temperature Bonding Structure Using Ultra-Thin Buffer Layer Technique for 3D Integration** *SPEAKER: Hao-Wen Liang, National Chiao Tung University (TW)*
16:20	**Corrosion Mechanisms of Cu Bond Wires on AlSi Pads** *SPEAKER: George Chang, ON Semiconductor (US)*

Room: Foyer

Exhibition Opening / Get-together / Drinks Reception

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Laser Decapsulation

Chemical Decapsulation

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Micro Cleaving | Adaptive Ion Milling | Dry Sawing

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Advanced Surface & Sample Preparation

Time	Room: Planck	Room: Einstein	Room: Fraunhofer
	Session 3B: Power Devices Reliability: Tutorial	**Session 3A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Tutorial	**Session 3C:** Progress in Failure Analysis Methods: Laser probing techniques
08:30	**10 Years Robustness Validation (Tutorial)** *SPEAKER: Eckhard Wolfgang, ECPE e.V. (DE) Werner Kanert, Infineon Technologies AG, (DE)*	**Fast Wafer Level Reliability Monitoring as a tool to achieve automotive quality for a wafer process (Tutorial)** *SPEAKER: Andreas Martin, Infineon Technologies AG (DE)*	**Laser Voltage Probing – its value and the race against scaling (invited)** *Ulrike Ganesh, Qualcomm (US)*
09:10			**Automatic process for Time-Frequency scan of VLSI** *SPEAKER: Anthony Boscaro, LE2i (FR)*
09:30	**Session 4B:** Power Devices Reliability: Metallization and Interconnects	**Session 4A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories - Part 1	**Static logic state analysis by TLS on powered logic circuits: Three case studies for suspected stuck-at failure modes** *SPEAKER: Clemens Helfmeier, Robert Bosch GmbH (DE)*
	Reliability aspects of copper metallization and interconnect technology for power devices (invited) *SPEAKER: Frank Hille, Infineon Technologies AG (DE)*	**Reliability Management – the central Enabler for Advanced Technologies in Automotive (invited)** *SPEAKER: Andreas Aal, Volkswagen AG (DE)*	
09:50			**Session 5:** Exhibitor Workshop: Defect Localization and Nanoprobing
			3D LIT calibration tool development *SPEAKER: Thijs Kempers, Maser Engineering (NL)*
10:00			**Improvements on localisation techniques for high power devices** *SPEAKER: Minh Vo, Hamamatsu Photonics Deutschland GmbH (DE)*
10:10	**Power Cycling Test and Failure Analysis of Molded Intelligent Power IGBT Module under Different Temperature Swing Durations** *SPEAKER: Francesco Iannuzzo, Aalborg University (DK)*	**Efficient reliability evaluation for combinational circuits** *SPEAKER: Hao Cai, Telecom Paristech (FR)*	**New phase Laser Voltage Imaging technique** *SPEAKER: Antoine Reverdy, Sector Technologies (FR)*
10:20			**Micromanipulators in Reliability Testing Environments: Fault Localization, Nanoprobing, and TEM Sample Preparation** *SPEAKER: Andrew Jonathan Smith, Kleindiek Nanotechnik GmbH (DE)*
10:30	**Power electronic assemblies: thermo-mechanical degradations of gold-tin solder for attaching devices** *SPEAKER: Faical Arabi, IMS (FR)*	**A process-variation-resilient methodology of circuit design by using asymmetrical forward body bias in 28nm FDSOI** *SPEAKER: You Wang, Télécom-ParisTech (FR)*	**Versatile probers for micro and nanoprobing** *SPEAKER: Karl Boche, Imina Technologies SA (CH)*
10:40			**EBIC and EBAC/RCI techniques** *SPEAKER: Grigore Moldovan, point electronic GmbH (DE)*

10:50–11:10 Coffee Break / Exhibition

Time	Room: Planck	Room: Einstein	Room: Fraunhofer
	Session 6B: Power Devices Reliability: SiC Devices	**Session 6A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories – Part 1 (continued)	**Session 6C:** Progress in Failure Analysis Methods: Nanoscale failure analysis
11:10	**Gate oxide degradation of SiC MOSFET under short-circuit aging tests** *SPEAKER: Safa Mbarek, University of Rouen (FR)*	**FPGA LUT delay degradation due to HCI: Experiment and simulation results** *SPEAKER: François Marc, University of Bordeaux (FR)*	**Scanning Microwave Microscopy for Electronic Device Analysis on Nanometre Scale** *SPEAKER: Sören Hommel, Infineon Technologies AG (DE)*
11:30	**Mission-profile-based stress analysis of bond-wires in SiC power modules** *SPEAKER: Francesco Iannuzzo, Aalborg University (DK)*	**Impact of Resistive Paths on NVM Array Reliability: Application to Flash & ReRAM Memories** *SPEAKER: Jérémy Postel-Pellerin, IM2NP (FR)*	**Current Imaging, EBIC/EBAC and Electrical Probing combined for fast and reliable in situ Electrical Fault Isolation** *SPEAKER: Stephan Kleindiek, Kleindiek Nanotechnik GmbH (DE)*
11:50	**Lifetime Estimation of SiC MOSFETs under High Temperature Reverse Bias Test** *SPEAKER: Kosuke Uchida, Sumitomo Electric Industries, Ltd. (JP)*	**Session 7:** Exhibitor Workshop: Sample Preparation **Sample Preparation with the X-Prep** *SPEAKER: Chris Richardson, Allied High Tech Products Inc. (US)*	**Electrical analysis on implantation-related defect by nanoprobing methodology** *SPEAKER: Changqing Chen, GLOBALFOUNDRIES Inc. (SG)*
12:00		**Laser Decap : the sample prep Swiss Army Tool** *SPEAKER: Yvan Pfeffer, Sector Technologies (FR)*	
12:10	**Power Cycling Analysis Method for High Voltage SiC Diodes** *SPEAKER: Viorel Banu, Centro Nacional de Microelectronica (ES)*	**SELA Sample Preparation Tools** *SPEAKER: Vladimir Zheleznyak, John P. Kummer GmbH*	**Cross-sectional Nanoprobing Fault Isolation Technique on Submicron Devices** *SPEAKER: Yuzhe Zhao, GLOBALFOUNDRiES Inc. (SG)*
12:20		**Curtaining-Free Top-Down TEM Lamella Preparation from a Cutting Edge Integrated Circuit** *SPEAKER: Tom Jaepel, Tescan a.s (CZ) / EO Elektronen-Optik-Service GmbH (DE)*	
12:30	**Development and characterisation of pressed packaging solutions for high-temperature high-reliability SiC power modules** *SPEAKER: Jose Angel Ortiz Gonzalez, University of Warwick (UK)*	**Helios G4: Enabling breakthrough failure analysis for 7 nm design nodes** *SPEAKER: David Donnet, FEI Company (NL)*	**Study on non-contact current path formation using charged particle beams** *SPEAKER: Yoji Mashiko, Oita University (JP)*
12:40		**Preliminary Idea for Preparing 1000's of TSV's** *SPEAKER: Roland Ries, Gatan GmbH (DE)*	

12:50–13:50 **Session 8:** Poster Session for Tracks:

Semiconductor Reliability & Failure Mechanisms

Progress in Failure Analysis Methods

Power Devices Reliability

Reliability & Failure Mechanisms of Special Devices (Photonics, anorganic and organic LED)

13:50–15:10 Lunch Break / Exhibition

Time	Room: Planck	Room: Einstein	Room: Fraunhofer
	Session 9B: Power Devices Reliability: Passives	**Session 9A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories - Part 2	**Session 9C:** EFUG – Workshop (Part 1)
15:10	**200V FRED diode with superior ESD capability** *SPEAKER: Andrea Irace, Università di Napoli Federico II (IT)*	**A run-time built-in approach of TID test in SRAM based FPGAs** *SPEAKER: Shaojun Wang, Harbin Institute of Technology (CN)*	**Ga contamination in silicon by focused ion beam milling: Atom Probe Tomography and simulation with dynamic model** *SPEAKER: Jin Huang, TU Dresden (DE)*
15:30	**Charging–discharging characteristics of a wound aluminum polymer capacitor** *SPEAKER: Ui Hyo Jeong, Korea Testing Certification (KR)*	**Reliability analysis of hybrid Spin Transfer Torque Magnetic Tunnel Junction/ CMOS Majority Voters** *SPEAKER: Mariem Slimani, Telecom ParisTech (FR)*	**Micro mechanical robustness tests of 28nm BEOL layer stack** *SPEAKER: Eckhard Langer, GLOBALFOUNDRIES Inc. (DE)*
15:50	**Session 10:** Exhibitor Workshop: Failure Analysis **Introduction of MA-tek total solution FA** *SPEAKER: Shih-Hsin Chang, Materials Analysis Technology Inc. (US)*	**Application of the Defect Clustering Model for Forming, SET and RESET Statistics in RRAM Devices** *SPEAKER: Nagarajan Raghavan, Singapore University of Technology and Design (SG)*	**Laser-based sample preparation for advanced packaging applications** *SPEAKER: Thomas Höche, Fraunhofer IMWS-CAM (DE)*
16:00	**Failure Analysis and Failure Prevention on Ceramic Capacitors** *SPEAKER: Jürgen Gruber, RoodMicrotec GmbH (DE)*		
16:10	**New technology approaches in scanning acoustic microscopy for advanced failure analysis** *SPEAKER: Peter Czurratis, PVA TePla Analytical Systems GmbH (DE)*	**Resistive RAM Variability Monitoring using a Ring Oscillator based Test Chip** *SPEAKER: Hassen Aziza, Aix-Marseille Université (FR)*	**Planar FIB Milling of Copper by using the Novel Rocking Stage Technology** *SPEAKER: Sharang Sharang, Tescan Orsay Holding a.s. (CZ)*
16:20	**Multiple Pass/Fail Detection Scheme** *SPEAKER: Romain Stomp, Zurich Instruments AG (CH)*		
16:30	**Below 10nm technology analysis solution** *SPEAKER: Ching Yu Tai, MESOSCOPE Technology Co., Ltd.(TW)*	**Permanent and Single Event Transient Faults Reliability Evaluation EDA tool** *SPEAKER: Cristina Meinhardt, Universidade Federal do Rio Grande do Sul (BR)*	**Fast, Reliable, Intuitive TEM Sample Preparation using a Load-Lockable Platform Combined with Smart Control Software** *SPEAKER: Stephan Kleindiek, Kleindiek Nanotechnik GmbH (DE)*
16:40	**High Resolution Cathodoluminescence for Defect Inspection and Failure Analysis** *SPEAKER: David Gachet, Attolight AG (CH)*		

16:50–17:10 Coffee Break / Exhibition

	Room: Planck	Room: Einstein	Room: Fraunhofer
	Session 11B: Power Devices Reliability: Testing Methods	**Session 11A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Space and Radiation	**Session 11C:** EFUG - Workshop (Part 2)
17:10	**Topologies for inverter like operation of power cycling tests** *SPEAKER: Christian Herold, TU Chemnitz (DE)*	**Natural Radiation Events in CCD Imagers at Ground Level** *SPEAKER: Tarek Saad Saoud, Aix-Marseille University (FR)*	**3D Inspection Solutions for 3D Devices** *SPEAKER: Ingo Schulmeyer, Carl Zeiss Microscopy (DE)*
17:30	**End of life and acceleration modelling for power diodes under High Temperature Reverse Bias stress** *SPEAKER: Oliver Schilling, Infineon Technologies AG (DE)*	**Single Event Transient Acquisition And Mapping For Space Device Characterization** *SPEAKER: Giovanna Mura, University of Cagliari (IT)*	**Innovative TEM sample Preparation on Helios G4 platform** *SPEAKER: David Donnet, FEI Company (NL)*
17:50	**Internal processes in power semiconductors at virtual junction temperature measurement** *SPEAKER: Weinan Chen, TU Chemnitz (DE)*		**FIB and P-FIB assisted sample preparation for in-situ TEM characterization** *SPEAKER: Remy Berthier, CEA-LETI (FR)*

18:30–20:30 Drinks Reception

	Room: Planck	Room: Einstein	Room: Fraunhofer
	Session 12A: Semiconductor Reliability & Failure Mechanisms: FD-SOI and RRAM	**Session 12B:** Failure mechanisms and precautions in plug connectors and relays: Tutorial	**Session 12C:** Students Workshop
08:30	**Device to circuit reliability correlations for Metal Gate / High-k transistors in scaled CMOS technologies (invited)** *SPEAKER: Andreas Kerber, GLOBALFOUNDRIES Inc. (US)*	**Failure mechanisms and precautions in plug connectors and relays (Tutorial)** *SPEAKER: Peter Jacob, EMPA Swiss Fed Labs for Materials Testing and Research (CH)*	
09:10	**FDSOI and Bulk CMOS SRAM Cells Resilience to Radiation Effects** *SPEAKER: Ricardo Reis, Universidade Federal de Rio Grande de Sul (BR)*		
09:30	**Performance vs. Reliability Adaptive Body Bias Scheme in 28nm & 14nm UTBB FDSOI nodes** *SPEAKER: Cheikh Ndiaye, STMicroelectronics (FR)*	**Session 13: EUFANET/CAM-Workshop** “Automotive Electronics Systems Reliability” (Part 1) **The southeast automotive hub and Georgia Tech’s automotive electronics ecosystem** *SPEAKER: Klaus-Juergen Wolter, Georgia Tech Atlanta, 3D Systems Packaging Research Center (US)*	
09:50	**Potentiality of Healing Techniques in Hot-Carrier Damaged 28nm FDSOI CMOS nodes** *SPEAKER: Alain Bravaix, Institut Supérieur de l’Électronique et du Numérique (FR)*		**Session 14: Reliability and Failure Mechanisms of special photonics and LED Devices:** LED systems **LED Degradation: from component to system (invited)** *SPEAKER: Benoit Hamon, Philips Lighting (NL)*
10:10	**Electromagnetic susceptibility characterization of double SOI device** *SPEAKER: Binhong Li, Institute of Microelectronics of Chinese Academy of Sciences (CN)*	**77Ghz Automotive RADAR in eWLB package: from consumer to automotive packaging** *SPEAKER: Gerhard Haubner, Infineon Technologies AG (DE)*	
10:30	**Analysis of Quantum Conductance, Read Disturb and Switching Statistics in HfO2 RRAM Using Conductive AFM** *SPEAKER: Alok Ranjan, Singapore University of Technology and Design (SG)*	**Reliability of automotive LED systems** *SPEAKER: Wolfgang Pohlmann, Hella KGaA Hueck & Co (DE)*	**Transient thermal testing for quality control of electronic devices** *SPEAKER: Dominik Müller, Technische Hochschule Ingolstadt (DE)*

10:50–11:10 Coffee Break / Exhibition

Session 15: Panel Discussion + Keynote 3

11:10 **Power and industry electronics – future perspectives for Europe**
SPEAKER: Sabine Herlitschka, Infineon Technologies AG (AT)

11:50 **Reliability – becoming the key factor for electronics in Europe? (Panel Discussion)**

Participants:

Berthold Hellenthal, AUDI AG (DE), Sabine Herlitschka, Infineon Technologies Austria AG (AT), Mervi Paulasto-Kröckel, Aalto University (FIN), Yves Gigase, ECSEL Joint Undertaking, Klaus-Juergen Wolter, Georgia Tech Atlanta, 3D Systems Packaging Research Center (US)

13:50–14:50 Lunch Break / Exhibition

Time	Room: Planck	Room: Einstein	Room: Fraunhofer
	Session 16A: Semiconductor Reliability & Failure Mechanisms: BTI	**Session 16B:** EUFANET/CAM-Workshop “Automotive Electronics Systems Reliability” (Part 2)	**Session 16C:** Reliability and Failure Mechanisms of special photonics and LED Devices: LED; laser diodes and VCSELs
14:50	**Degradation and Recovery of variability due to BTI** *SPEAKER: Andreas Martin, Infineon Technologies AG (DE)*	**Automotive Memory Trends and System Reliability Concepts** *SPEAKER: Reinhard Weigl, Micron Semiconductor GmbH (DE)*	**Experimental observation of TDDB-like behavior in reverse-biased green InGaN LEDs** *SPEAKER: Matteo Buffolo, University of Padova (IT)*
15:10	**Early Detection and Prediction of HKMG SRAM HTOL Performance by WLR PBTI Tests** *SPEAKER: Wei-Ting Chien, SMIC (CN)*		**Degradation of InGaN-based LEDs related to charge diffusion and build-up** *SPEAKER: Marco La Grassa, University of Padova (IT)*
15:30	**Session 17:** Exhibitor Workshop: Reliability Testing and Failure Analysis **Reliability Testing** *SPEAKER: David Sulyok, Mentor Graphics (DE)*	**Powertrain electronics reliability** *SPEAKER: Mihai Nica, AVL Deutschland GmbH (DE)*	**ESD tests on 850 nm GaAs-based VCSELs** *SPEAKER: Massimo Vanzi, University of Cagliari (IT)*
15:40	**Fault Isolation at 5um Resolution using Electro-Optical TDR with 6ps Rise Time** *SPEAKER: Atsushi Konno, Advantest Corporation (JP)*		
15:50	**Use of Lock-in Thermography and Magnetic Current Imaging as complemetary techniques for localization of shorts in GaN transistors** *SPEAKER: Fulvio Infante, Intraspec Technologies (FR)*	**Requirements for Reliability and new Solutions for Transmission Control Units** *SPEAKER: Michael Novak, Conti Temic microelectronic GmbH (DE)*	**Degradation of InGaN laser diodes caused by temperature- and current-driven diffusion processes** *SPEAKER: Carlo de Santi, University of Padova (IT)*
16:00	**TBC** *SPEAKER: NN, Digit Concept (FR)*		
16:10	**Solutions for semiconductor failure analysis with SEM** *SPEAKER: Simon Burgess, Oxford Instruments (UK)*	**Cu-wire Bond Reliability in Automotive Electronics** *SPEAKER: Rene Rongen, NXP Semiconductors (NL)*	**Catastrophic optical damage of high power InGaAs/AlGaAs laser diodes** *SPEAKER: Juan Jimenez, Universidad de Valladolid (ES)*
16:20	**NN** *SPEAKER: NN*		

16:30–16:50 Coffee Break / Exhibition

	Room: Planck	Room: Einstein	Room: Fraunhofer
	Session 18A: Semiconductor Reliability & Failure Mechanisms: Miscellaneous	**Session 18B:** EUFANET/CAM-Workshop "Automotive Electronics Systems Reliability" (Part 3)	**Session 18C:** Progress in Failure Analysis Methods: Novel non-destructive testing
16:50	**Plasma Process Induced Damage Detection by Fast Wafer Level Reliability Monitoring for Automotive Applications** *SPEAKER: Daniel Beckmeier, Infineon Technologies AG (DE)*	**Si IGBT reliability for HVs** *SPEAKER: Satoshi Yasuda, Toyota Motor Corporation (JP)*	**Copper Through Silicon Vias Studied by Photoelastic Scanning Infrared Microscopy** *SPEAKER: Martin Herms, PVA Metrology & Plasma Solutions GmbH (DE)*
17:10	**Channel width dependence of AC stress on bulk nMOSFETs** *SPEAKER: Donghee Son, Pohang University of Science and Technology (KR)*	**Power modules in automotive powertrains: qualification and test** *SPEAKER: Martin Rittner, Robert Bosch GmbH (DE)*	**Investigating Stress Measurement Capabilities of GHz Scanning Acoustic Microscopy for 3D Failure Analysis** *SPEAKER: Ahmad Khaled, IMEC (BE)*
17:30	**Effects of voltage stress on the single event upset (SEU) response of 65 nm flip flop** *SPEAKER: Chung Tah Chua, Nanyang Technological University (SG)*	**Reliability of inverters and DC Link capacitors for e-mobility** *SPEAKER: Tim Langer, Volkswagen AG (DE)*	**Detection and Analysis of Stress-induced Voiding in Al-Power lines by Acoustic GHz-Microscopy** *SPEAKER: Sebastian Brand, Fraunhofer IMWS-CAM (DE)*
17:50	**Conductive filament formation at grain boundary locations in polycrystalline HfO2 based MIM stacks- Computational and Physical Insight** *SPEAKER: Shubhakar Kalya, Singapore University of Technology and Design (SG)*	**Estimation of IGBT power module reliability in pre-design phase** *SPEAKER: Amelie Thionville, Valeo (FR)*	**Magnetic Field and Current Density Imaging using off-line Lock-In Analysis** *SPEAKER: Michael Kögel, Fraunhofer IMWS-CAM (DE)*
18:10	**Microcontroller susceptibility variations to EFT burst during accelerated aging** *SPEAKER: Jianfei Wu, National University of Defense Technology (CN)*	**Batteries and their reliability with special respect to traction applications** *SPEAKER: Marcel Held, EMPA Swiss Fed Labs for Materials Testing and Research (CH)*	**Detection of cracks in multilayer ceramic capacitors by X-ray imaging** *SPEAKER: Caroline Andersson, ABB Switzerland Ltd (CH)*

19:00–20:00 Concert / Church of St. Ulrici

20:00–22:00 Gala Dinner / Hotel Rotes Ross

	Room: Planck	Room: Einstein	Room: Fraunhofer
	Session 19A: Reliability & Failure Mechanisms of MEMS and sensors	**Session 19B:** Reliability & Failure Mechanisms in Packages and Assembly: Tutorial	**Session 19C:** Reliability & Failure Mechanisms of Wide Bandgap Devices: Tutorial
08:30	**Application of high frequency scanning acoustic microscopy for the failure analysis and reliability assessment of MEMS sensors (invited)** *SPEAKER: Stefan Oberhoff, Robert Bosch GmbH (DE)*	**Tutorial: Creeping corrosion of copper on printed circuit board assemblies (Tutorial)** *SPEAKER: Gert Vogel, Siemens AG (DE)*	**Field- and time dependent degradation of GaN HEMTs (Tutorial)** *SPEAKER: Enrico Zanoni, University of Padova (IT)*
09:10	**Dielectric charging phenomena in diamond films used in RF MEMS capacitive switches: The effect of film thickness** *SPEAKER: George Papaioannou, University of Athens (GR)*		
09:30	**Effects of residual stresses on cracking and delamination risks of an avionics MEMS pressure sensor** *SPEAKER: Juergen Auersperg, Fraunhofer ENAS (DE)*	**Session 20A:** Reliability & Failure Mechanisms in Packages and Assembly: Tutorial **Effects of salt spray test on lead-free solder alloy** *SPEAKER: Hélène Frémont, IMS-Bordeaux (FR)*	**Session 20B:** Reliability & Failure Mechanisms in Packages and Assembly: Tutorial **GaN devices: millimeter wave applications challenges (invited)** *SPEAKER: Sylvain Delage, III-V Labs (FR)*
09:50	**A novel correlative model of failure mechanisms for evaluating MEMS devices reliability** *SPEAKER: Yaqiu Li, Beihang University (CN)*	**Novel failure mode of chip corrosion at automotive HALL sensor devices under multiple stress conditions** *SPEAKER: Michél Simon-Najasek, Fraunhofer IMWS-CAM (DE)*	
10:10	**Optimization of contact metallizations for reliable wafer level Au-Sn bonds** *SPEAKER: Vesa Vuorinen, Aalto University (FN)*	**Moisture absorption by molding compounds under extreme conditions: impact on accelerated reliability tests** *SPEAKER: Amar Mavinkurve, NXP Semiconductors (NL)*	**Continuous Time-Domain RF waveforms monitoring under overdrive stress condition of AlGaN/GaN HEMTs** *SPEAKER: Denis Barataud, XLIM laboratory (FR)*
10:30		**Effect of PCBA surface morphology and chemistry on water layer formation under humid conditions and corrosion reliability** *SPEAKER: Kamila Piotrowska, Technical University of Denmark (DK)*	**Correlation of gate leakage and local strain distribution in GaN/AlGaN HEMT structures** *SPEAKER: Mikael Broas, Aalto University (FN)*

10:50–11:10 Coffee Break / Exhibition

Time	Room: Planck	Room: Einstein	Room: Fraunhofer
	Session 21A: Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Miscellaneous	**Session 21B:** Reliability & Failure Mechanisms in Packages and Assembly: Reliability and Modelling	**Session 21C:** Reliability & Failure Mechanisms of Wide Bandgap Devices: GaN power devices and deep level transient spectroscopy
11:10	**Early life field failures in modern automotive electronics – An overview, root causes and precautions** *SPEAKER: Peter Jacob, EMPA Swiss Fed Labs for Materials Testing and Research (CH)*	**Reliability Evaluation of Donut-Tungsten-Via as an Element of the Highly Robust Metallization** *SPEAKER: Verena Hein, X-FAB AG (DE)*	**Study of the stability of e-mode GaN HEMTs with p-GaN gate based on combined DC and optical analysis** *SPEAKER: Isabella Rossetto, University of Padova (IT)*
11:30	**Crack-guided effect on dynamic mechanical stress for foldable low temperature polycrystalline silicon thin film transistors** *SPEAKER: Sang Myung Lee, Yonsei University (KR)*	**Reliability Evaluation of Si-Dies due to Assembly Issues** *SPEAKER: Falk Naumann, Fraunhofer IMWS-CAM (DE)*	**UIS test of high-voltage GaN-HEMTs with p-type gate structure** *SPEAKER: Wataru Saito, Toshiba Corp. (JP)*
11:50	**Impact on Non-linear Capacitances on Transient Waveforms during System Level ESD Stress** *SPEAKER: Fabien Escudié, LAAS-CNRS (FR)*	**Fatigue testing method for fine bond wires in an LQFP Package** *SPEAKER: Bernhard Czerny, Vienna University of Technology (AT)*	**Temperature Dependent Dynamic ON State Resistance in GaN on Si Based Normally OFF HFETs** *SPEAKER: Eldad Bahat Treidel, Ferdinand-Braun-Institut für Höchstfrequenztechnik (DE)*
12:10	**Evolution study of the ElectroMagnetic Interference for RF LDMOS in series chopper application after thermal accelerated tests** *SPEAKER: Mohamed Ali Belaid, SAGE-ENISo (TN)*	**Fast and Trusted Intrinsic Stress Measurement to Facilitate Improved Reliability Assessments** *SPEAKER: Dietmar Vogel, Fraunhofer ENAS (DE)*	**Experimental study of the short-circuit robustness of 600V E-mode GaN transistors** *SPEAKER: Matthieu Landel, SATIE ENS Cachan CNRS CNAM (FR)*
12:30	**Temperature rise measurement for power-loss comparison of an aluminium electrolytic capacitor between sinusoidal and square current injections** *SPEAKER: Shin-Ichi Nishizawa, Kyushu Institute of Technology (JP)*	**Delamination of polyimide/Cu films under mixed mode loading** *SPEAKER: Thomas Walter, Vienna University of Technology (AT)*	**Local deep level transient spectroscopy using super-higher-order scanning nonlinear dielectric microscopy** *SPEAKER: Yasuo Cho, Tohoku University (JP)*

12:50–13:50 **Session 22:** Poster Session for Tracks:

Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems

Reliability & Failure Mechanisms in Packages and Assembly

Reliability & Failure Mechanisms of Wide Bandgap Devices

Reliability & Failure Mechanisms of MEMS and sensors

13:50–15:10 Lunch Break / Exhibition

15:10–16:00 Closing Ceremony

Abstracts – Oral Presentations

Session 1: Opening Session with Keynotes 1+2

22FDX and it's application in Energy Efficient Designs, Automotive and IoT - from foundry perspective

Manfred Horstmann, GLOBALFOUNDRIES Inc., Germany

We were used to execute according to Moore's Law over the last decades. This road leads the semiconductor industry into highly scaled technologies: 14, 10 and 7 nanometer.

However, economically a foundry should look towards the next hype building up, the Internet of Things. It is critical to offer the right technology to market at competitive cost with high performance, low power consumption and with build in connectivity. This automatically leads to Fully Depleted technologies with optional embedded RF capability as well as 28/22nm patterning, with no need of extensive use of double patterning or new light sources for lithography.

28nm is known as the "sweet spot" in Foundry Industry for yield/performance AND cost. This node is in high volume production and will be the basis to add technology features like embedded RF, Flash, High Voltage (HV) or other value add solutions and is already predicted to have a long lifetime in our industry. In particular embedded RF and HV are key to communicate with the outside analog world in a power efficient and user -friendly way.

Technology-wise, 22FDX is reusing proven 28nm processes, while adding new features. Devices on Fully Depleted SOI substrates can operate at voltages down to 0.4V with outstanding performance. This technology meets the desire of IOT products to be ultra mobile and enables small form factors. In addition, the technology setup is much simpler, requires a lower number of mask layers and is ideal for a broad range of low power devices for automotive and IOT applications at lower cost.

22FDX makes "Faster, cooler, simpler" a reality and delivers FinFET performance at 28nm costs.

Automotive Electronics Roadmap and the Wish List on Electronics

Berthold Hellenthal, Audi AG, Germany

Piloted driving, always connected, artificial intelligence and digitization are necessary ingredients for the mobility of tomorrow. The automotive industry, its applications, use cases and customer expectations are changing at a progressively faster speed. Already more than 80% of all automotive innovations are directly or indirectly enabled by semiconductors. How to resolve the conflicts between the latest semiconductor technologies and the stringent automotive quality and reliability requirements? How to solve the future automotive challenges towards autonomous driving and an always-on 24/7 operation? How to ensure a mission critical robustness?

The presentation will deduce a roadmap and a wish list on tomorrows automotive electronics from the new challenges.

Session 2: Opening Session - Exchange Papers

Quantitative model for post-program instabilities in filamentary RRAM

Robin Degraeve, A. Fantini, P. Roussel, S. Clima, M. Chen, B. Govoreanu, L. Goux, D. Linten, M. Jourczak, A. Thean, IMEC, Belgium; G. Gorine, University of Pavia, Italy

This paper discusses and models the program instability observed in filamentary Hf-based RRAM devices in the context of the Hourglass model. It is demonstrated that two variability sources can be distinguished: (i) number variations of the amount of vacancies in the filament constriction and (ii) constriction shape variations. The shape variations are not stable in time and show a log(time)-dependent relaxation behavior after each programming pulse. This makes program/verify schemes, aiming at widening the resistive window, highly ineffective. We develop a quantitative, mathematical description of the instability using an auto-correlated step process of the shape parameters of the QPC conduction model.

Asymmetric Low Temperature Bonding Structure Using Ultra-Thin Buffer Layer Technique for 3D Integration

Hao-Wen Liang, Ting-Yang Yu, Yao-Jen Chang and Kuan-Neng Chen, National Chiao Tung University, Taiwan

Wafer-level Sn/In-Cu bonding structure with Ni ultra-thin buffer layer is investigated to achieve a reduction in solder thickness, bonding temperature and duration. Furthermore, the asymmetric bonding structure is able to separate the manufacturing process of solder and electrical isolation layer. It is a promising approach for the application on hybrid bonding of three-dimensional integration.

Corrosion Mechanisms of Cu Bond Wires on AlSi Pads

Wantao Qin, George Chang, Harold Anderson Anderson, Tom Anderson Anderson, Denise Barrientos Barrientos, ON Semiconductor, US

Cu wires were bonded to AlSi (1%) pads, subsequently encapsulated and subjected to uHAST (un-biased Highly Accelerated Stress Test, 130 °C and 85% relative humidity). After the test, a pair of bonding interfaces associated with a failing contact resistance and a passing contact resistance were analyzed and compared, with transmission electron microscopy (TEM), electron diffraction, and energy dispersive spectroscopy (EDS). The data suggested the corrosion rates were higher for the more Cu-rich Cu-Al intermetallics (IMC). The corrosion was investigated with factors including electromotive force (EMF), self-passivation of Al, thickness and homogeneity of surface oxide on the IMC, ratio of the Cu-to-Al surface areas exposed to the electrolyte for an IMC taken into account. The preferential corrosion observed for the Cu-rich IMC is attributed to the high ratios of the surface areas of the cathode and anode that were exposed to the electrolyte, and degradation of the passivation of the surface oxide. With the understanding of the corrosion mechanisms, prohibiting the formation of Cu-rich IMCs is expected to be an approach to improve the corrosion resistance of the wire bonding, which is actually consistent with Pd-coating of the wire that is nowadays widely adopted in the industry.

Session 3A: Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Tutorial

Fast Wafer Level Reliability Monitoring as a tool to achieve automotive quality for a wafer process (Tutorial)

A. Martin, R.-P. Vollertsen, A. Mitchell, M. Traving, D. Beckmeier, H. Nielen, Infineon Technologies AG, Germany

After any process reliability qualification some tool is needed which verifies the stability of the process throughout mass production. A continuous "fast Wafer Level Reliability" (fWLR) Monitoring is essential especially for stringent product reliability specifications of automotive, medical or space applications. "Zero Defect" programs are well known and manifest the implementation of fWLR Monitoring on product wafers. However, often used quarterly reliability re-qualification cannot achieve this quality goal and is inappropriate. Therefore, fWLR Monitoring must be employed, covering reliability topics such as dielectric quality, plasma induced damage, device degradation and metallisation reliability. Additionally, fWLR can support a fast assessment of reliability during process development, split investigations, process tool changes and process qualifications.

In this tutorial an overview will be given on dedicated fWLR test structures, highly accelerated stress measurements, data analysis and sampling. Further, the challenges and limitations of the fWLR methodology will be pointed out as well as benefits will be highlighted. The topics of an out of control action plan, the scrapping of wafers with fWLR and defect density monitoring will be addressed.

This tutorial is suited for engineers and scientists who start in the area of reliability monitoring. But also experts who already work on this topic will benefit since also advanced methods are described. Valuable details and literature citations can be picked up.

Session 3B: Power Devices Reliability: Tutorial

10 Years Robustness Validation (Tutorial)

Eckhard Wolfgang, ECPE e.V., Germany; Werner Kanert, Infineon Technologies AG, Germany

It is a truism that reliability is related to applications requirements. Robustness Validation (RV) is a methodology to provide data demonstrating that a product is "fit for use". The ZVEI working group Robustness Validation was initiated 10 years ago. The concept has received increasing attention over this period, also beyond the automotive qualification procedures it initially originated from. The tutorial gives an overview of the basic concept of RV and experiences made in applying it to development and qualification. Two examples are discussed in detail: qualification of power modules and of thin-film DC-link capacitors. It also discusses difficulties in applying the concept.

Session 3C: Progress in Failure Analysis Methods: Laser probing techniques

Laser Voltage Probing – its value and the race against scaling (invited)

Ulrike Ganesh, Qualcomm, USA

After providing a brief introduction to Laser Voltage Probing (LVP), along with useful information and further reading suggestions, this paper provides a deep dive into current benefits and challenges of LVP applied to 16/14 nm FinFET technology and discusses the issues that arise from scaling of technology nodes according to the International Technology Roadmap for Semiconductors.

Automatic process for Time-Frequency scan of VLSI

Anthony Boscaro, Sabir Jacquir, Stéphane Binczak Le2i, France; Kevin Melendez, Kevin Sanchez, Philippe Perdu, CNES, France

Electro Optical Techniques (EOP: Electro Optical Probing and EOFM: Electro Optical Frequency Mapping) are effective backside contactless methods for defect localization and design debug for VLSI. The image mode (EOFM) gives only one frequency at each scan. In this case, the frequency mapping is a long and hard task. Furthermore, temporal information is not included in EOFM mode. Building a map by point by point EOP is usually too long so it cannot be used as it is to extract all the frequencies of interest in a region of interest. To overcome this limitation, we have developed an automatic process using EOP mode with a wavelets approach and autocorrelation. Temporal and frequency information are simultaneously computed with only one acquisition. We will underline the challenge and define application boundaries of this technique.

Static logic state analysis by TLS on powered logic circuits: Three case studies for suspected stuck-at failure modes

Clemens Helfmeier, Erik Frieß, J. Glück, Robert Bosch GmbH, Germany

Thermal Laser Stimulation (TLS) for static logic state analysis is applied to failure analysis. Three case studies of analyses of the digital logic in an automotive Application Specific Integrated Circuit (ASIC) are discussed. By analyzing the logic states of the circuit we were able to identify the mechanism and localize the site of irregular behavior non-destructively, both for a stuck-at fault and two weak interconnects. The approach measures the power supply current while applying TLS to the device back side. This allows an extremely high analysis coverage, because every transistor is connected to the power supply, making this method a universal tool for every digital circuit failure analysis (FA) workflow, because the gained understanding of the fault allows to replace multiple steps of alternative FA techniques by only a single technique, reducing time and cost for successful FA.

Session 4A: Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Tutorial

Reliability Management – the central Enabler for Advanced Technologies in Automotive (invited)

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Mobility is in a transition phase from individual human controlled to assisted and autonomous driving. Also, new roles add to car manufacturers being now forced to adapt to digital service providers as cars become the ultimate mobile office. Today, functional automotive requirements start to exceed on what's on the market accompanied with huge reliability assurance process gaps along the supply chain. Standards are out dated, research data unavailable and activities to change this strongly bound to market dynamics and mass volume requirements. This is why reliability engineering and management becomes a leading role in product design and business model formation. Transparency about technological gaps and how they are being handled determine market positions. To create industry awareness, we demonstrate two examples out of an OEM driven study on mechanical induced parametric deviations which relate to corresponding product verification/validation issues that can end up in real, but which are mostly classified as no fault found (NFF) issues.

Efficient reliability evaluation for combinational circuits

Hao Cai, Kaikai Liu, Lirida Naviner, Jean-François Naviner, Telecom Paristech, France

Reliability evaluation methodologies have become important in circuit design. In this paper, we focus on the probabilistic transfer matrix (PTM), which has proven to be a gate-level approach for accurately assess the reliability of a combinational circuit with penalty in simulation runtime and memory usage. In order to improve its efficiency, several methodologies based on traditional PTM are proposed. A general tool is developed to calculate the reliability of a circuit with efficient computation methods based on an optimized PTM (denoted as ECPTM), which achieves runtime and memory usage improvement. Experiments demonstrate how the proposed simulation framework, combined with traditional PTM method, can provide significant reduction in computation runtime and memory usage with different benchmark circuits.

A process-variation-resilient methodology of circuit design by using asymmetrical forward body bias in 28nm FDSOI

You Wang, Hao Cai, Lirida Naviner, Telecom Paristech, France; Jacques-Olivier Klein, Institut d'Electronique Fondamentale, France; Weisheng Zhao, Beihang University, China

Due to the process variation, Spin Transfer Torque Magnetic Tunnel Junction (STT-MTJ) faces great challenges in fabrication process. Meanwhile, its neighbor CMOS is also influenced by significant process variation with the continuous technology scaling down. Both of the two effects lead to degraded performance of hybrid MTJ/CMOS circuit. This paper proposes a methodology to alleviate the impact of process variation on the performance of MTJ based applications. The methodology is presented by carrying out a novel design of non-volatile flip-flop (NVFF) using asymmetrical forward body bias (FBB) in fully depleted silicon on insulator (FD-SOI). Simulation results show that the sensing errors have been almost removed by this method with the minimum size of circuit. In addition, the thermal robustness of this circuit has also been dramatically improved.

Session 4B: Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Tutorial

Reliability aspects of copper metallization and interconnect technology for power devices (invited)

Frank Hille, Roman Roth, Carsten Schäffer, Holger Schulze, Nicolas Heuck, Daniel Bolowski, Karsten Guth, Alexander Ciliox Ciliox, Karina Rott Rott, Frank Umbach, Infineon Technologies AG, Germany

The introduction of thick copper metallization and topside interconnects as well as a superior die attach technology is improving the performance and reliability of IGBT power transistor technologies significantly. The

much higher specific heat capacity and higher thermal conductivity increases the short circuit capability of IGBTs, which is especially important for inverters for drives applications. This opens the potential to further optimize the electrical performance of IGBTs for higher energy efficiency. The change in metallization requires the introduction of a reliable barrier against copper diffusion and copper silicide formation. This requires the development of an efficient test method and reliability assessment according to a robustness validation approach. In addition, the new metallization enables interconnects with copper bond wires, which yield, together with an improved die attach technology, a major improvement in the power cycling capability.

Power Cycling Test and Failure Analysis of Molded Intelligent Power IGBT Module under Different Temperature Swing Durations

Ui-Min Choi, Frede Blaabjerg, Francesco Iannuzzo, Huai Wang, Christian Uhrenfeldt, Stig Munk-Nielsen, Aalborg University, Denmark; Søren Jørgensen, Grundfos Holding A/S, Denmark

Molded IGBT modules are widely used in low power motor drive applications due to their advantage like compactness, low cost, and high reliability. Thermo-mechanical stress is generally the main cause of degradation of IGBT modules and thus much research has been performed to investigate the effect of temperature stresses on IGBT modules such as temperature swing and steady-state temperature. The temperature swing duration is also an important factor from a real application point of view, but there is a still lack of quantitative study. In this paper, the impact of temperature swing duration on the lifetime of 600 V, 30 A, 3-phase molded Intelligent Power Modules (IPM) and their failure mechanisms are investigated. The study is based on the accelerated power cycling test results of 36 samples under 6 different conditions and tests are performed under realistic electrical conditions by an advanced power cycling test setup. The results show that the temperature swing duration has a significant effect on the lifetime of IGBT modules. Longer temperature swing duration leads to the smaller number of cycles to failure. Further, it also shows that the bond-wire crack is the main failure mechanism of the tested IGBT modules.

Power electronic assemblies: thermo-mechanical degradations of gold-tin solder for attaching devices

Faical Arabi, Loic Theolier, Eric Woirgard, IMS University of Bordeaux, France; Donatien Martineau, Labinal Power Systems, France; Jean-Yves Deletage, University of Bordeaux, France

The eutectic Au80Sn20 solder alloy has been applied in semiconductor assemblies and other industries for years. Due to some superior physical properties, Au/Sn alloy gradually becomes one of the best materials for soldering in electronic devices and components packaging but the voids growth in AuSn solder joints is one of the many critical factors governing the solder joint reliability. Voids may degrade the mechanical robustness of the die attach and consequently affect the reliability and thermal conducting performance of the assembly. Severe thermal cycles [–55 °C / +175 °C] have highlighted degradations in AuSn die attach solder. The inspection of as-prepared die-attachments by X-ray and SEM (observation of cross-section) shows that the initial voids sizes were increased and a propagation of transverse cracks inside the joint between voids has appeared after ageing, it was featured also the existence of the IMC typical scallop-shape morphology with the phase structure of (Ni, Au)3Sn2 on as-reflowed joints. In this paper, we evaluate the origin of these degradations and ways to address them.

Session 6A: Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories - Part 1

FPGA LUT delay degradation due to HCI : Experiment and simulation results

Mohammad Naouss, François Marc, University of Bordeaux, France

Reliability of advanced VLSI circuits becomes more and more important as both product designers and manufactures relentlessly pursue technology advantages and stretch device physical limits to capitalize the consumer electronic market. In this paper, we focus on aging degradation of the Look-Up Table (LUT) on FPGAs. We have characterized the delay degradation of LUT dependent on the duty cycle and the frequency of stress signal. We have identified that the HCI degradation mechanism affects the fall delay more than the rise delay, it is related directly to the frequency stress and independent from the duty cycle. In addition, we built a model of the delay degradation due to HCI depending on switching frequency of stress signal and the aging time. Furthermore, we identified the relation between the effect of each aging transistor and the LUT delay for the HCI aging mechanism. This work is ideal for modelling the LUT aging mechanisms in FPGA.

Impact of Resistive Paths on NVM Array Reliability: Application to Flash & ReRAM Memories

Pierre Canet, Jérémy Postel-Pellerin, Hassen Aziza, IM2NP, France

In memory technology, size reduction induces consequences in terms of reliability, including an increase in the line resistances and a voltage drop along the line during memory operation. This problem can occur in Flash products during sector erase mode, and in resistive RAM (ReRAM) during forming, reset or word-reading modes. In this paper we apply a simple resistive model to determine the wordline (or bitline) length of a Flash memory (and thus to optimize the Flash memory array's size) or the word length of a ReRAM, according to specific reliability criteria: the threshold voltage drop of cells along a line in a Flash memory sector, or the resistance variation of the cells in a ReRAM word.

For the technologies considered in this paper, on the one hand we demonstrate a maximal threshold voltage drop of 2V for a 4 Gbit Flash array and we provide design recommendations, and on the other hand we demonstrate that a maximal word length of 32 bits for ReRAM can be achievable in a ReRAM matrix. The presented methodology can easily be extended to any memory technology.

Session 6B: Power Devices Reliability: SiC Devices

Gate oxide degradation of SiC MOSFET under short-circuit aging tests

Safa Mbarek, Pascal Dherbecourt, Mohamed Masmoudi Olivier Latry, Groupe de Physique des Matériaux, France; François Fouquet, Irseem, France

SiC MOSFETs reliability issues remain a challenge that requires further investigation. In this article, a short-circuit aging test was developed to characterize the electrical parameter evolution. The threshold voltage and gate drain capacitance seem to be relevant degradation indicators. These two parameters indicate a gate oxide degradation. Electron trapping in the oxide layer could be the mechanism behind this deterioration.

Mission-profile-based stress analysis of bond-wires in SiC power modules

Amir Sajjad Bahman, Francesco Iannuzzo, Frede Blaabjerg, Aalborg University, Denmark

This paper proposes a novel mission-profile-based reliability analysis approach for stress on bond wires in Silicon Carbide (SiC) MOSFET power modules using statistics and thermo-mechanical FEM analysis. In the proposed approach, both the operational and environmental thermal stresses are taken into account. The approach uses a twodimension statistical analysis of the operating conditions in a real one-year mission profile sampled at time frames 5 minutes long. For every statistical bin corresponding to a given operating condition, the junction temperature evolution is estimated by a thermal network and the mechanical stress on bond wires is consequently extracted by finite-element simulations. In the final step, the considered mission profile is translated in a stress sequence to be used for Rainflow counting calculation and lifetime estimation.

Lifetime Estimation of SiC MOSFETs under High Temperature Reverse Bias Test

Kosuke Uchida, Toru Hiyoshi, Taro Nishiguchi, Hirofumi Yamamoto, Masaki Furumai, Takashi Tsuno, Yasuki Mikamura, Sumitomo Electric Industries Ltd., Japan

Reliability physics of silicon carbide (SiC) metal-oxide semiconductor field-effect transistor (MOSFET) is not sufficiently clear; therefore an accurate estimation method of lifetime has been strongly required. The relationship between the failure time of 4H-SiC double implanted MOSFETs under high temperature reverse bias test and the doping concentration in a drift layer was studied to clarify the failure physics. The failure time of the device showed dependence on the doping concentration in the 150 mm wafer. The breakdown occurred at the gate oxide over the threading dislocation in the JFET region. The electric field simulation indicated that the oxide electric field linearly depends on the doping concentration, which means the failure time depends on the oxide electric field. According to these results, the electric field acceleration tests were conducted with the samples in the uniform area of the doping concentration so as to exclude the distribution of the oxide electric field in each sample. The lifetime showed dependence on the oxide electric field varied by the drain bias intentionally. These results revealed the importance of the doping concentration uniformity of the epitaxial layer and we established the method to estimate the lifetime accurately.

Power Cycling Analysis Method for High Voltage SiC Diodes

Viorel Banu, D+T Microelectronica A.I.E., Spain; Victor Soler, Josep Montserrat, José Millán, Philippe Godignon, IMB-CNM, CSIC, Spain

This work describes a novel analysis method for the power cycling test, developed for high voltage and temperature silicon carbide diodes. The silicon carbide devices working at temperatures beyond 170°C, the maximum temperature rating for silicon devices, need specific reliability tests adapted to high temperature operation of this new generation of power devices. The specificity of the further presented method consist in the use of 10ms sinusoidal power current pulses that are able to evidence the temperature developed inside the diode during the power pulse, the temperature characteristic delay versus the applied current and the temperature calibration method. Moreover, this overall method is able to evidence the transformations occurred in the bonding contact and the dye attach.

Development and characterisation of pressed packaging solutions for high-temperature high-reliability SiC power modules

Jose Angel Ortiz Gonzalez, Olayiwola Alatise, Li Ran, Philip Mawby, University of Warwick, United Kingdom; Attahir Murtala Aliyu, Alberto Castellazzi, University of Nottingham, United Kingdom

SiC is a wide bandgap semiconductor with better electrothermal properties than silicon, including higher temperature of operation, higher breakdown voltage, lower losses and the ability to switch at higher frequencies. However, the power cycling performance of SiC devices in traditional silicon packaging systems is in need of further investigation since initial studies have shown reduced reliability. These traditional packaging systems have been developed for silicon, a semiconductor with different electrothermal and thermomechanical properties from SiC, hence the stresses on the different components of the package will change. Pressure packages, a packaging alternative where the weak elements of the traditional systems like wirebonds are removed, have demonstrated enhanced reliability for silicon devices however, there has not been much investigation on the performance of SiC devices in press-pack assemblies. This will be important for high power applications where reliability is critical. In this paper, SiC Schottky diodes in pressure packages have been evaluated, including the electrothermal characterisation for different clamping forces and contact materials, the thermal impedance evaluation and initial thermal cycling studies, focusing on the use of aluminium graphite as contact material.

Session 6C: Progress in Failure Analysis Methods: Nanoscale failure analysis

Scanning Microwave Microscopy for Electronic Device Analysis on Nanometre Scale

Sören Hommel, Nicole Killat, Thomas Schweinboeck, Andreas Altes, Infineon Technologies AG, Germany; Doris Schmitt-Landsiedel, Technische Universität München, Germany; Marco Silvestri, Oliver Häberlen, Infineon Technologies Austria AG, Austria

Probing electrical properties of state-of-the-art electronic devices is one of the key features of Scanning Microwave Microscopy. While providing valuable information on charge carrier properties, the combination of an atomic force microscope cantilever with a microwave signal raises the question on the actual spatial resolution of the system. On the example of the highly confined two-dimensional electron gas of an AlGaN/GaN structure, the effective tip radius is demonstrated to be in the range of the theoretical tip radius for sharp tips, while both values differ for unevenly shaped cantilever tips. The presented method demonstrates the role of the microwave excitation region for the spatial resolution of the system as well as the potential of this method to characterise the effective tip radius.

Current Imaging, EBIC/EBAC, and Electrical Probing combined for fast and reliable in situ Electrical Fault Isolation

Stephan Kleindiek, Klaus Schock, Andreas Rummel, Kleindiek Nanotechnik, Germany; Michael Zschornack, Pascal Limbecker, Andreas Meyer, Matthias Kemmler, Global Foundries, Germany

Using a compact nanoprobing setup comprising eight probe tips attached to piezo-driven micromanipulators, various techniques for fault isolation are performed on 28 nm samples inside an SEM. The employed techniques include nanoprobing as well as EBAC. The recently implemented Current Imaging technique is used to quickly image large arrays of contacts providing a means of locating faults. In this case, Current Imaging provides insight into the sample's behaviour yielding qualitatively comparable results to the more cumbersome cAFM technique. While the results of the TEM investigations including EDX mappings were inconclusive, the Current Imaging technique clearly shows that the root cause is located below the SiGe layer. By combining these techniques inside a FIB/SEM microscope, it is possible to locate and characterize a failure as well as prepare a TEM lamella for further investigation without the necessity to switch to a different tool.

Electrical analysis on implantation-related defect by nanoprobing methodology

Changqing Chen, Pengtiong Ng, Ghim Boon Ang, GLOBALFOUNDRIES Inc., Singapore

Implantation is the key process in the modern semiconductor process which forms the basic device cell by different doping ditribution, depth, angle and element type. They are the key factors to affect the transistor performance, but the implantation-related defect is invisible by the normal failure analysis method. Then electrical analysis and verification is necessary to visualize this kind of defect. Electrical theory is important in this kind of failure analysis to indirectly proven the problematic process. The transistor body effect is a well know effect which is utilized in some kind of IC design to change the transistor Vth for certain purpose. But nobody uses this effect for the implantation-related failure analysis since the implant itself is complex and is not ideally uniform as the theory model. In this paper, implantation-related defect was successfully identified by the application of transistor body effect combined with nanoprobing on the localized structure.

Cross-sectional Nanoprobing Fault Isolation Technique on Submicron Devices

Pik Kee Tan, Huei Hao Yap, Chang Qing Chen, Fransiscus Rivai, Yuzhe Zhao, Hua Feng, Hao Tan, Zhi Hong Mai, GLOBALFOUNDRIES Inc. Singapore Pte. Ltd, Singapore

With continuous scaling on CMOS device dimensions, it is becoming increasingly challenging for conventional failure analysis (FA) methods to identify the failure mechanism at the circuit level in an integrated chip. Scanning Electron Microscopy (SEM) based nanoprobing is becoming

an increasingly critical tool for identifying non-visual failures via electrical characterization in current electrical FA metrology for fault isolation since 2006 [1-3]. Currently, most of the nanoprobing fault isolation is nanoprobe in top-down planar direction, such as nanoprobe on via, contact and metal line. This paper focused on fault isolation of sub-micron devices by nanoprobing on a crosssectional plane. This is a new application area; it is very useful for sample that cannot perform fault isolation with conventional top-down planar nanoprobing, especially on non-volatile memory that with single transistor memory array that arrange in a vertical direction, such as Magnetic Random Access Memory (MRAM), Phase-Change Random Access Memory (PC-RAM), flash memory and etc.

Study on non-contact current path formation using charged particle beams

Yoji Mashiko, Oita University, Japan

For measurement of electrical characteristics it is essential to supply an electrical current or apply a voltage to the circuit. This study have been carried in order to realize the creation of a stable electrical current flow in the microscopic region only by using the charged particle beams, without requiring contact of the mechanical probes. And it was revealed that stable and constant current flow can be achieved in a self-aligned current-controlling manner by utilizing the secondary electrons. We also have clarified that the mechanism of stabilizing current in a self-aligned manner is dependent on space charge limited current of secondary electrons.

Session 8: Poster Session for Tracks:

- Semiconductor Reliability & Failure Mechanisms
- Progress in Failure Analysis Methods
- Power Devices Reliability
- Reliability & Failure Mechanisms of Special Devices (Photonics, anorganic and organic LED)

Numerical study of destruction phenomena for punch-through IGBTs under unclamped inductive switching

Tomohiro Tamaki, Yoshinori Yabuuchi, Masato Izumi, Norio Yasuhara, Kazutoshi Nakamura, Semiconductor & Storage Company, Toshiba Corp., Japan

In this paper, a numerical description of the ruggedness of punch-through (PT) IGBTs under the unclamped inductive switching (UIS) has been proposed using two-dimensional (2D) simulations with the calibration to experimental results. The UIS capability is an important design factor of device structures for the purpose of screening defects produced during the wafer process. The local hot spot due to the current filament threedimensionally (3D) distributed over the chip area requires 3D simulations to reproduce the current density of the filament and its behavior leading to the device destruction; however, it is difficult to simulate such a large area with an appropriate mesh size and a boundary condition. To provide a possible solution of this technical issue, 2D simulations using large scale multi-cell structures with the increased current density has been proposed to reproduce experimental results without resorting to 3D simulations. With this approach, not only destructive phenomena including the UIS ruggedness and the latch-up failure mode have been reproduced, but also the device internal state leading to the destruction has been revealed. The spatial distribution of the electric potential and the lateral electric field during the UIS condition is shown to be a key role determining the current filament width and the UIS ruggedness. Besides, the high frequency oscillation of the collector voltage during the UIS observed by experiments has been analyzed and has found to be related with the hopping motion of the current filament from a cell to its neighboring cell of the device.

Accelerated Life Test of high luminosity blue LEDs

Eduardo Nogueira, Vincenzo Orlando, Jorge Ochoa, Universidad Politecnica Madrid, Spain

A complete Accelerated Life Test on high luminosity blue LEDs is presented. The test was conducted at different temperatures, humidity and current conditions, involving a total of seven individual tests. Life models were obtained for the catastrophic failures of the tests and then a complete temperature, humidity and current model was developed, which enabled the calculation of the life of the LEDs for any of these conditions. Catastrophic failures and model parameters were consistent with earlier results using different high luminosity LEDs. Non-catastrophic failures were modelled with their corresponding luminous power loss on each test, with expected results.

Reliability Design of Direct Liquid Cooled Power Semiconductor Module for Hybrid and Electric Vehicles

Yangang Wang, Dynex Semiconductor, United Kingdom

With the global interests and efforts in popularizing low carbon vehicles, automotive power module has been becoming one of the fastest growing sectors in power semiconductor industry. As working in a harsh environment, the performance and reliability requirements of automotive module are stringent than industrial products. In this work, an integrated direct liquid cooled power module with enhanced reliability for hybrid and electric vehicles (HEV/EV) is developed. The design and assembly of the module were optimized in terms of performance, weight, cost and reliability. The module is integrated Al direct liquid cooling structure, leading to about 40% reduction of weight and cost and almost 50% reduction of junction to heat sink thermal resistance. Therefore, the junction temperature stays below the upper limit at the worst operation case which enhances the thermal reliability and lifetime. By incorporating advanced die lead bonding, the parasitics can be reduced by 50%, which is beneficial to efficiency and reliability. Furthermore, the die and terminal attach technologies are investigated to improve reliability. The lifetime prediction under a typical driving cycle shows that the proposed module is capable of working in the whole vehicle service period.

Micro PCB Rogowski coil for current monitoring and protection of high voltage power modules

Masanori Tsukuda, Green Electronics Research Institute, Japan; Masahiro Koga, Kenta Nakashima, Ichiro Omura, Kyushu Institute of Technology, Japan

We have developed a printed circuit board Rogowski coil for monitoring of current and protection of highvoltage power modules and packages. It is small, thin, and inexpensive current sensor and is almost the ideal Rogowski coil because of its fishbone pattern. For noise reduction under high-voltage/-current conditions in a module, shield layers and coaxial connector are employed. In addition, a new, fast simulation tool was developed to optimize the main coil pattern for realization of arbitrary printed circuit board geometry in specific, limited spaces.

Effects of stress-loading test methods on the degradation of light-emitting diode modules

Miao Cai, Daoguo Yang, Guilin, Xianping Chen, University of Electronic Technology, China; Jianlin Huang, Guoqi Zhang, TU Delft, Netherlands

This study investigates the degradation of light-emitting diode (LED) lamp modules by various stress–load test approaches, namely, step-up stress accelerated degradation testing, step-down stress accelerated degradation testing (SDSADT), and constant stress accelerated degradation testing. Two types of commercial LED lamps with different capabilities of heat dissipation (CHDs) are utilized in the experiment. LM-80 testing on two types of LED packages is further implemented to reproduce the degradation reaction of Lamp B. Result shows that SDSADT can effectively alleviate the initial increase in optical parameters. Lamp B with a strong CHD exhibits a similar lumen decay rate at each stress of step stress testing; this similarity implies that the decay rate of Lamp B is only related to the current loaded stress. The lumen decay rate of the initial decay paths for Lamp B as the thermal stress increases exhibits a parabolic law. This parabolic pattern is also detected in the LM-80 testing for the LED packages and is explained by the strong CHD of Lamp B. The thermally induced mechanisms, which influence the optical emission of LEDs, should be responsible for the parabolic decay law. Moreover, the color shift of the LED modules with increasing loaded stresses is more sensitive than lumen degradation.

Nanowire width dependence of data retention and endurance characteristics in nanowire SONOS flash memory

Jin Hyung Choi, Chong Gun Yu, Jong Tae Park, Incheon National University, Korea

The investigations on the nanowire width (W) dependence of memory performance including P/E (programming and erasing) speed, data retention time and endurance characteristics in nanowire SONOS flash memory have been performed through the measurement and the device simulation. From measured results, a narrow device has advantages in terms of a fast P/E speed and the endurance characteristics. However, a narrow device has disadvantage in terms of the decreased data retention time. Another disadvantage of a narrow device is expected to the large power consumption due to large GIDL (Gate Induced Drain Leakage) current. The device simulation was performed to explore the causes for a fast P/E speed, an enhanced endurance characteristics and the reduced data retention time in narrow devices.

Novel heatsink for power semiconductor module using high thermal conductive graphite

Yasushi Yamada, Masashi Yanase, Daiki Miura, Daido University, Japan; Katsuhiro Chikuba, Thermo Graphitics Co., Ltd., Japan

The thermal properties and reliability of novel heatsinks that use high thermal conductivity graphite were investigated. Graphite plates with different high-thermal-conductivity directions were laminated together using an Ag-based brazing material, with thin Cu plates on their outer surfaces. The heatsinks were bonded to Si heater chips using Sn-3Ag-0.5Cu solder. Samples with conventional Cu or Cu-65Mo heatsinks were also fabricated as references. The samples were attached to an active cooling plate subjected to a constant water flow, and thermal and reliability measurements were conducted. The experimental results were also compared with the results of a finite element analysis. The novel laminated heatsinks exhibited a lower thermal resistance than the Cu or Cu-65Mo heatsinks, and the experimental results were in reasonable agreement with those of the finite element analysis. The graphite-based heatsinks had better power cycle reliability than Cu-based heatsinks. Therefore, these novel graphite heatsinks have potential for application to power semiconductor modules, it seems to be useful for applications with high heat flux of power semiconductor devices.

Mechanisms of metallization degradation in high power diodes

Mads Brincker, Peter Kjær Kristensen, Kristian Bondeup Pedersen, Vladimir Popok, Aalborg University, Denmark

Under operation the topside metallization of power electronic chips is commonly observed to degrade and thereby affects the device electrical characteristics. However, the mechanisms of the degradation process and role of environmental factors are not yet fully understood. In this work, we investigate the metallization degradation by passive thermal cycling of unpackaged high-power diode chips in different controlled atmospheres. The electrical degradation of the metallization is characterized by sheet resistance measurements, while the microstructural damage is investigated by scanning electron microscopy (SEM) and X-ray diffraction (XRD). To study the evolution of chemical composition of the metallization, energy dispersive X-ray spectroscopy (EDX) is also applied. Since the degradation depends on initial microstructure of the metallization, the film texture and grain size distribution is determined using electron backscatter diffraction (EBSD). The obtained data show that the type of atmosphere plays a minor role in the degradation process, with a slight tendency that cycling in dry nitrogen atmosphere accelerates the degradation compared to the experiments in ambient atmosphere with controlled relative humidity of 50 and 95%.

Application of Laser Deprocessing Technique in PFA on Chemical Over-etched on Bond-pad Issue

Huei Hao Yap, Pik Kee Tan, Zhihong Mai, Hao Tan, Jeffrey Lam, Lei Zhu, GLOBALFOUNDRIES Inc. Singapore Pte Ltd., Singapore

With technology scaling of semiconductor devices and further growth of the integrated circuit (IC)1 design and function complexity, the package size has shrank down proportionally too. Hence, flip-chip solder bump mounting is the current semiconductor devices trend to replace the wire bonding technology. When come to PFA2 on the flip-chip devices with solder bump, wet etch for solder bump removal is an essential method. Upon using wet etch methodology; it is very dependent on etching timing and the chemical aggressiveness to get a good removal result for the solder bump. If there is an excessive period in etching or chemical reacts too aggressively, chemical over-etched on bond pad will occur. It is very unfavorable for FA3 engineer to perform subsequent reverse engineering on the bond pad over-etched device. In this paper, the application of laser deprocessing technique is proposed to solve the bond pad over-etched issue. This proposed technique is a quick and reversal way in deprocessing technique for defect identification in PFA.

Avalanche Robustness of SiC Schottky Diode

Ilyas Dchar, SuperGrid-Institute, France; Cyril Buttay, Laboratoire Ampere, INSA de Lyon, CNRS UMR 5005, France; Hervé Morel, INSA/ Ampère, France

Reliability is one of the key issues for the application of Silicon carbide (SiC) diode in high power conversion systems. For instance, in high voltage direct current (HVDC) converters, the devices can be submitted to high voltage transients which yield to avalanche. This paper presents the experimental evaluation of SiC diodes submitted to avalanche, and shows that the energy dissipation in the device can increase quickly and will not be uniformly distributed across the surface of the device. It has been observed that failure occurs at a fairly low energy level (<0.3 J/cm²), on the edge of the die, where the electrical field intensity is the greatest. The failure results in the collapse of the voltage across the diode (short-circuit failure mode). If a large current is maintained through the diode after its failure, then the damage site is enlarged, masking the initial failure spot, and eventually resulting in a destruction of the device and an open circuit.

Application of Fast Laser Deprocessing Techniques on Large Cross-sectional View Area Sample with FIB-SEM Dual Beam System

Yuzhe Zhao, Pikkee Tan, Hueihao Yap, Binghai Liu, Hua Feng, Hao Tan, Ran He, Yamin Huang, Dandan Wang, Lei Zhu, Changqing Chen, Fransiscus Rivai, Yinzhe Ma and Zhihong Mai, GLOBALFOUNDRIES Inc. Singapore Pte. Ltd, Singapore;Qijie Wang, Nanyang Technological University

Cross-sectional analysis is one of the important areas for physical failure analysis. Focus Ion Beam (FIB) and mechanical polish sample preparation are commonly used and necessary techniques in the semiconductor industry and Failure Analysis (FA) Company [1]. However, each technique has its own limitation. Mechanical polishing technique easily induces artifact by mechanical force, especially on advance technology node. FIB can eliminate mechanically damaged artifact, but have the limitation on cross-sectional view area. Another potential technique will be plasma FIB, it used very high milling current and fast milling speed [2]. However, it comes with a very high cost and having the contamination issue. The contamination issue greatly affects the low kV Scanning Electron Microscopy (SEM) imaging quality. In recent semiconductor industry FA, low kV SEM imaging is preferable, because high kV imaging will introduce delamination artifacts especially on organic material from packaged sample. In this paper, Fast Laser Deprocessing Techniques (FLDT) application is further enhanced on large area cross-sectional FA with fast cycle time and low-cost equipment [3-4]. This is to prevent from mechanical damage. In short, the proposed FLDT is a costeffective and quick way to deprocess a sample for defect identification in cross-sectional FA.

Influence of I/O Oxide Process on the NBTI Performance of 28nm HfO2-Based HKMG p-MOSFETs

Weiting Chien, Yueqin Zhu, Atman Zhao, SMIC, China

The NBTI (Negative Bias Temperature Instability) performance of 28nm HfO2-based HKMG (High-κ Metal Gate) I/O thick oxide p-MOSFETs with different I/O oxide processes is reported. The results show that the NBTI performance from ISSG (In-Situ Steam Generation) process is better than that from the furnace Gox1 process. The NBTI dependence on the PDA (Post Deposition Anneal) process is studied and we show that PDA can significantly improve NBTI. We investigate the influence of DPN (Decoupled Plasma Nitridation) on NBTI; the NBTI performance from the DPN process is much better than that from non-DPN processes for the devices with the same EOT (Electrical Oxide Thickness). Based on the

experiments, we propose an extended NBTI model, which incorporates nitrogen concentration in the formula for the process with DPN. This extension provides much clearer direction on process tuning to better control the DPN dosage and the EOT to meet both process electric and reliability requirements.

Numerical Investigation of the Effects of Phosphorus on the Mechanical Responses of [1 1 0]-oriented Silicon Nano-wires

Bin Liu, Junyong Tao, Xun Chen, Yun'An Zhang, Yu Jiang, National University of Defense Technology, China; Yi Qian, Mianyang High-tech Experimental Middle School, China

The mechanism that phosphorus (P) impurities, one of the most commonly used impurities in silicon (Si), affect the tensile mechanical responses of [1 1 0]-Si nano-wires (NWs) is investigated using molecular dynamics (MD) with a Modified Embedded Atom Method (MEAM) potential. Tensile tests at 300K are carried out for unnotched and notched Si NWs. For unnotched cases, P impurities randomly replace Si atoms at specific concentrations. Two patterns are considered for notched models, one undoped and one with doped notch tip. Results show that evenly distributed P impurities introduce an overall decrement in fracture strength of unnotched Si NWs as the concentration increases. The failure manner is that the local defects come into being around P, then rapidly nucleate and propagate, finally lead to fracture. However, for notched models, P can evidently enhance the fracture strength by impeding the cracking and growth of pre-existing cracks. With regard to Si NWs with surface defects exposed to strain, fracture usually starts from surface owing to stress concentration, indicating that P functions more critically on surface, especially near crack tips. Hopefully, this finding can be applied in the reliability design of Si-based NW devices. Moreover, when doped with P or notched on surface, the transition of failure mode for 2nm and 3nm NWs can happen, namely from ductile to brittle.

Failure Rate Calculation Method for High Power Devices in Space Applications at Low Earth Orbit

Erdenebaatar Dashdondog, Harada Shohei, Shiba Yuji, Omura Ichiro, Kyushu Institute of Technology, Japan

This paper discusses the universal calculation method for space proton induced failure rate on high power device. High energetic particles can be the reason of power device failure in both terrestrial and space. T-CAD simulation result gives a threshold charge value for the device destruction which is triggered by energetic proton from space. The amount of threshold charge depends on applied voltage for high power device. The probability of charge generation in silicon due to proton penetration is considered as well. This probability function variation depends on the thickness of device and incident energy of proton which studied before at there. Last consideration on this paper is 3.3 kV PiN diode's single event upset cross section and failure rate which was calculated by proposed method in Low earth orbit environment condition.

Evolution of navigation and simulation tools in failure analysis

Etienne Auvray, Paul Armagnat, STMicroelectronics, France; Morgan Cason, Emanuele Villa, STMicroelectronics, Italy; Michael Bruegel, Synopsys,Germany; Maheshwaran Jothi, Synopsys, Italy

The work presented here is related to the utilization of EDA tools in combination with real time images from analytical equipment in order to improve the efficiency of Failure Analysis. The new developed applications help to better understand the design, as well as to provide capabilities to overlay signal traces in analog and logic domains of the chip, with real time images obtained from fault localization techniques. Thanks to this enhanced design visibility, the FA process can be performed with more efficiency. In this work we put special focus on interrupted scan chains. Results of diagnosis tools (simulation) and backside imaging tools (analytical measurements) are combined in order to provide very accurate results. The subsequently performed, destructive, physical analysis greatly benefits from precise and confirmed fault localization. In addition, we present the advantages of real-time simulation for imaging and probing analysis in term of immediate assessment of the diagnosis results quality. Our flow includes tools to start ATPG and BIST. We use diagnosis software including the latest options to improve the accuracy of localization [1], [14] and [15]. CAD Navigation and schematic view tools are brought up along with graphical drag and drop capability between them. This guides the FA engineers to visualize in significantly less time the result of diagnosis and fault localization simultaneously. Dedicated patterns can be gen–erated to improve the accuracy of diagnosis. We demonstrate applications specialized to analyse in particular failing scan chains in complex SOC and analog IP.

Elemental characterisation of 20nm structures in devices using new SEM-EDS technology

Simon Burgess, Xiaobing Li, Oxdford Instruments NanoAnalysis, United Kingdom; Conor McCarthy, Oxford Instruments NanoScience, United Kingdom

The continuing decrease in structure and defect size in devices has driven many applications away from SEM towards thin sample preparation and TEM investigation. The latest FIB/SEM technology has the capability to image structures down to less than 5nm on a bulk or thin specimen but cannot provide supporting chemical information from EDS. Here we investigate a new more sensitive EDS detector, which for the first time provides chemical information at these high spatial resolutions on the SEM. We outline operating conditions that are suitable to chemically resolve semiconductor structures below 20nm. Based on these results we propose workflows to speed up failure analysis by obtaining the analysis result directly in the FIB/SEM without the need for TEM analysis.

Automatized Failure Analysis of Tungsten Coated TSVs via Scanning Acoustic Microscopy

Eva Grünwald, Jördis Rosc, Renè Hammer, Stefan Defregger, Roland Brunner, Materials Center Forschung GmbH (MCL), Germany; Jochen Kraft, ams AG (AMS), Austria; Peter Czurratis, Matthias Koch, PVA TePla Analytical System GmbH, Germany

In 3D integrated microelectronics, the failure analysis of through silicon vias (TSVs) represents a highly demanding task. In this study, defects in tungsten coated TSVs were analysed using scanning acoustic microscopy (SAM). Here, the focus lay on the realization of an automatized failure detection method towards rapid learning. We showed that by using a transducer of 100 MHz center frequency, established with an acoustical objective (AO), it is possible to detect defects within the TSVs. In order to interpret our analysis, we performed acoustic wave propagation simulations based on the elastodynamic finite integration technique (EFIT). In addition, high resolution X-ray computed tomography (XCT) was performed which corroborated the SAM analysis. In order to go towards automatized defect detection, firstly the commercially available software "WinSAM8" was enhanced to perform scans at defined working distances automatically. Secondly, a pattern recognition algorithm was successfully applied using "Python" to the SAM scans in order to distinguish damaged TSVs from defectfree TSVs. Besides the potential for automatized failure detection in TSVs, the SAM approach exhibits the advantages of fast and non-destructive failure detection, without the need for special preparation of the sample.

Improved Etching Recipe for Exposing Cu Wire allowing Reliable Stitch Pull

Richart Stegink, Orla O'Halloran, NXP Semiconductors, Netherlands; Evan Liu, NXP Semiconductors, Taiwan; Manita Duangsang, NXP Semiconductors, Thailand

The AECQ-006 (Automotive Electronics Council Qualification Requirements for components using Cu wire) requires stitch pull tests on decapsulated Cu wire devices after TMCL and HAST/THB testing. The challenge is to perform decapsulation that exposes the complete interconnect without damaging the wires, leads or bondpads. A new method was developed in NXP to achieve this goal. An existing Cu wire decapsulation recipe was improved to protect the leads by adding Benzotriazole or AgNO3 to the nitric/sulphuric acid mixture.

Thermal design optimization of novel modular power converter assembly enabling higher performance, reliability and availability

Paolo Cova, Nicola Delmonte, University of Parma, Italy; Adane Kassa Solomon, Alberto Castellazzi, University of Nottingham, United Kingdom

An alternative integration scheme for a half-bridge switch using 70 mm thin Si IGBTs and diodes is presented. This flat switch, which is designed for high-frequency application with high power density, exhibits

high strength, high toughness, low parasitic inductance and high thermal conductivity. Such a novel assembly approach is suitable to optimize performance, reliability and availability of the power system in which it is used. The paper focuses on the thermal performance of this assembly at normal and extreme operating conditions, studied by means of FEM thermofluidynamic simulations of the module integrated with connectors and liquid cooler, and thermal measurement performed on an early prototype. Improved solutions are also investigated by the FE model.

Lifetime and Manufacturability of Integrated Power Electronics

Richard Randoll, Germany; Wolfgang Wondrak, Daimler AG, Germany; Andreas Schletz, Fraunhofer IISB, Germany

In case of battery electric cars, market data show a traditional exponential gradient of sales figures, known from other technology transitions. The worldwide installed wind and photovoltaic capacity show also an exponential gradient. Even the power density of power electronics is growing exponentially. Power electronics is a prerequisite to enable the exponential growth of power density. Requirements on power electronic packaging technologies are electric performance, thermal performance and robust design. Due to the lack of bond wires, SMD capacitors can be mounted close to semiconductors, resulting in a minimization of parasitic inductance. Thermally, the packaging technology benefits from heat spreading inside the copper leadframe and thin dielectric layers. It obtains a thermal resistance of 0.5 K/W, and there is potential to further reduce the thermal resistance by alternative dielectric material. The thermal resistance can be further reduced to at least 0.42 K/W by the construction of a double side chip cooling. A robust design can be offered by the combination of a chip copper metallization connecting to copper microvias connecting to the top copper layer, which means no difference in coefficients of thermal expansion. On the bottom side, a silver sinter layer offers a reliable connection between chip and leadframe. This paper describes production process optimizations, thermal optimization possibilities, power cycling lifetime measurements and first conductive anodic filament lifetime measurements at 1000 V DC. The outlook onto an integrated 120 A 700 V SiC MOSFET demonstrator is given.

On the Prediction of Radiation-Induced SETs in Flash-based FPGAs

Sarah Azimi, Luca Sterpone, Politecnico di Torino, Italy

The present work proposes a methodology to predict radiation-induced Single Event Transient (SET) phenomena within the silicon structure of Flash-based FPGA devices. The method is based on a MonteCarlo analysis, which allows to calculate the effective duration and amplitude of the SET once generated by the radiation strike. The method allows to effectively characterize the sensitivity of a circuit against the transient effect phenomenon. Experimental results provide a comparison between different radiation tests data, performed with different Linear Energy Transfer (LET) and the respective sensitiveness of SETs.

Online computation of IGBT on-state resistance for off-shelf three-phase two-level power converter systems

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Power converter systems in most of the applications are operated continuously with dynamically varying and highly inductive loads. The operating environmental conditions of the IGBT modules in such power converter systems is highly dependent on the thermal management. Hence, the operating conditions can be adverse when the system thermal management is not optimal. All this eventually triggers wear out failures in the power modules. The on-state voltage and threshold voltage have been usually considered in the literature to investigate the device degradation in power modules. In this paper, a novel online computation method for the on-state resistance (rCE) of IGBT modules to develop the health monitoring model for power modules in off-shelf power converter system is proposed. The on-state resistance of power module is investigated so that it could be used as a potential precursor to identify aging of devices with solder die degradation as a failure mechanism.

Fault isolation at P/N junction by nanoprober

Wan-Yi Liu, Chih-Feng Chiang, Hui-Jhen Tsai, Chia-Hsiang Yen, Rung-Jiun Lin, Shen-Rong Shih, Te-Fu Chang, Shih-Hsin Chang, Pau-Sheng Kuo, Chih-Hsun Chu, Materials Analysis Technology Inc., Taiwan

Precise location of leakage in a P-WELL/N-WELL junction has been identified by an AFM (atomic force microscope)-based nanoprober. In order to provide the accurate position of the failure for further analysis, a new method was proposed by combining nanoprobing I-V results on each P-well/N-well contact together with semi-empirical calculation to identify the possible leakage path. Further plan view TEM analysis confirms our result.

Effect of H/Ar treatment on ZnO:B transparent conducting oxide for flexible a-Si:H/μc-Si:H photovoltaic modules under damp heat stress

Jae-Seong Jeong, Korea Electronics Technology Institute (KETI), Korea

A flexible amorphous/microcrystalline Si:H (a-Si:H/μc-Si:H) tandem-junction photovoltaic (PV) module was produced in which a thin film of ZnO:B grown by metalorganic chemical vapor deposition (MOCVD) served as the transparent conducting oxide (TCO). The Hall mobility of ZnO:B is degraded by damp heat, simulated here using the conditions of 85°C at 85% relative humidity; this affects the series resistance and efficiency of the PV module. In this study, ZnO:B was treated by H/Ar plasma to reduce the degradation experienced under damp heat. The degradation time of the Hall mobility of ZnO:B, defined as the time necessary for the cell to reach the efficiency loss of -20%, was improved by ~54% by H/Ar treatment (ZnO:B•H/Ar). The mechanism behind this improvement was investigated by assessing the reactions of the ZnO:B and ZnO:B•H/Ar thin films to moisture. Related changes in the physical and chemical properties of ZnO:B and ZnO:B•H/Ar were analyzed by X-ray photoelectron spectroscopy, secondary-ion mass spectroscopy, and ultraviolet photoelectron spectroscopy. The analyses showed that the concentration of OH- was high while those of Zn2+ and B3+ were low in the grain boundaries of the ZnO:B surface after exposure to humidity. After H/Ar treatment, the increase in OH-concentration in ZnO:B was reduced, and the decrease in the Zn2+ and B3+ concentrations was much smaller. The H/Ar plasma treatment of ZnO:B affected the surface reaction forming Zn(OH)2, between the OH- and Zn2+ ions at the grain boundaries under damp heat.

Investigation of Temperature Variations on Analog/RF Linearity Performance of Stacked Gate GEWE-SiNW MOSFET for Improved Device Reliability

Neha Gupta, Ajay Kumar, Rishu Chaujar, Delhi Technological University, India

In this paper, reliability issues of Stacked Gate (SG)-Gate Electrode Workfunction Engineered (GEWE)-Silicon Nanowire (SiNW) MOSFET is examined over a wide range of ambient temperatures (200-600K) and results so obtained are simultaneously compared with conventional SiNW and GEWE-SiNW MOSFET using 3D-technology computer aided design quantum simulation. The results indicate that two temperature compensation points (TCP) are obtained: one for drain current (Ids) and other for cut-off frequency (fT) where device Figure Of Merits (FOMs) become independent of temperature, and it is found at 0.65V in SG-GEWE-SiNW in comparison to other devices, hence will open opportunities for wide range of temperature applications. Furthermore, significant improvement in Analog/RF performance of SG-GWEW-SiNW is observed in terms of Ion/Ioff, Subthreshold Swing (SS), device efficiency, fT, noise conductance and noise figure as temperature reduces. It is also observed that at low temperature SG-GEWE-SiNW unveils highly stable linearity performance owing to reduced distortions. These results explain the improved reliability of SG-GEWE-SiNW at low temperatures over GEWE-SiNW MOSFET.

Improving the short circuit ruggedness of IGBTs

Lukas Tinschert, Josef Lutz, TU Chemnitz, Germany; Magnar Hernes, SINTEF Energy AS, Norway

The demands on reliable and fault tolerant power electronic devices are increasing. One opportunity to increase the IGBT short circuit ruggedness is to modify the thermal capacitance and the thermal resistance close to the chip and hence extend the possible short circuit duration.

Therefore simulations with different metallization, bond wire and chip interconnect materials are compared to identify the most promising solution for enhancing short circuit capability of IGBTs.

Comparison of Thermal Runaway Limits under Different Test Conditions Based on a 4.5 kV IGBT

Paula Diaz Reigosa, Francesco Iannuzzo, Munaf Rahimo, Aalborg University, Denmark; Daniel Prindle, Gontran Pâques, ABB Switzerland Ltd, Semiconductors, Switzerland

This investigation focuses on determining the temperature-dependent leakage current limits which compromise the blocking safe operating area for silicon IGBT technologies. A discussion of a proper characterization method for selecting the maximum rated junction temperature for devices operating at high temperatures is given by comparing the different testing methods: Static performance (including and excluding self-heating effects), Short Circuit Safe Operating area and High-Temperature Reverse Bias. Additionally, a thermal model is used to predict the junction temperature at which thermal runaway takes place. In this paper guidelines are proposed based on the correlation among short circuit withstand capability and off-state leakage current for guarantying reliable operation and ensuring that they are thermally stable under parameter variations. This study is helpful to facilitate application engineers for defining the correct stability criteria and/or margins in respect of thermal runaway.

Body diode reliability investigation of SiC power MOSFETs

Asad Fayyaz, Alberto Castellazzi, University of Nottingham, United Kingdom; Gianpaolo Romano, University of Naples Federico II, Italy

A special feature of vertical power MOSFETs, in general, is the inbuilt body diode which could eliminate the need of having to use additional anti-parallel diodes for current freewheeling in industrial inverter applications: this, clearly, subject to their demonstration of an acceptable level of reliability. Recent improvements in Silicon Carbide (SiC) power MOSFET device manufacturing technology has resulted in their wider commercial availability with different voltage and current ratings and from various manufacturers. Hence, it is essential to perform characterisation of its intrinsic body diode. This paper presents the reliability assessment of body diodes of latest generation discrete SiC power MOSFETs within a 3-phase 2-level DC-to-AC inverter representing realistic operating conditions for power electronic applications.

Evaluation of Potential-Induced Degradation in Crystalline Si Solar Cells using Na-Fault Injection

Wonwook Oh, Junhee Kim, Byungjun Kang, Sung-Il Chan, Korea Electronics Technology Institute, Korea; Soohyun Bae, Kyung Dong Lee, Hae-Seok Lee, Donghwan Kim, Korea University, Korea

Photovoltaic (PV) modules are exposed to high-voltage stress between grounded module frames and solar cells, a configuration called potential-induced degradation (PID). Since PID mainly depends on the solar cells used for module packaging, several steps for PID tests can be omitted. We carried out PID tests on the cell level with Na fault injection in accordance with IEC 62804 and examined the extent of PID with saturation current density (J02) extracted from I-V measurements in the dark. Na-fault injection is a reasonable means for performing PID tests on the cell level without module packaging.

Session 9A: Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories - Part 2

A run-time built-in approach of TID test in SRAM based FPGAs

Ning Ma, Shaojun Wang, Yu Peng, Harbin Institute of Technology, China

Run-time TID test in SRAM based FPGAs can improve reliability in space applications, but none feasible approach has been presented. This paper proposes a lightweight built-in test approach, in which the propagation delay of combinational logic in FPGA is measured with ring oscillator in runtime. The differences between propagation delays in different time slots are provided as the metric of TID degradation. The irradiation experiments on Xilinx Zynq chip prove the validity of the proposed method.

Reliability analysis of hybrid Spin Transfer Torque Magnetic Tunnel Junction/CMOS Majority Voters

Mariem Slimani, Lirida Naviner, Telecom ParisTech, France; Paulo Butzen, Federal University of Rio Grande, Brazil

Majority voters are typically used in redundancy hardening techniques aiming to increase the reliability of nanoscale circuits. Besides, Spin Transfer Torque Magnetic Tunnel Junction (STT-MJT) has been identified as the most promising candidate for low power and high speed applications. In this paper, we present two majority voter circuits based on nanometer STT-MTJ. By using STMicroelectronics FDSOI 28nm process and a precise STT-MTJ compact model, electrical simulations have been carried out to compare their performances and analyze their reliability. Both radiation sensitivity and variability have been investigated in the reliability-aware analysis.

Application of the Defect Clustering Model for Forming, SET and RESET Statistics in RRAM Devices

Nagarajan Raghavan, Singapore University of Technology and Design, Singapore

The choice of the right statistical model to describe the distribution of switching parameters (forming, SET and RESET voltages) is a critical requirement for RRAM, as it is used to analyze the worst case scenarios of operation that have to be accounted for while designing the cross-bar array structures, so as to ensure a robust design of the circuit and reliable data storage unit. Several models have been proposed in the recent past to characterize the voltage variations in VFORM, VSET and VRESET using the percolation framework. However, most of these models assume defect generation to be a Poisson process and apply the standard Weibull distribution for parameter extraction and lifetime extrapolation. Recent dielectric breakdown studies both at the front-end as well as back-end have shown that the Weibull statistics does not describe the stochastic trends well enough, more so in downscaled structures at the low and high percentile regions given the possibility of defect clustering which is either physics-driven or process quality-driven. This phenomenon of defect clustering is even more applicable in the context of resistive random access memory (RRAM) devices, as switching occurs repeatedly at ruptured filament locations where defect clusters pre-exist. This study examines the validity of the clustering model for RRAM switching parameter statistics (time / voltage to FORM, SET and RESET) and presents a physical picture to explain the origin of clustering in RRAM. A large set of data from various published studies has been used here to test the suitability and need for aclustering model based reliability assessment. Dependence of the clustering factor on temperature, voltage, device area, dielectric microstructure and resistance state has been examined.

Resistive RAM Variability Monitoring using a Ring Oscillator based Test Chip

Hassen Aziza, Jean-Michel Portal, Aix-Marseille Université, France

Common problems with Oxide-based Resistive Random Access Memory (so-called OxRRAM) are related to high variability in operating conditions and low yield. Although research has taken steps to resolve these issues, variability remains an important characteristic for OxRRAMs. In this paper, a test structure consisting of an OxRRAM matrix where each memory cell can be configured as a ring oscillator is introduced. The oscillation frequency of each memory cell is function of the cell resistance. Thus, the test structure provides within-die accurate information regarding OxRRAM cells variability. The test structure can be used as a powerful tool for process variability monitoring during a new process technology introduction but also for marginal cells detection during process maturity.

Permanent and Single Event Transient Faults Reliability Evaluation EDA tool

Ygor Quadros de Aguiar, Cristina Meinhardt, Universidade Federal do Rio Grande, Brazil; Alexandra Zimpeck, Ricardo Reis, Universidade Federal do Rio Grande do Sul, Brazil

In nanotechnology domain, reliability is a fundamental concern in the design and manufacturing process of VLSI circuits. Thus, this paper pres-

ents a tool developed to evaluate the reliability of logic cells in order to provide a set of information to improve design robustness. The tool is able to evaluate logic cells under Single Event Transient (SET) faults and, also, permanent faults such as Stuck-On (SOnF) and Stuck-Open (SOF). The information produced by this tool help designers to choose the most reliable cells to be adopted in their designs.

Session 9B: Power Devices Reliability: Passives

200V FRED diode with superior ESD capability

Andrea Irace, Luca Maresca, Paolo Mirone, Michele Riccio, Giovanni Breglio, University of Naples - Federico II, Italy; Laura Bellemo, Rossano Carta, Marco Naretto, Nabil El Baradai, Vishay Semiconductor Italiana, Italy; Isabella Para, Natale Di Santo, Politecnico di Torino, Italy

In this paper the Electrostatic Discharge (ESD) capability of 200 V Fast Recovery Epitaxial Diodes (FREDs) is analysed by means of suitable experiments, TCAD simulations and theoretical analyses. Different doping profiles are investigated in order to improve the ESD robustness of a standard device and an optimized doping profile is proposed. The newly fabricated devices show a remarkably high ESD capability without any significative loss in forward voltage drop and a reduction of the breakdown voltage that does not affect device rating.

Charging–discharging characteristics of a wound aluminum polymer capacitor

Ui Hyo Jeong, Jae Phil Hyung, Yang Gi Yoon, Min Ji Ko, Hong Woo Lim, Korea Testing Certification, Korea; Seok Geun Ha, Enesol Co. Ltd, Korea; Dong Hyuk Lee, LG Display Co. Ltd, Korea; Jang Joong Soon, Ajou University, Korea

This study characterized aluminum polymer capacitors, especially when they are charging and discharging. Tests were conducted under various conditions. The following environments were considered: three hightemperature conditions, two high temperature/high humidity conditions, and room temperature. Various operating conditions were also considered, such as charging–discharging, operating, and storage. The test results showed that the capacitance of the wound polymer aluminum capacitor degraded with charging–discharging at low temperature. At lower temperatures, this characteristic accelerated but was mitigated with a dry electrolyte. The degraded capacitances partially recovered when the capacitors were stored at a high temperature. These characteristics were not observed for a conventional liquid aluminum capacitor. This unreported special characteristic of polymer aluminum capacitors should be considered when designing systems such as power electronics. Polymer capacitors are known for their high reliability, especially at high temperatures. At low temperatures, however, the charging–discharging characteristic should be carefully considered. This paper reports on this characteristic of polymer capacitors for consideration by industries.

Session 9C: EFUG - Workshop (Part 1)

Ga contamination in silicon by focused ion beam milling: Atom Probe Tomography and simulation with dynamic model

Jin Huang, Markus Loeffler, TU Dresden, Germany; Wolfhard Moeller, HZDR, Germany; Ehrenfried Zschech, Fraunhofer IKTS, Germany

Focused ion beam (FIB) milling is a widely used and important technique to prepare Transmission Electron Microscopy (TEM) lamella samples. However, it unavoidably introduces contamination on the samples, typically by Ga ions implantation. This study presents an Atom Probe Tomography (APT) analysis together with a computer simulation based on a dynamic Binary Collision Approximation (BCA) model to predict such contamination on silicon samples. Conventional BCA models like SRIM is useful to predict ion implantation on the substrate. But it is not able to describe situation like FIB milling, where significant material transport happens. In this study, a dynamic BCA model is used to describe FIB milling and the simulated Ga contamination results are discussed jointly with APT experiment results. The strong agreement between the two shows the dynamic BCA model is applicable to predict FIB induced Ga ion contamination on silicon samples.

Micro mechanical robustness tests of 28nm BEOL layer stack

Eckhard Langer

In order to evaluate the mechanical robustness of 28nm BEOL on the µm-scale, two non-standard mechanical test methods were used and will be presented in the talk. First an in situ micro pillar bending test and second a cross sectional nanindentation method. These applications will demonstrate their value for finding appropriate integration schemes for improved robustness.

Laser based sample preparation for advanced packaging applications

Thomas Höche and Michael Krause

3D integration in microelectronics has been generating the need for new, massive ablation techniques of sample preparation. This challenge is addressed with microPREPTM, Gatan's all-new, laser-based preparation tool. Using an ultrashort pulsed laser, synchronized hardware, and a dedicated laser micromachining scheme, large-area, smooth, vertical flanks are prepared. Two workflows will be discussed, complementing the laser cutting either by broad ion-beam or FIB polishing. While the former facilitates the preparation of hundreds of TSV's within less than two hours, the latter workflow is more surgical in character.

Planar FIB Milling of Copper by using the Novel Rocking Stage Technology

Sharang Sharang

Copper has found immense applications within the semiconductor industry. In order to make site-specific alterations using focused ion beam (FIB) at nanoscale levels, it is imperative we manage to operate on polycrystalline copper directly with no need for an extensive grain size and orientation study prior to performing FIB milling operations. Homogenous copper FIB milling arises from the need to perform various circuit edit operations below the dielectric layer following the copper layer. If the layer beneath the dielectric is affected by inhomogeneous milling, it can lead to short-circuit and eventual device breakdown [1-2]. Failure analysis on an integrated circuit was performed using rocking stage with 6-axes piezo movement capabilities together with the novel approach of the combined Xe-plasma ion source FIB and SEM system (XEIA) [3-5]. Site-specific milling of copper with different milling strategies were tested to optimize time and homogeneity of the milling across the target surface and to overcome the channelling effect posed by polycrystalline copper. Only during the last few nanometres of copper layer the water vapour is used to protect the dielectric layer. The complete removal of copper was followed with XeF2 assisted milling of the dielectric layer to observe the unharmed circuitry [6]. Channelling effect was reduced by regulating the sputtering rates across different grains keeping the underlying dielectric layer safe. High-resolution scanning electron microscopy (HR-SEM) imaging was used for constant monitoring of the removed material to help modulate the process for highest throughput in the least possible amount of time.

Fast, Reliable, Intuitive TEM Sample Preparation using a Load-Lockable Platform Combined with Smart Control Software

Stephan Kleindiek, Andreas Rummel and Matthias Kemmler

Session 11A: Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Space and Radiation

Natural Radiation Events in CCD Imagers at Ground Level

Tarek Saad Saoud, Soilihi Moindjie, Daniela Munteanu, Jean-Luc Autran, Aix-Marseille University, France

In Charged Coupled Devices (CCDs), radiation-induced events generate electron hole pairs in silicon that cause artifacts and contribute to degrade

image quality. In this work, the impact of natural radiation at ground level has been characterized at sea level, in altitude and underground for a commercial full-frame CCD device. Results have been carefully analyzed in terms of event shape, size and hourly rates. The respective contributions of atmospheric radiation and telluric contamination from ultra-traces of alpha-particle emitters have been successfully separated and quantified. Experimental results have been compared with simulation results obtained from a dedicated radiation transport and interaction code.

Single Event Transient Acquisition And Mapping For Space Device Characterization

Roberta Pilia, Giovanna Mura, University of Cagliari, Italy; Guillaume Bascuil, Fulvio Infante, Intraspec Technologies, France; Kevin Sancez, CNES, France

It is necessary for space applications to evaluate the sensitivity of electronic devices to radiations. It was demonstrated that radiations can cause different types of effects to the devices and possibly damage them [1][2]. The interest in the effect of Single Event Transient (SET) has recently risen because of the increased ability of parasitic signals to propagate through advanced circuit with gate lengths shorter than 0.65 nm and to reach memory elements (in this case they become Single Event Upset (SEUs)). Analog devices are especially susceptible to perturbations by such events which can induce severe consequences, from simple artifacts up to the permanent fail of the device. This kinds of phenomena are very difficult to detect and to acquire, because they are not periodical. Furthermore, they can vary a lot depending on different parameters such as device technology and biasing. The main obstacle for the analysis is due to the maximum frequency of these signals, which is unknown. It is consequently difficult to set a correct sample frequency for the acquisition system. In this document a methodology to evaluate SETs in analog devices is presented. This method allows to acquire automatically these events and to easily study the sensitivity of the device by analyzing a “SETs cartography”. The advantages are different: it allows to easily acquire and analyze the SETs in an automatic way; the obtained results allow the user to accurately characterize the device under test; and, finally, the costs due to the implementation of the tests are lower than a classical analysis performed by a particle accelerator.

Session 11B: Power Devices Reliability: Testing Methods

Topologies for inverter like operation of power cycling tests

Christian Herold, Peter Seidel, Josef Lutz, TU-Chemnitz, Germany; Reinhold Bayerer, Infineon Technologies AG, Germany

In standard power cycling devices are always in on-state and heated solely by conduction losses. Contrary the devices in application are heated also by switching losses, which rise with temperature increase. Degradation of interconnects causing higher temperature swings might be thereby accelerated stronger than in standard tests. This paper discusses test bench topologies implemented to overcome this gap.

End of life and acceleration modelling for power diodes under High Temperature Reverse Bias stress

Oliver Schilling, Klaus Leitner, Karl-Dietger Schulze Frank Umbach, Infineon AG, Germany

This work is motivated by the growing importance of lifetime modelling in power electronics. Strongly accelerated High Temperature Reverse Bias (HTRB) testing of power diodes at different stress conditions is performed until alterations and fatigue mechanisms become evident. Two categories of effects can be separated: Drifting breakdown voltage and hard failures with complete loss of blocking capability. Nevertheless the overall stress duration needed to provoke destructive failures is very high with test durations >2500h even at almost 230°C and 100% rated voltage. For both mechanisms the temperature and voltage acceleration is evaluated. Especially temperature acceleration is significant in the regime of testing between 200°C and 230°C and an activation energy Ea in the regime >1eV can be deduced which is higher compared to values commonly reported in the literature. Failure analysis shows that both package and also chip related effects could contribute to the observed hard failures in HTRB stress under extreme conditions.

Internal processes in power semiconductors at virtual junction temperature measurement

Weinan Chen, Jörg Franke, Christian Herold, Riteshkumar Bhojani Josef Lutz, Technische Universität Chemnitz, Germany

High measurement accuracy is the basis for a precise determination of the junction temperature Tj. Temperature measurement can be performed by means of temperature sensitive parameters (TSP) as shown in [1] using the VCE(T)-method, however, internal semiconductor processes like the removal of stored charge in bipolar devices have to be respected. The aim of this work is to determine the earliest time point of accurate measurement tMD after switching off, as well as dependencies on device voltage classes and applied battery voltage. Measurement results are confirmed by performing the simulation with Sentaurus TCAD. Dependencies of delay tMD on temperature, applied measurement current and battery voltage are demonstrated for IGBT and silicon diode.

Session 11C: EFUG - Workshop (Part 2)

3D Inspection Solutions for 3D Devices

Ingo Schulmeyer, Lorenz Lechner, Raj Jammy, Allen Gu, Raleigh Estrada, Diane Stewart, Lewis Stern, Shawn McVey, Bernhard Goetze and Ulrich Mantz, Carl Zeiss Microscopy (DE)

Semiconductor devices and packages have firmly moved in to an era where scaling is driven by 3D architectures. However, most of the metrology and inspection technologies in use today were developed for 2D devices and are inadequate to deal with 3D structures. An additional complication is the need for specific structural and defect information that may be buried deep within a 3D structure. We present concepts and technologies that allow for 3D imaging as well as tomography, enabling engineers to view structural information with unprecedented clarity, detail and speed. The discussed methods include FIB and X-Ray Microscopy and show the abilities of these technologies for the analysis of electronic devices.

Innovative TEM sample Preparation on Helios G4 platform

Ladin Trevan and David Donnet

Advanced TEM sample preparation is required for the failure analysis and process control of bleeding edge technology nodes. Ultra-thin lamella with minimal amorphous damage can be made using the Phoenix ion column of the Helios G4 dualbeam microscope, permitting projection free imaging of even the smallest features. Front-end defects are increasingly difficult to locate for root cause analysis in the TEM, especially for 3D transistor structures. A sample preparation method is described in which a planar view sample of the region of interest is initially made and observed in STEM to more accurately locate the failing region. Subsequently a cross sectional lamella is prepared from the plan-view. In the Helios G4, all of these steps can be performed without taking the sample out of the chamber or physical handling, thus leading to a faster and more robust workflow.

FIB and P-FIB assisted sample preparation for in-situ TEM characterization

Remy Berthier

Session 12A: Semiconductor Reliability & Failure Mechanisms: FD-SOI and RRAM

Device to circuit reliability correlations for Metal Gate / High-k transistors in scaled CMOS technologies (invited)

Andreas Kerber, GLOBALFOUNDRIES Inc., USA

Metal Gate / High-k stacks are in CMOS manufacturing since the 45nm technology node. To meet technology performance and yield targets gate stack reliability is constantly being challenged. Assessing the associated reliability risk for CMOS products relies on a solid understanding of device to circuit reliability correlations. In this paper we summarize our findings

on the correlation between device reliability and circuit degradation and highlight areas for future work to focus on.

FDSOI and Bulk CMOS SRAM Cells Resilience to Radiation Effects

Walter Enrique Calienes Bartra, Ricardo Reis, Universidade Federal do Rio Grande do Sul, Brazil; Andrei Vladimirescu, ISEP, France

With shrinking dimensions and increased number of on-chip transistors radiation can provoke faults in integrated circuits even at sea level. This paper presents a comparison of Fully Depleted SOI (FDSOI) and Bulk CMOS 6T SRAM Cells' Resilience to Radiation Effects. Both cells were simulated using TCAD tools, considering heavy-ion impacts in different locations of the transistor as well as using different impact angles. Two types of radiation effects have been considered: Single-Event Transients (SETs) and Single-Event Upsets (SEUs). The minimum critical collected charge (CC) to flip a cell is almost the same in both technologies. However, it is shown that a FDSOI SRAM cell needs a heavy-ion impact with a Linear Energy Transfer (LET) around 10 times greater than a Bulk-CMOS SRAM cell, to generate a similar CC and to flip a cell.

Performance vs. Reliability Adaptive Body Bias Scheme in 28nm & 14nm UTBB FDSOI nodes

Cheikh Ndiaye, Vincent Huard, Xavier Federspiel, STMicroelectronics, France

This paper shows the advantages of using body bias. Experiments are performed in 14 nm and 28nm UTBB FDSOI transistors and ring oscillators (ROs). The impact of body bias on performance and reliability are highlighted. The body biasing offers significant advantages for adapting the tradeoff between reliability and performance in logic circuits without changing the design margins. With FDSOI technology, we have an additional degree of freedom of process variability compensation by using body bias voltage (Adaptive Body Bias, ABB) next to supply voltage compensation used before. We show that ABB compensation technique presents better results for a complete power optimization.

Potentiality of Healing Techniques in Hot-Carrier Damaged 28nm FDSOI CMOS nodes

Alain Bravaix, ISEN-IM2NP, France; Florian Cacho, Xavier Federspiel, Cheikh Ndiaye, Souhir Mhira, Vincent Huard, ST Microelectronics, France

We have developed the possibility of using healing phases on hot-carrier (HC) degraded transistors from devices to logic cells (1) by the combined effects of oxide charge neutralization and channel shortening (2) using back bias VB sensing effects in forward (FBB) mode in 28nm FDSOI CMOS node. This is done for DC to AC operations from Input-Ouput device (EOT= 3.6nm) to core blocks (EOT= 1.35nm) leading to an almost complete cure of HC damaged devices for digital application. Continuous or short sequences of healing phases help to regenerate HC degraded parameters (IOn, VT) offering new perspectives for on time repeatedly cure digital operation as well as under some analog case.

Electromagnetic susceptibility characterization of double SOI device

Binhong Li, Jianfei Wu, Xing Zhao Jiantou Gao, Chuang Gao and Jiajun Luo, Institute of Microelectronics of Chinese Academy of Sciences, China; Kai Zhao, Fudan Mictroelectronics Group, China; Jianwei Su, Tianjin Binhai Civil-military Integrated Innovation Institute, China

Under a research project of monolithic pixel detectors, a double silicon on insulator (DSOI) structure was introduced based on fully depleted SOI (FDSOI) technology. It not merely integrates the sensor and readout circuit on the same processed wafer, but also increases radiation tolerance. Electromagnetic susceptibility (EMS) is also an important reliability issue in pixel detectors. The readout circuit should avoid false signal generation due to coupled noise from the substrate. This paper evaluates the performance of DSOI devices regarding total ionizing dose (TID) effect compensation in transistors by applying a negative bias to the middle silicon layer, and evaluates the electromagnetic susceptibility of the substrate by a ring oscillator. The experiment results show that the DSOI device is able to compensate for TID, and the threshold voltage and leakage current are recoverable. However, the reduction of TID effect on the DSOI device is at the expense of increasing susceptibility to electromagnetic interference (EMI) on the substrate.

Analysis of Quantum Conductance, Read Disturb and Switching Statistics in HfO2 RRAM Using Conductive AFM

Alok Ranjan, Nagarajan Raghavan, Shubhakar Kalya, Kin Leong Pey, Singapore University of Technology and Design, Singapore; Joel Molina, National Institute of Astrophysics, Optics and Electronics, Mexico; Sean O'Shea, Institute of Materials Research and Engineering, Singapore

Most studies on resistance switching have been carried out at the device level with the standard electrical characterization setup, which allows for effective automated reliability test and extensive characterization of the lifetime of an RRAM device. However, it is equally important to be able to probe the switching phenomenon at the nanoscale so as to improve insight on the bias-dependent kinetic behavior of the filament during multiple reversible breakdown and recovery cycles. This study aims to do just that by probing HfO2 blanket films (~4 nm) with a W bottom electrode using an ultra-sharp Ptwire conductive-AFM (CAFM) tip with an areal resolution of 10-20 nm at ambient conditions. The use of the CAFM allows for a more reliable assessment of single filament evolution behavior as possible multiple filamentation events (common at the device level) are rare for such small probing areas. The role of oxygen vacancy induced filaments is studied here by using low compliance setting and moderate voltage levels, ensuring operation in the sub-quantum conductance regime. Our results show good repeatable switching trends and also provide insight on the quantum conductance phenomenon in oxygen vacancy based filaments. The read disturb trends in switching are investigated for the high resistance state (HRS) and the impact of tip-induced mechanical stresses on forming lifetime is also presented, which could serve as a motivator for further studies on non-volatile memory (NVM) reliability for flexible electronics devices and system on chip (SoC) applications.

Session 12B: Failure mechanisms and precautions in plug connectors and relays: Tutorial

Failure mechanisms and precautions in plug connectors and relays (Tutorial)

Peter Jacob, EMPA Swiss Fed Labs for Materials Testing and Research, Switzerland

Plug connectors are one of the frequent failure causes when regarding at electronic systems. Since connectors had to keep pace with ongoing miniaturization on PCB level, current and voltage capabilities and specifications are frequently sportive or even overestimated. The tutorial focuses on the interfaces between connector and PCB as well as on connector-to cable and the connector contact itself, showing various failure mechanisms and precautions. Environmental conditions may also severely impact the connector reliability. The tutorial sensitizes the failure analyst to this underestimated topic and offers a deeper understanding and precaution measures against connector-related failures. Since many aspects considering plug connectors also apply for relays, the most important relay failure aspects are included in a small chapter of this tutorial.

Session 13: EUFANET/CAM-Workshop "Automotive Electronics Systems Reliability" (Part 1)

Georgia Tech's automotive electronics ecosystem

Klaus-Juergen Wolter, Georgia Tech (US)

The southeast United States continues to develop the fastest growing automotive industry in North America. Known for its world-class automotive production and excellent business environment, the region's supply-base has grown while OEMs and major suppliers continue to invest. Georgia Tech as the number one ranked engineering university in southeast cooperates with many automotive companies in southeast. Georgia Tech automotive industry partners include BMW, GM and Ford, to date. Additional R&D collaborations are underway with Mercedes Benz, Ferrari, Honda, VW and Toyota in many areas that include hybrid vehicle R&D, internal component design, communication-vehicle interactions,

automated driving, driver-assist, human-robot interactions and in environmental impacts.

77Ghz Automotive RADAR in eWLB package: from consumer to automotive packaging
Gerhard Haubner and Walter Hartner, Infineon Technologies AG, Germany

ADAR technology as sensor for collision warning has been used in upper class vehicles for some years now. Assembling this electronic is highly sophisticated and therefore expensive. With new developments in SiGe-technology and semiconductor packaging RADAR technology is now available much smaller and cheaper. It is therefore affordable for mass-market in Advanced Driver Assistance Systems (ADAS) – which means "safety for everyone". This paper emphasizes the evolution from a consumer electronic package to an automotive package enduring the requirements relating to quality and reliability in these applications. Using 2nd level interconnect reliability as an example, we show the systematic approach utilizing "Design for Reliability" to enhance system properties. Particularly, the package board interaction and the solder joint performance regarding temperature cycling is discussed in matters of board material and build-up.

Reliability of automotive LED systems
Wolfgang Pohlmann and Stephan Böckhorst, Hella KGaA Hueck & Co, Germany

In the last years, many new intelligent headlamp and rear lamp technologies based on semiconductor light sources (LEDs) were developt in order to reduce the traffic accident rates on different road topologies and situations, to improve night time driving comfort and to get better sight conditions. The resulting new intelligent automotive lighting technologies are able to adapt their lighting distributions and luminous intensity on and beside the road in dependence on the traffic density, weather or car speed.

The lecture therefore deals with system development and system reliability of these innovative lighting systems in automotive lighting. First new lighting systems in LED technology are presented. The design of both the LEDs required for this purpose and the PCB technologies applied has a significant impact on LED solder joint reliability, on optimized low position tolerance of the LED component by, component self-alignment mechanism. It also has a key role to play in the system reliability of LED modules. In addition the latest miniaturized LED housing developments – featuring remodeled designs and new materials – are turning the focus toward the thermal management of LED modules, tolerance characteristics, and the entire LED-module production process. This report concludes with an outlook for new high resolution light sources systems for automotive lighting.

Session 14: Reliability and Failure Mechanisms of special photonics and LED Devices: LED systems

LED Degradation: from component to system (invited)
Willem van Driel, B. Hamon, Philips Lighting, Netherlands

Human civilization revolves around artificial light. Since its earliest incarnation as firelight to its most recent as electric light, artificial light is at the core of our existence. It has freed us from the temporal and spatial constraints of daylight by allowing us to function equally well night and day, indoors and outdoors. It evolved from open fire, candles, carbon arc lamp, incandescent lamp, fluorescent lamp to what is now on our door step: solid state lighting (SSL). SSL refers to a type of lighting that uses semiconductor light-emitting diodes (LEDs), organic or polymer light-emitting diodes (OLED / PLED) as sources of illumination rather than electrical filaments, plasma (used in arc lamps such as fluorescent lamps), or gas. SSL applications are now at the doorstep of massive market entry into our offices and homes. This penetration is mainly due to the promise of an increased reliability with an energy saving opportunity: a low cost reliable solution. An SSL system is composed of a LED engine with a micro-electronics driver(s), integrated in a housing that also provides the optical, sensing and other functions. Knowledge of (system) reliability is crucial for not only the business success of the future SSL applications, but also solving many associated scientific challenges. In practice, a malfunction of the system might be induced by the failure and/or degradation of the subsystems/interfaces. This paper will address the items to ensure high reliability of SSL systems by describing LED degradation from a component and a system perspective.

Transient thermal testing for quality control of electronic devices
Dominik Müller, Gordon Elger, Technische Hochschule Ingolstadt, Germany

Reliability of LED light sources is essential for many general and automotive lighting application where exchange of LED modules would be expensive. Reliability testing to predict the life-time of the devices is required. In this paper transient thermal testing is applied and further developed to monitor the structural integrity of the LED modules during accelerated stress testing. The temperature shock test is one important test because thermomechanical stress is a dominating root cause for structural failures as delamination in the package or cracking of solder joints between package and board. New flip chip LEDs (WLP-LEDs) are assembled directly on printed circuit boards (PCB). The initial assembly quality is tested using X-Ray, optical inspection and transient thermal analysis (TTA). In combination the methods deliver essential data to ensure initial assembly quality. Afterwards, the LED modules are exposed to temperature shock tests (-40°C to 125°C) and the TTA is performed repeatedly. By TTA the structural integrity is resolved and cracks or delamination can be identified. Failure modes can be separated and the root cause is investigated by support of transient finite element analysis. One test board is measured In-situ during temperature shock testing. Due to differences in thermo-mechanical stress under hot and cold conditions additional information can be obtained.

Session 15: Panel Discussion + Keynote 3

Power and industry electronics – future perspectives for Europe (tentative)
Sabine Herlitschka

The European Union has identified Micro- and Nanoelectronics as one of the key enabling technology of our times. Specific program lines were initiated in order to support research and development activities throughout the entire value chain. "Pilot Line" projects are intended to close the gap between research and commercial availability of technologies for customers. Infineon Technologies with its core competencies in power and industry electronics, together with its partners in academia and industry uses these programmes actively to enable new technologies contributing to providing solutions to societal challenges such as energy efficiency, mobility and security. The presentation will give an overview on respective strategies and activities contributing to a strong knowledge-based Europe in the global competition

Session 16A: Failure mechanisms and precautions in plug connectors and relays: Tutorial

Degradation and Recovery of variability due to BTI
Christian Schlünder, Fabian Proebster, Hans Reisinger, Wolfgang Gustin, Andreas Martin, Infineon Technologies AG, Germany

BTI parameter degradation of MOSFETs shows a statistical variation. The distribution of the threshold voltage Vth after NBTI stress originates from a convolution of the distribution of the virgin devices together with the additional distribution of the BTI degradation itself. The variability of the Vth (and other electrical parameters) of the virgin devices bases on process induced fluctuations of dopant atoms, oxide thickness, channel length, etc [1]. The dependence on the transistor size is proven by several publications [e.g. 2,3]. The variability of the BTI parameter degradation itself and the convolution are not fully understood yet and need further investigation. The impact of the recovery behavior on the distribution of the Vth - values is, to our knowledge, not yet studied at all. In this paper we investigate the increase (degradation) of variability due to NBTI and the

statistical behavior of Vth after end of stress (recovery). Furthermore we analyze the dependency of the additional variability of Vth on the transistor size and geometry. For the necessary statistical relevance we perform long term NBTI experiments with a special smart array test-structure at a large amount of pMOSFETs with various geometries. We prove our results for a second technology node with a different oxide thickness. We demonstrate for the first time that also the induced additional variability recovers. Furthermore we show that the variability of pMOSFETs after NBTI depends not only on the size of the active area (w×l) but also on its geometry (w/l).

Early Detection and Prediction of HKMG SRAM HTOL Performance by WLR PBTI Tests

Kary Chien, Atman Zhao, Yueqin Zhu, Wei-Ting Chien, SMIC, China

With technologies scaling down to 28nm and below, and HKMG (High-κ Metal Gate) process being introduced, the NMOS PBTI (Positive Bias Temperature Instability) becomes a reliability concern due to the higher pre-existing trap density in the HfO2 film. These traps can lead to electron trapping and device parameters shifts. Degradation of Vccmin read is a dominant factor in SRAM Vccmin degradations, and PD (Pull Down) NMOS PBTI degradation dominates the Vccmin read degradation, especially at HKMG development phase because of the un-optimized HK dielectric process. This paper provides a feasible methodology to evaluate chip level HTOL (High Temperature Operation Life) performance based on device level PBTI test by studying a correlation relationship between device Vt degradation in WLR (Wafer-Level Reliability) NMOS PBTI stressed tests and SRAM Vccmin degradation in HTOL tests. The proven correlation model allows characterization of Vccmin shifts in SRAM HTOL through WLR PBTI tests at HKMG development, and therefore has significant impacts in promoting reliability test efficiency and reduces development times.

Session 16B: Failure mechanisms and precautions in plug connectors and relays: Tutorial

Automotive Memory Trends and System Reliability Concepts

Reinhard Weigl, Micron Semiconductor GmbH, Germany

In this presentation, current trends and requirements for memories in different automotive applications will be discussed. We see an increasing demand for high density and high performance memory subsystems. These requirements are driven from high-quality video demands within the infotainment segment but as well from an increasing number of sensors to support the ADAS applications leading into an autonomous driving car. More and more connected cars and related networking communication traffic further increases the performance requirements and additionally asks for a secure memory subsystem. However all those innovative systems and features have to meet the strict reliability requirements of the automotive industry. This requires an involvement and a close collaboration at a much earlier point in time within the supply chain. Based on a new level of cooperation we developed a concept that allows investigating the functionality and reliability of new memory subsystems and solutions on system level already during the product design stage.

Powertrain electronics reliability

Mihai Nica, AVL Deutschland GmbH, Germany

Requirements for Reliability and new Solutions for Transmission Control Units

Michael Novak, Wolfgang Grübl, Bernhard Schuch, Continental, Germany

A general trend in automotive electronics is the development of customized products with the focus on system integration in combination with increased reliability and lower costs. For transmission control units (TCUs) of Continental this means: extended functionalities have to be integrated in a minimum of available space. At the same time, the TCU has to operate in an harsh environment with increasing temperature, high vibration loads and most aggressive transmission fluids. As a result of these extreme requirements, the development of new TCU solutions and high performance materials is necessary to guarantee a reliable operation over lifetime.

Cu-wire Bond Reliability in Automotive Electronics

Rene Rongen, NXP Semiconductors, Netherlands

During the past decade Cu-wire bonding has been gradually industrialized. Meanwhile, it has become a mature technology in standard commercial electronics. This presentation explains what is needed for a flawless introduction into automotive electronics. First of all, a comprehensive overview will be given on Cu-wire specific failure mechanisms including the current status on what is known on the Physics-of-Fail. Based on this fundamental knowledge, it will be shown that in-line wire bond responses, if correctly interpreted and used, can both safeguard against early life PPM fails as well as guarantee reliability robustness with respect to wear out failure mechanisms.

Session 16C: Failure mechanisms and precautions in plug connectors and relays: Tutorial

Experimental observation of TDDB-like behavior in reverse-biased green InGaN LEDs

Matteo Buffolo, Matteo Meneghini, Carlo De Santi, Henry Felber, Gaudenzio Meneghesso, Enrico Zanoni, University of Padova, Italy

This paper reports the outcome of a series of reverse-bias experiments performed on commercial GaN-based green LEDs. The experimental results showed that green LEDs submitted to reverse bias i) show a time-dependent failure when they are submitted to constant (reverse) voltage stress, at a bias point smaller than the BDV; ii) experience an increase of the reverse-bias electro-luminescence signal, well-correlated with the increase of the reverse leakage current; iii) the TTF (Time-To-Failure) related to the time-dependent breakdown process has an exponential dependence on stress voltage; iv) the TTF is Weibull distributed. This work provides the first experimental demonstration of time-dependent failure of GaN LEDs.

Degradation of InGaN-based LEDs related to charge diffusion and build-up

Marco La Grassa, Matteo Meneghini, Carlo De Santi, Enrico Zanoni, Gaudenzio Meneghesso, University of Padova, Italy

The aim of this paper is to contribute to the understanding of the impact of charge/impurity instabilities on the optical degradation of InGaN LEDs. We demonstrate a correlation between the optical degradation and the accumulation of charge within the active region of the devices; more specifically, we provide experimental evidence that the increase in SRH recombination is strongly related to the diffusion/build-up of charged defects within the active region of the devices. The properties of the defects involved in the degradation are investigated by means of deep level transient spectroscopy DLTS.

ESD tests on 850 nm GaAs-based VCSELs

Massimo Vanzi, Giovanna Mura, Giulia Marcello, University of Cagliari, Italy; Kunhui Xiao, Huawei Technolgy Co. Ltd, China

Forward and reverse HBM, MM, CDM ESD tests have been performed on 850-nm VCSELs, together with EOS and overpower test. The physical analysis of the tested devices showed a variety of damages not easily correlated to the measured electro-optical degradations. The solution requires the detailed interpretation of the observed physical mechanism, by means of electron microscopy and device modelling.

Degradation of InGaN laser diodes caused by temperature- and current-driven diffusion processes

Carlo De Santi, Matteo Meneghini, Gaudenzio Meneghesso, Enrico Zanoni, University of Padova, Italy

In this paper, we analyze the degradation of InGaN-based green laser diodes submitted to stress tests at different bias currents and junction temperatures. The variation of the threshold current suggests the presence of a diffusion process. The fitting of the degradation kinetics according to

Fick's second law allows for the extrapolation of the diffusion coefficient of the impurity/defect involved in the degradation process, and the related activation energy of 1.98 eV. The diffusion process is accelerated not only by the temperature but also by the flow of current. Taking into account the strong difference between experimental and theoretical diffusion coefficients of Mg and H in GaN, the physical model of the diffusion may need to be revised in order to take into account the role of electric field and carrier flow. The extrapolated values of the diffusion coefficient and of the related activation energy is consistent with the hypothesis that the degradation originates from the diffusion of hydrogen in the H+ species.

Catastrophic optical damage of high power InGaAs/AlGaAs laser diodes

Jorge Souto, Jose Luis Pura, Alfredo Torres, Juan Jimenez, Universidad de Valladolid, Spain; Mauro Bettiati, Francois Laruelle, 3SP Technologies, France

The defects generated by the catastrophic optical degradation (COD) of high power laser diodes have been examined using cathodoluminescence (CL). Discontinuous dark lines that correspond to different levels of damage have been observed along the ridge. Finite element methods have been applied to solve a physical model for the degradation of the diodes that explicitly considers the thermal and mechanical properties of the laser structure. According to this model, the COD is triggered by a local temperature enhancement that gives rise to thermal stresses leading to the generation of dislocations. Damage is initially localized in the QW, and when it propagates to the waveguide layers the laser ends its life.

Session 18A: Semiconductor Reliability & Failure Mechanisms: Miscellaneous

Plasma Process Induced Damage Detection by Fast Wafer Level Reliability Monitoring for Automotive Applications

Daniel Beckmeier, Andreas Martin, Infineon Technologies AG, Germany

Plasma process induced damage (PID) poses a device lifetime risk to all semiconductor products containing MOS gate dielectrics. This risk increases for smaller technology nodes. In this work we will present how to protect automotive products from PID. Products need to be made robust against PID by design checks with antenna rules determined in technology reliability qualifications. Additionally, damage that is invisible at zero hour, i.e. in parameter or product tests, needs to be detected by fast wafer level reliability (fWLR) monitoring on the fully produced wafer. The application and details of different stress types for charging cases are presented and discussed.

Channel width dependence of AC stress on bulk nMOSFETs

Donghee Son, Gang-Jun Kim, Ji-Hoon Seo, Bongkoo Kang, Pohang University of Science and Technology, Korea; Nam-Hyun Lee, Yongha Kang, Samsung Electronics, Korea

Channel width dependence of AC stress was investigated. OFF-state stress generated negative interface traps, positive oxide charges, and neutral traps in the whole channel region. Comparison of drain currents of parasitic and main MOSFET during OFF-state indicates that more defects were generated on channel edge than near its center. During ON-state stress, electrons were dominantly trapped in the neutral traps near channel edge. These results cause degradation due to AC stress to become increasingly severe as W is scaled down. The operating voltage to guarantee 10-year lifetime decreased as width decreased. The above results show that electron trapping in neutral traps near the channel edge induce severe degradation on narrow nMOSFET during AC stress. Therefore, degradation of channel edge during AC stress is an importantly considered in narrow nMOSFET.

Effects of voltage stress on the single event upset (SEU) response of 65 nm flip flop

Chung Tah Chua, Chee Lip Gan, Hock Guan Ong, Nanyang Technological University, Singapore; Philippe Perdu, Kevin Sanchez, CNES, French Space Agency, France

A newly integrated pulsed laser system has been utilized to investigate the effects of voltage stress on single event upset (SEU) of flip flop chain manufactured in 65 nm bulk CMOS technology. Laser mappings of the flip flop chain revealed that the SEU sensitive regions increased with laser energy. Post-processing of the data from the laser mapping facilitated the plotting of the cross-section versus laser energy curve. We found a clear shift in the crosssection curves after voltage stress of 130 hours. Comparisons of data revealed at least a doubled increase in sensitive areas after voltage stress. During the voltage stress, various electrical parameters were monitored and changes were observed. It was found that the increase in SEU sensitivity is related to electrical parameter changes and SPICE simulation results concur likewise.

Conductive filament formation at grain boundary locations in polycrystalline HfO_2 based MIM stacks- Computational and Physical Insight

Shubhakar Kalya, Sen Mei, Nagarajan Raghavan, Kin Leong Pey, Singapore University of Technology and Design, Singapore; Michel Bosman, Alok Ranjan, Sean Joseph O'Shea, IMRE Singapore, Singapore

Resistive switching in high-κ (HK) dielectric based metal-insulator-metal (MIM) devices occurs locally and is accompanied by dynamic changes in structural and electrical property of the HK dielectric. In polycrystalline HfO_2 HK dielectric based MIM devices, the presence of grain boundaries (GBs) play a significant role in the formation of a percolation path for the resistive switching as the GB regions contain large number of defects and favor the formation of conduction/low resistive paths. In this work, we present a multi-physics based combined Kinetic Monte Carlo- Finite element model (KMC-FEM) based 3D percolation framework to simulate the resistive switching (high resistive state (HRS) to low resistive state (LRS)) process in TiN/HfO_2 (~5nm)/Pt MIM stacks. The KMC-FEM model describes the effect of GBs on the nucleation of conduction path during the HRS to LRS resistive switching process. In addition, this model is used to find the statistical distribution of conductive path formation in amorphous and polycrystalline HfO_2 dielectrics. Conductive atomic force microscopy and transmission electron microscopy observations on the characteristics of the HfO_2 dielectrics at the nanometer scale complement the simulation results. The results clearly show that the resistive switching occurs preferably at the GB regions in polycrystalline HfO_2, whereas resistive switching in amorphous HfO_2 based MIM stacks occurs at random locations.

Microcontroller susceptibility variations to EFT burst during accelerated aging

Jianfei Wu, Chuangwei Li, Hongyi Wang, National University of Defense Technology, China; Binhong Li, Institute of Microelectronics of Chinese Academy of Sciences, China; Wei Zhu, Tianjin Binhai Civil-military Integrated Innovation Institute, China

With deterioration of the electromagnetic environment, microcontroller unit (MCU) electromagnetic susceptibility (EMS) to transient burst interference has become a focus of academia and enterprise. Most electromagnetic compatibility (EMC) studies of MCUs have not taken the effects of aging into account. However, component aging can degrade the physical parameters of an MCU and change its immunity to EMI. This paper proposes a time-equivalent interval accelerated aging methodology combining DC electrical and high temperature stresses. The test results show variations in susceptibility to electrical fast transients (EFT) burst revealing increasing susceptibility. The reasons for MCU immunity drifts in the aging process are discussed.

Session 18B: EUFANET/CAM-Workshop "Automotive Electronics Systems Reliability" (Part 3)

Si IGBT reliability for HVs

Satoshi Yasuda, Toyota Motor Corporation, Japan

Double side bonding technology has been applied in various electrified vehicles to realize higher power density by better cooling performance. This structure has an interface between power semiconductor device and solder on its top surface electrode. To enjoy the high power density

potential of double side bonding structure, we have to care about new reliability aspect on it in terms of mechanical stress. In this talk, I will show new reliability demand on Si power semiconductor devices for electrified vehicles in case introducing new double side bonding structure.

Power modules in automotive powertrains: qualification and test
Martin Rittner, Robert Bosch GmbH, Germany

Power electronics applications in electrified automotive powertrains demand for high robustness in technology selection and design for power modules. In drive inverters especially the active loading by currents, which heat up the chip and its surrounding, lead to significant temperature swings in the core of the module and initiates specific failure modes in the materials involved. Therefor the technology depended life-time curves exhibit a meaningful output parameter for the design of the entire powertrain.

New near chip technologies like Silver-sintering, diffusion soldering and Copper-bonding shift existing life-time curves to higher robustness. This means higher active power cycle numbers to failure at given temperature swing or higher temperature swings at given attainable power cycle numbers. This enables the operation of wide-band-gap power semiconductors like SiC and GaN at high temperature Tjunction values around 200°C and beyond. The initiation of new failure modes and the adaption of the latest qualification routines have to be taken into consideration for such equipped power modules.

Reliability of inverters and DC Link capacitors for e-mobility
Tim Langer, Volkswagen AG, Germany

The reliability for components used in cars is of highest importance. For traction inverters used in cars for e-mobility DC-link capacitors are one of the key components. Partners of the whole supply chain covering OEM to TIER2 have developed a significantly improved qualification standard for DC-link capacitors compared with the AEC-Q200. A uniform qualification procedure will help to decrease development costs and facilate the comparability of components of different suppliers. Capacitors qualified on basis of the new standard will help to even further increase the reliability of traction inverters in the future.

Estimation of IGBT power module reliability in pre-design phase
Amelie Thionville, Valeo, France

VALEO is currently developing sub-systems for new generation of electric powertrain (inverters, DC/DC converters...). As parts of these applications, semiconductors are subjected to very high stresses (especially thermal and cyclic) in their lifetime. Reliability database of electronic components such as FIDES, MIL-HDBK 217F, IEC/TR62380 have a lack of feedback for these new components for the automotive world, such as IGBT power modules. This is an issue for the pre-design phase, it is not possible to give a correct field returns on these components. That is why VALEO has developed a methodology and a tool to estimate the reliability of an IGBT power module for an inverter application based on the methodology used in the reliability prediction for mechanics as strength-constraint methodology.

Batteries and their reliability with special respect to traction applications
Marcel Held, R. Brönnimann, EMPA Swiss Fed Labs for Materials Testing and Research, Switzerland

Incidents of electrical vehicle catching fire forced on a root cause analysis. Failure mode and effects analysis (FMEA) and fault tree analysis (FTA) approaches were used for failure analysis and to design experiments on the battery system level. Analysis focused on the behaviour of an internal short circuit of a cell and its effect on the battery system and the vehicle. An internal short circuit of a stand-alone cell leads to venting and the release of dense smoke, however no fire or explosion occurred which complies with manufacturer declaration and hazard assessments according to battery safety standards. When such cell venting was triggered in the battery system it could be demonstrated that electric sparks on the carbonizing cell battery management print ignite the smoke and eventually lead to a fire of the complete vehicle. It has been shown that the use of comparatively safe Lithium-Iron-Phosphate cells does not entail a safe battery. The identification of the fire root cause enabled to develop and successfully test a mitigation method preventing fire caused by this failure mode.

Session 18C: Progress in Failure Analysis Methods: Novel non-destructive testing

Copper Through Silicon Vias Studied by Photoelastic Scanning Infrared Microscopy
Martin Herms, Matthias Wagner, PVA Metrology & Plasma Solutions GmbH, Germany; Ingrid De Wolf, IMEC, Belgium

The in-plane stress distribution in copper through silicon vias (TSV) ensembles of different design has been studied by the scanning infrared stress explorer (SIREX). SIREX is a reflection-based plane polarimeter particularly developed for the high-resolution stress state visualization in silicon-based electronic and mechanic devices. The SIREX method is based on the principle of stress-induced birefringence. We demonstrate that the silicon crystal matrix around the TSV is optically anisotropic with a stress distribution being similar to fields which are known from point-like stress sources. The maps of optical anisotropy have been converted into maps of difference of principal stress components Ds with a resolution of a few kPa. We show that magnitude and direction of Ds depend on the geometrical design of the TSV, in particular on length and diameter. The average radial profile of magnitude is discussed. In consequence, we offer a promising tool and method for the non-destructive evaluation of TSV structures in view of their stress characteristics and integrity.

Investigating Stress Measurement Capabilities of GHz Scanning Acoustic Microscopy for 3D Failure Analysis
Ahmad Khaled, Ingrid De Wolf, IMEC, Belgium; Sebastian Brand, Michael Kögel, Tim Appenroth, Fraunhofer Institute for Microstructure of Materials and Systems IMWS, Germany

This paper discusses the possibility of using Scanning Acoustic Microscopy in GHz frequencies for detection and analysis of stresses around TSVs. An innovative idea was employed to measure the slight variations in Rayleigh wave velocities as a function of Si crystal orientation using a spherical imaging lens. The fringe pattern around an empty TSV and a copper TSV were analyzed in different directions and Rayleigh wave velocities were calculated. The initial comparison between the measured velocities around the TSVs and the calculated values from a pure Si Crystal suggest the capability of using this technique in detecting Rayleigh wave velocity differences and thus, measuring stresses around Cu TSVs.

Detection and Analysis of Stress-induced Voiding in Al-Power lines by Acoustic GHz-Microscopy
Sebastian Brand, Michel Simon-Najasek, Michael Kögel, Jörg Jatzkowski, Frank Altmann, Fraunhofer Institute for Microstructure of Materials and Systems IMWS, Germany; Rainhard Portius, X-FAB Semiconductor Foundries AG, Germany

The formation of voids in metal layers upon stress-induced migration is a well-known defect mechanism in integrated circuits. This phenomenon largely accelerates with increasing ambient temperature. Consequently, the occurrence and the growth of voids result in an increased electrical resistivity which once more leads to an acceleration of the growth rate highly impacting the reliability and the life span of the device. Technological improvements aim at the minimization of stress induced voiding. However, for understanding and optimization of process related factors non- destructive methods for screening and systematic monitoring of the void formation e.g. during stepwise reliability testing are required. In the current paper, the formation of voids induced by repetitive thermal loads has been assessed and evaluated semi-destructively by employing Scanning Acoustic GHz-Microscopy. Prior to the acoustic inspection, sophisticated semi-destructive preparation was required to provide access to the region of interest. Voids with sizes below the acoustic resolution limit have been detected. The relative number and the size of appearance have been analysed using a custom made analysis software tool.

Magnetic Field and Current Density Imaging using off-line Lock-In Analysis

Michael Kögel, Sebastian Tismer, Frank Altmann and Sebastian Brand, Fraunhofer Institute for Microstructure of Materials and Systems IMWS, Germany

In the current paper the application of a custom developed 2-dimenional scanning magnetic field microscope based on tunnel-magnetoresistive sensors and subsequent qualitative and quantitative analysis is described. To improve sensitivity and to enable the detection and evaluation of phase deviations, an off-line lock-in approach was employed by driving the samples under test with an injected current at a fixed signal frequency. Amplitude and phase evaluation was based on simultaneous acquisition of the reference and the measurement signal obtained from the magnetic field sensor. This off-line lock-in approach enables not just the detection but also the estimation of changes in signal phase caused by capacitive, inductive or ohmic coupling of the induced currents. Furthermore assessed magnetic fields were converted into the current density by solving the inverse magnetic problem and post processing of the acquired signals. For verification of the developed set up the current density distribution was computed from experimentally acquired magnetic fields for a two-wire test structure. In addition quantitative values of the current density were derived for a calibration pattern containing defined structures. Finally, to evaluate the practical relevance a power MOSFET with unknown defect was analysed and an area of unexpectedly increased magnetic field intensity was observed.

Detection of cracks in multilayer ceramic capacitors by X-ray imaging

Caroline Andersson, Elise Varescon, ABB Switzerland Ltd., Switzerland; Jonny Ingman, Mika Kiviniemi, ABB Oy, Finland

A non-destructive method using X-ray imaging to find cracks in multilayer ceramic capacitors (MLCCs) mounted in different orientations with respect to the bending direction is presented. In total 300 MLCCs were investigated by 2D and 3D X-ray imaging after bending to varying levels of strain, and cross-section analysis was done to verify the findings. With X-ray imaging it was possible to not only detect the continuously cracked MLCCs, but also the cracked ones which were mounted 45° to the bending direction. These non-continuous cracks are difficult to identify even with cross-section analysis because the crack can be absent at the selected interface. None of the cracks could be identified by external optical inspection of the components using optical microscopy. The MLCCs mounted perpendicular to the bending direction were not cracked during the experiments, whereas the MLCCs mounted 45° or parallel to the bending direction were cracking at 3100 and 4300mStr, respectively. Finding cracks with a non-invasive technique such as X-ray imaging is very advantageous because of its possible implementation as a screening test in a production environment.

Session 19A: Reliability & Failure Mechanisms of MEMS and sensors

Application of high frequency scanning acoustic microscopy for the failure analysis and reliability assessment of MEMS sensors (invited)

Stefan Oberhoff, Kay Goetz, Karin Trojan, Martin Zoeller, Joachim Glueck, Robert Bosch GmbH, Germany

We successfully applied high frequency scanning acoustic microscopy (SAM) as a tool for the analysis of MEMS sensors. Using state of the art transducers with frequencies up to 300 MHz, we evaluated the achievable resolution and performed case studies: we localized a contamination-induced delamination on the ASIC surface and studied failure modes after mechanical stability tests, showing that a combination of SAM and infrared microscopical evaluation provides information about the course of cracks on a micrometer length scale.

Dielectric charging phenomena in diamond films used in RF MEMS capacitive switches: The effect of film thickness

Matroni Koutsoureli, Athanasios Zevgolatis, Loukas Michalas, George Papaioannou, University of Athens, Greece; Samuel Saada, Christine Mer-Calfati, Philippe Bergonzo, CEA, LIST, Diamond Sensors Lab., France

The present paper aims to provide a better insight to the dielectric charging phenomena of nano-crystalline diamond (NCD) films that are used in RF MEMS capacitive switches. The electrical properties of NCD films of various thicknesses are investigated with the aid of metal-insulator-metal (MIM) capacitors. The dominant conduction mechanisms have been identified by obtaining current-voltage characteristics in the temperature range from 300 K to 400 K and dielectric charging phenomena have been investigated by using thermally stimulated depolarization currents (TSDC) technique. The experimental results indicate a thermally activated conductivity for low electric field intensities while Hill-type conduction takes place for field intensities greater than 130 kV/cm. The conductivity as well as the defect density seems to increase with film thickness. Enhanced dielectric charging phenomena have been observed on thicker films and the injected charges are found to be trapped through the material's volume. These results indicate that thinner NCD films seems to be more promising for RF MEMS capacitive switches.

Effects of residual stresses on cracking and delamination risks of an avionics MEMS pressure sensor

Juergen Auersperg, Dietmar Vogel, Micro Materials Center at Fraunhofer ENAS, Germany; Christian Collet, Thierry Dean, Thales Research & Technology, France; Thomas Winkler, Berliner Nanotest and Design GmbH, Germany

Silicon based pressure sensors often take advantage of piezo-resistive gages which are normally embedded by multiple silicon oxide and silicon nitride layers where gold lines form a Wheatstone bridge. As a result of manufacturing – stepwise deposition of multiple layers – significant layer residual stresses in the GPa range occure in tension and compression. Especially in avionics MEMS applications such stresses determine the major risks for cracking and delamination. To overcome the related reliability issues the authors performed experiments and nonlinear FEM-simulations. Basic information about the residual stresses in the gage stack were captured by a Focused Ion Beam (FIB) trench technique combined with digital image correlation. These results enriched the data base for finite element studies with the ABAQUS™. Especially delamination risks were investigated by a surface based cohesive contact approach which simulates the initiation and propagation of damage and cracking within and underneath the gage layer. The cracking risk is investigated by means of an Extended Finite Element Method (XFEM). Both, crack initiation location as well as crack path are results of XFEM simulations. Several design variations have been investigated and compared to give insights to potential crack initiation sites and to evaluate the risk of fracture during processing.

A novel correlative model of failure mechanisms for evaluating MEMS devices reliability

Yaqiu Li, Yufeng Sun, Weiwei Hu, Zili Wang, Beihang University, China

The failure behavior of MEMS can be regarded as the result of certain dependent failure mechanisms in accordance with device's internal attributes and external environment. However, the correlative effects among multiple mechanisms that governing the failure process of MEMS have not been well characterized. This paper reviews significant failure mechanisms of MEMS products and proposes a new correlative model for MEMS reliability evaluation. Based on the nature of different failure mechanisms, dependent factors of these correlations are discussed and mathematical models are derived. With a case, reliability of a sort of RF switch is evaluated taking into account the failure mechanism correlative effects, and sensitivity analysis is conducted to assess the effects of the model parameters on reliability function R(t) and failure time distribution f (t).

Optimization of contact metallizations for reliable wafer level Au-Sn bonds

Vesa Vuorinen, Antti Rautiainen, Mervi Paulasto-Kröckel, Aalto University, Finland; Hannele Heikkinen, VTT Technical Research Centre, Finland

In this study, the focus was on the design for reliable wafer level hermetic Sn-Au based interconnection for MEMS devices by optimizing the contact metallization structures. The investigations were done in two parts: i)

the formation and evolution of interconnection microstructures in AuSn|Cu, AuSn|Ni and AuSn|Pt systems were studied with bulk diffusion couples and ii) thin film structures (i.e. adhesion layers and diffusion barriers) for Pt metallization on AuSn SLID bonded wafers were investigated from manufacturability and reliability viewpoints. The failure analysis was carried out on as bonded as well as aged interconnections. Distinct thin film structures showed clear differences in shear strength and fracture mechanisms. The mechanical reliability of the interconnection was increased by i) introducing sputtered Ni metallization between TiW and AuSn bond, ii) increasing the Pt thickness from 100 nm to 200 nm and iii) using Mo diffusion barrier underneath the Pt layer. Based on the results obtained from diffusion couples the thermodynamic descriptions of the ternary systems were re-assessed and the thermodynamic data was utilized in rationalizing the observed interconnection microstructures, failure mechanisms in thin film samples and the effect of Pt metallization thickness on the re-melting temperature of the SLID bond.

Session 19B: Reliability & Failure Mechanisms in Packages and Assembly: Tutorial

Creeping corrosion of copper on printed circuit board assemblies (Tutorial)

Gert Vogel, Siemens AG, Germany

The mechanism of creeping corrosion of copper has been studied and is understood. Creeping corrosion of copper occurs when low concentration of hydrogen sulfide (< 1 ppm H2S) in combination with a relative humidity greater than 60 % meets with bare copper on the bottom of a crack or pinhole. The forming copper sulfide is immobile but can be attacked by oxidizing agents and will diffuse in form of mobile copper oxide in a water layer (i. e. more than three molecule layers H2O) out of the pinhole. There it is retransformed again to immobile copper sulfide by attacking hydrogen sulfide. This is the reason that we find copper sulfide in combination with copper oxide a long distance away from the source of the copper, even if copper sulfide actually is immobile. In the humidity layer on a surface not only hydrogen sulfide acid as the essential corrosive substance is present but also oxidizing agents like O2, SO2 or NO2. The proportion between hydrogen sulfide and the oxidizing gases decides if copper oxide can be formed and creeping corrosion will start. In a microclimate like a hole or a crack the relation between oxidizing gases/acids and hydrogen sulfide is shifting to very low hydrogen sulfide concentration and the suggested mechanism will occur if enough oxidizing substances are present. Palladium in form of a nickel-palladium finish can act as a catalyst under certain circumstances. If H2S plus oxidizing gases as well as a humidity layer are present and cracks in bent copper pins supply the microclimate that is needed for creeping corrosion then a catalytic assisted corrosion takes place. The corrosive gases in the water layer are catalytically oxidized to form stronger acids and the forming copper oxide Cu2O from CuS is oxidized to smaller and more stable CuO that is more mobile and harder to retransform to CuS so it can cover longer distances. So we observe CuS far away from the corroded copper, even if CuS is immobile in principle. The corresponding effect on silver with diffusion of mobile silver oxide and a retransformation to immobile silver sulfide is not depending on humidity. Apart from that the mechanism is the same, but typically the silver sulfide forms sulfide needles and no flat corrosion layer.

Session 19C: Reliability & Failure Mechanisms of Wide Bandgap Devices: Tutorial

Field- and time dependent degradation of GaN HEMTs (Tutorial)

Enrico Zanoni, Gaudenzio Meneghesso, Matteo Meneghini, Isabella Rossetto, Carlo De Santi, University of Padova, Italy

For both microwave and power switching applications, Gallium Nitride (GaN) devices offer significant advantages with respect to their silicon and GaAs counterparts: high carrier mobility and carrier density, outstanding breakdown fields and the possibility of operating at very high temperature are reflected into the possibility of designing high efficiency and high frequency power amplifiers and power conversion systems. According to the targeted application and market, these devices are epitaxially grown on Si or SiC substrates, the option of GaN bulk substrates being still limited and expensive. Material defectivity, related with lattice mismatch between GaN and substrate, and the extremely high electric field values may cause potential reliability issues which are under intense investigation worldwide. This tutorial will review most recent works concerning the study of defects-related parasitic effects and of physical failure mechanisms of GaN devices.

After a short overview on the reliability of GaN HEMTs for microwave applications, the analysis will focus on the characterization of deep level effects in enhancement- and depletion-mode power GaN devices for switching applications. Threshold voltage instabilities in MISHEMT structures and their dependence on dielectric properties will be reviewed. Subsequently, it will be shown how the extremely high electric field values may lead to time dependent breakdown phenomena, affecting not only dielectric layers but also the GaN semiconductor itself. Recent data on the reliability of p-gate devices will be presented. Finally, breakdown mechanisms limiting the maximum device operating voltages will be reviewed.

Session 20A: Reliability & Failure Mechanisms in Packages and Assembly: Moisture and corrosion related studies

Effects of salt spray test on lead-free solder alloy

Alexandrine Guédon-Gracia, Hélène Frémont, Bernard Plano, Jean-Yves Deletage, IMS lab, France; Kirsten Weide, Leibniz Universität Hannover, Germany

This paper starts with a bibliographic survey about solder corrosion and experimental results of the corrosion on lead-free solder balls during salt spray tests. Focus is made on the SnAgCu solder alloy. Ball Grid Array assemblies and "Package on Package" components were put up to 96 hours in a salt spray chamber at 35°C with 5% sodium chloride (NaCl) aqua according to the ASTM B117-09 standard. The weight is measured during the test. The solder alloys are observed and analysed along the ageing with optical microscope and scanning electron microscope equipped with an energy-dispersive x-ray system. The solder alloy deterioration is visible after 48 hours. The microstructure is analysed in order to determine the corroded residues found on the surface solder balls after the salt spray test. Tin oxychloride (Sn(OH)Cl) is found on BGA solder joints after reflow and on PoP solder balls before reflow. The size of the solder balls has an influence on the corrosion state. Finally a method is developed in order to measure the corrosion product growth on the same sample during the salt environment exposure.

Novel failure mode of chip corrosion at automotive HALL sensor devices under multiple stress conditions

Michél Simon-Najasek, Georg Lorenz, Frank Altmann, Fraunhofer Institute for Microstructure of Materials and Systems IMWS, Germany; Achim Lindner, Micronas GmbH, Germany

Semiconductor devices used in automotive applications undergo numerous stress situations depending on their particular application. Corrosion, as one main crucial failure mechanisms, can affect the lifetime of electronic components on system, device or even die level. In this paper, a novel corrosion mechanism on HALL sensor devices is investigated and clarified. This corrosion is only occurring under complex conditions like layout aspects, ionic impurities combined with humidity penetration and thermo-mechanical strain due to packaging and additional mechanical load from further over moulding. It is shown how advanced physical and chemical analysis can be combined with finite element simulation to ascertain a chemical degradation running on silicon, silicon dioxide and metallisation level to derive the complete chemical reaction mechanism for the observed corrosion defects. To verify the new failure mode, experiments to recreate this type of corrosion were carried out. Finally, conclusions are drawn on how failure modes can be prevented and how the robustness of the HALL devices under harsh environments can be increased.

Moisture absorption by molding compounds under extreme conditions: impact on accelerated reliability tests

Amar Mavinkurve, Michiel van Soestbergen, Jeroen Zaal, NXP Semiconductors, France; Jaume Llacer Martinez, NXP Semiconductors, Spain

The Highly Accelerated Stress Test (HAST) [130°C/85%RH or 110°C/85%RH with applied bias voltage] or Autoclave test [121°C/100%RH] are well-accepted tests during qualification and reliability testing of automotive microelectronics. These tests are often preferred since results can be obtained relatively fast due to the high acceleration. On the other hand, there is a risk of accelerating non-relevant failure modes e.g. due to changes in material behavior under test conditions, which will not occur during application. However, predicting what happens under test conditions is not straightforward since one needs to understand material behavior under such extreme conditions. Especially the amount of water absorption, which is highly relevant for test result interpretation, is challenging to obtain at temperatures above 100 °C, since here we deal with pressurized conditions.In this paper a novel, and straightforward, method is proposed to determine the moisture absorption under pressurized conditions. To verify the method, data obtained under pressurized conditions is compared to behavior under standard conditions. Under autoclave conditions it is shown that the moisture uptake at higher temperatures is much higher than predicted by extrapolation. The reported data can also be used to predict more reliably the moisture saturation level, and rate of moisture saturation during HAST.

Effect of PCBA surface morphology and chemistry on water layer formation under humid conditions and corrosion reliability

Kamila Piotrowska, Rameez Ud Din, Morten Stendahl Jellesen, Rajan Ambat, Technical University of Denmark, Denmark

In this paper, the effect of different laminate and solder mask surface morphology and composition on water film formation under humid and condensing conditions was investigated. Water film formation, its thickness, and the resulting electrical properties as a function of humidity levels and temperature conditions were evaluated. Thickness of the water layer under condensing conditions was measured as a function of sample cooling rates and compared to the resulting reduction in impedance. The dependency of water film formation on the surface chemistry and topography, and its influence on the changes of electrical signal as a function of different climatic conditions are described.

Session 20B: Reliability & Failure Mechanisms of Wide Bandgap Devices: Microwave devices

GaN devices: millimeter wave applications challenges (invited)

Sylvain Delage, III-V Labs (FR)

GaN-HEMT technology has been commercially available for several years and is a disruptive technology for high frequency RF power applications. GaN semiconductor offers wide band and high power capabilities thanks to its high saturation electron velocity, chemical stability and high breakdown voltage. GaN technology has been first developed and made available for base station applications for L-Band. Fierce competition does exist against well installed Si-LDMOS technology for saturated output power up to 1kW at frequencies below 4GHz. The landscape is more open for higher frequency bands as silicon devices have intrinsic physical limitations. Actually GaAs devices are the current existing solid-state competitor for high power microwave applications and occupy strong positions in various applications. GaN devices are allowing higher output powers, denser circuits and wider bandwidths. Products are coming in the market for Ka-Band applications. It is foreseen that circuits will be developed for up to 90GHz for applications such as E-Band data backhauling. Material and technological challenges will be presented with a particular focus on reliability aspects.

Continuous Time-Domain RF waveforms monitoring under overdrive stress condition of AlGaN/GaN HEMTs

Agostino Benvegnu, Sylvain Laurent, Raymond Quere, Denis Barataud, XLIM laboratory, France; Matteo Meneghini, Enrico Zanoni, University of Padova, Italy; Jean-Luc Roux, CNES, France

This paper reports an advanced time-domain methodology to investigate the device reliability and determine its Safe Operating Area of AlGaN/GaN HEMTs. The presented technique is based on the continued monitoring of the RF waveforms and DC parameters in order to assess the degradation of transistor characteristics in RF power amplifiers. The reliability study is carried out in class AB operation, under RF operating excitation at high drain voltages and overdrive conditions (12 dB compression). The analysis is carried out with two different output load impedances: optimum of PAE and mismatched impedance. The results show a drift of RF performances due to a variation of electrical parameters. In particular, the operation with optimum PAE load impedance induces slight positive threshold voltage shift. The operation with mismatched load shows a stronger degradation, with a positive threshold voltage shift and a drop in saturation drain current, due principally to the high temperature reached by the devices during RF stress.

Correlation of gate leakage and local strain distribution in GaN/AlGaN HEMT structures

Mikael Broas, Aalto University, Finland; Andreas Graff, Michel Simon-Najasek, David Poppitz, Frank Altmann, Fraunhofer Institute for Microstructure and Systems IMWS, Germany; Helmut Jung, Hervé Blanck, United Monolithic Semiconductors GmbH, Germany

GaN/AlGaN HEMT structures are observed to undergo a reversible, drastic change in the leakage current when covered with an additional polymer passivation layer. The polymer layer induces a stress on the HEMT structures, which initiates material migration processes and the formation of structural defects, influencing the electrical performance. Local strain measurements were performed in the semiconductor, at the critical HEMT gate electrode, to evaluate the impact of the stress on the Schottky gates. The strain distributions in the structures were measured with nanobeam electron diffraction from electron-transparent samples at cross sections and longitudinal sections at the positions of high leakage currents. A variation of the strain distribution underneath the gate electrode was detected in a cross-sectional sample. On the contrary, only minor differences in the strain values were measured in the longitudinal sections at different photoemission sites. Finally, localized metal interdiffusion was detected at the sites with the highest photoemission intensities.

Session 21A: Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Miscellaneous

Early life field failures in modern automotive electronics – An overview, root causes and precautions

Peter Jacob, EMPA Swiss Fed Labs for Materials Testing and Research, Switzerland

Forensic failure analysis of automotive electronics deals in most cases with failures within the guarantee period. Frequently, specific operational conditions, even for a short moment, combine with specific electronic sensitivities – against ESD discharge, switching spikes, humidity ingress, vibration, undefined grounding circuitry. The paper lists impressive, partially curious examples of related failure anamnesis and analysis and tries to draw some important conclusions with respect to prevention and failure anamnesis/ failure analysis methodologies.

Crack-guided effect on dynamic mechanical stress for foldable low temperature polycrystalline silicon thin film transistors

Sang Myung Lee, Cheon Taek Park, Ilgu Yun, Yonsei University, Korea

In the thin film transistors (TFTs) device research for foldable display, the degradation effect by the mechanical stress is crucial. Here, the crack position is critical for TFT reliability. However, it is difficult to characterize the crack position due to the random generation of the crack by mechanical stress. In this paper, the crack-guided low temperature polycrystalline silicon (LTPS) TFT test structures are fabricated and the crackguided effects on mechanical stress of the tested TFT structure are analyzed. To strain on the foldable LTPS TFTs, 50,000 cycles of tensile and parallel direction dynamic mechanical stresses were applied with 2.5-mm bending radius. Based on the results, the generating crack position can be guided and controlled and also TFT reliability for foldable display can be enhanced.

Impact on Non-linear Capacitances on Transient Waveforms during System Level ESD Stress

Fabien Escudié, Fabrice Caignet, Nicolas Nolhier, Marise Bafleur, LAAS-CNRS, France

Prediction of failures induced during system level ESD stress is mainly related to the transient waveforms at chip level. To investigate hard and soft failures a precise modeling of the system is required. On-chip protection models can be obtained using quasi-static measurements. Even if such models can achieve good ESD simulations the impact of the external elements are more important. Paper deals with non-linear behaviors of the external elements related to the on-chip protections. Characterization techniques and models are presented, based on two types of capacitances, two different values, placed in parallel to on-chip protections. The paper shows the important variations of X7R capacitances during stresses that change the waveforms at the input of the chip. In measurements different behaviors are observed and reproduced by simulation. The methodology to build model and simulation will be presented.

Evolution study of the ElectroMagnetic Interference for RF LD-MOS in series chopper application after thermal accelerated tests

Mohamed Ali Belaid, SAGE-ENISo, Tunesia

The temperature is a critical parameter, for proper functioning of a system or a circuit, particularly in RF electronic devices. It considerable influence on reliability and performances; consequently plays an essential part in failure mechanisms and in lifetime. Recent studies have been focused in ElectroMagnetic Interferences (EMI) evolution after accelerated ageing tests and their effects on robustness behaviours (static, dynamic and RF). Even rarer to use RF devices in a power application.

This paper deals with the (EMI) evolution of conducted interferences in common and differential mode of RF LDMOS (Radio Frequency Lateral Diffused Metal–Oxide–Semiconductor) devices applied to a series chopper. In addition their influences on the electrical parameters are studied after various thermal accelerated ageing tests. The experimental results (spectre and waveform parameters) are presented and discussed. The obtained measurements have highlighted that there is a clear increase in the amplitude of resonances on the interference spectra after ageing. The evolution is not the same for all the parameters and for the different thermal tests. The shift is proportional to temperature. To reach a better understanding of the physical mechanisms of parameter's shift after thermal tests, a numerical model (Silvaco-Atlas) was employed to confirm the degradation phenomena. Actually, the charge trapping in the gate oxide causes a decrease in the Miller capacity value (Crss), thereafter in turn a decrease in the disturbances level.

Temperature rise measurement for power-loss comparison of an aluminium electrolytic capacitor between sinusoidal and square current injections

Kazunori Hasegawa, Kentaro Kozuma, Kousuke Tsuzaki, Ichiro Omura, Shin-Ichi Nishizawa, Kyushu Institute of Technology, Japan

DC-link capacitors are a major factor of degrading reliability of power electric converters because they usually have a shorter lifetime and higher failure rate than those of semiconductor devices or magnetic devices. Characteristics of the capacitors are usually evaluated by a single sinusoidal current waveform. However, actual current flowing out of the converter into the capacitor is a modulated square current waveform. This paper provides experimental comparison of the power loss dissipated in an aluminium electrolytic capacitor between sinusoidal and square-wave current injections. Power loss is estimated by temperature rise of the capacitor. Experimental results confirms that power losses of the square-wave current injection were always lower than those of the sinusoidal current injection by 10-20%. Moreover, the power losses of the square-wave current injection can be estimated by a synthesis of fundamental and harmonic currents based on the Fourier series expansion, which brings a high accuracy less than 1% when more than fifth harmonic current is introduced. This comparison will be useful for estimating power loss and life time of electrolytic capacitors.

Session 21B: Reliability & Failure Mechanisms in Packages and Assembly: Reliability and Modelling

Reliability Evaluation of Donut-Tungsten-Via as an Element of the Highly Robust Metallization

Verena Hein, Marco Erstling, X-FAB AG, Germany; Raj Sekar Sethu, X-FAB AG, Malaysia; Kirsten Weide-Zaage, Leibniz Universität Hannover, Germany

The typical via layout in CMOS technology with AlCu-metallizations and tungsten via is cylindrical. Common vias have a size as small as possible in the related process. More challenging application, temperature and mission profiles require higher robustness of a metallization [1, 2]. Via arrays of small common vias are in use to the transfer of higher currents [3]. But the typical via array layout is not the best layout for applications which are faced to high mechanical stress because via arrays metal layer connections make these parts in the stack inflexible. The developed so called highly robust metallization is optimized for applications with extended operating conditions regarding higher currents and temperatures as well as mechanical stress [4]. Donut-Vias are elements of the highly robust metallization for the interconnection of highly robust metal lines. The paper shows the layout of a Donut-Via and explains the benefits and limits of the new layout by simulation and test results.

Reliability Evaluation of Si-Dies due to Assembly Issues

Falk Naumann, Frank Altmann, Fraunhofer Institute for Microstructure and Systems IMWS, Germany; Volkmar Gottschalk, Bernd Burchard, ELMOS Semiconductor AG, Germany

Silicon based semiconductor devices are stressed during fabrication, handling and packaging with significant thermal and mechanical loadings. In worst cases, these induced loadings can cause initial chip damage leading to electrical failure or fracture of the Si-die during further process steps or application. In order to evaluate the risk of pre-damage during assembly, a case study of potential failure modes taking pick-and-place processes into account was performed. Therefore, pre-damaged samples using a misaligned pick-and-place setup were generated. Afterwards, methods of microstructural crack analyses and mechanical strength testing were applied to evaluate the damage impact of the generated needle imprint. In addition, finite element analyses in combination with fracture mechanical approaches were combined to evaluate the failure probability of Si-dies during the following assembly or thermal cycling steps. As a result of this study, critical process steps during chip assembly can be identified and critical tolerance limits of the process can be evaluated to achieve an acceptable reliability level. Consequently, the risk of failure caused by handling or assembly issues can be estimated and appropriate steps for quality assurance procedures can be defined.

Fatigue testing method for fine bond wires in an LQFP Package

Bernhard Czerny, Golta Khatibi, CTA, TU Wien, Austria; Ali Mazloum-Nejadari, Laurens Weiss, Infineon AG, Germany; Michael Zehetbauer, University of Vienna, Austria

A mechanical testing setup was developed to study the fatigue response of fine thermo-sonic wire bond connection in low profile quad flat packages (LQFP). The testing set-up was designed to induce pre-defined multiaxial stresses in the wire bond loops of non-encapsulated packages in order to mimic their deformation behavior during the thermo-mechanical loading. Lifetime curves were obtained up to 1.0e7 loading cycles with fatigue failure occurring in the heat affected zone of the ball bond. The experimental fatigue data in combination with extended FEA provided the basis for a Coffin Manson lifetime model. The proposed fatigue testing procedure can be applied as a highly efficient method for evaluation of various wire bonded packages by using a limited number of test samples and simultaneous testing of several wire bonds.

Fast and Trusted Intrinsic Stress Measurement to Facilitate Improved Reliability Assessments

Dietmar Vogel, Ellen Auerswald, Ghanshyam Gadhiya, Sven Rzepka, Fraunhofer ENAS, Germany

A new measurement method for mechanical stresses with microscopic and sub-microscopic spatial resolution is presented. It bases on classical

stress relief techniques in experimental mechanics, as for example the familiar hole drilling method. Applicability of the classic method for micro and nano size objects was achieved, using very local stress relief caused by ion milling inside commercial FIB equipment and image correlation algorithms for the determination of corresponding relaxation strains. Approximately 10 years ago, first publications demonstrated the principal feasibility of the approach. Now, this work gives a more detailed view on different measurement variations, their capabilities and limitations. The paper reports on the effort made for qualifying the new method for use under real industrial conditions, which includes validation of techniques, best practice based choice of tools and sufficient automation of the measurement process. Finally an application example from 3D integration in electronics demonstrates practical benefit obtained by the method.

Delamination of polyimide/Cu films under mixed mode loading

Thomas Walter, Martin Lederer, Golta Khatibi, Peyman Rafiee, Vienna University of Technology, Austria

Organic passivation layers are used as coatings in semiconductor devices for protection of metallization films against a variety of environmental effects. Polyimides (PI) have been used successfully as conformable protection layers on aluminium and also recently on copper metallization. While adhesion properties of Cu interconnects to compliant polymer substrates have been investigated so far, studies on PI/Cu passivation layers are scarce. In this study the adhesion strength of polyimide passivation layer to Cu film stacks on Si has been studied by using different fracture mechanic methods including four point bending, double cantilever beam and single lap shear tests. The focus is investigation of the dependency of the critical energy release rate to the mode mixity obtained by different testing techniques and evaluation of the delamination data using analytical models and by means of FEA and cohesive zone modelling.

Session 21C: Reliability & Failure Mechanisms of Wide Bandgap Devices: GaN power devices and deep level transient spectroscopy

Study of the stability of e-mode GaN HEMTs with p-GaN gate based on combined DC and optical analysis

Isabella Rossetto, Matteo Meneghini, Vanessa Rizzato, Gaudenzio Meneghesso, Enrico Zanoni, University of Padova, Italy; Steve Stoffels, Marleen Van Hove, Niels Posthuma, Tian-Li Wu, Denis Marcon, Stefaan Decoutere, IMEC, Belgium

This paper investigates the robustness of normally-off High Electron Mobility Transistors (HEMTs) with p-GaN gate submitted to forward gate bias overstress. By means of combined DC and spectral analysis we demonstrate the following results: (i) the devices demonstrate a time-dependent failure mechanism; (ii) time to failure (TTF) can be described by a Weibull distribution with a shape factor higher than 1, suggesting a wear-out failure; (iii) the devices have an estimated 20-years lifetime for a gate voltage of 7.2V; (iv) TTF is temperature-dependent, with an activation energy of 0.5 eV; (v) emission microscopy reveals the presence of hot spots, whose emission originates from yellow luminescence and/or hot electron radiation.

UIS test of high-voltage GaN-HEMTs with p-type gate structure

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This paper reports the withstanding capability of unclamped inductive switching (UIS) of high voltage GaNHEMTs as a function of the gate voltage in the off-state. One of the critical disadvantages of GaN-HEMTs is its lack of the UIS withstanding capability because of the non-removable structure of holes, which are generated by the avalanche breakdown. Therefore, a p-type GaN gate structure is attractive not only for normally-off operation but also for the UIS withstanding capability design from the viewpoint of hole-removal. This paper shows the results of the UIS test for GaN-HEMTs with the p-type gate structure. The UIS withstanding capability of GaN HEMTs can be designed via the hole removal structure and the package thermal resistance.

Temperature Dependent Dynamic ON State Resistance in GaN on Si Based Normally OFF HFETs

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Enhancement-mode GaN-on-Si HFETs for power switching application are investigated under fast switching and elevated ambient temperatures conditions. The switching characteristics are used to evaluate the dynamic ON-state resistance at temperatures up to 175°C, while switching drain voltage up to 400 V. The devices show a low increase of less than 25% in dynamic resistance when increasing the ambient temperature up to 125°C. However, differing from expectations, above this temperature a rapid increase of ON-resistance up to 85% occurs. Such anomaly indicates the existence of thermally activated trapping processes. Trapping transients taken over a large temperature range and a wide range of OFF-state stressing time show that in parallel to the buffer trapping, with activation energy of 0.80 ±0.02 eV, an additional de-trapping process with activation energy of 0.42 ±0.05 eV occurs through increased leakage current over the temperature.

Experimental study of the short-circuit robustness of 600V E-mode GaN transistors

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This paper presents experimental robustness of 600 V GaN High Electron Mobility Transistors (HEMT) submitted to Short-Circuits (SC) operation modes. A dedicated secured test bench has been developed and designed in order to protect as quickly as possible the Device Under Test (DUT) after failure. Some devices featured a great robustness under SC and were able to support several SC of a very long duration. On the contrary, others failed immediately at the first pulse, for a low dissipated energy. The obtained results reveal a severe dispersal in terms of SC robustness for these new emerging components. Gate behavior has been also studied, showing a leakage current during each SC, destructive or not. A part of the paper is also dedicated to the study of the effects of case temperature and DC voltage on robustness.

Local deep level transient spectroscopy using super-higher-order scanning nonlinear dielectric microscopy

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A new technique for local deep level transient spectroscopy imaging using super-higherorder scanning nonlinear dielectric microscopy is proposed. Using this technique, SiO2/SiC structure samples with different post oxidation annealing conditions were measured. We observed that the local DLTS signal decreases with post oxidation annealing (POA), which agrees with the well-known phenomena that POA reduces trap density. Furthermore, obtained local DLTS images had dark and bright areas, which is considered to show the trap distribution at/near SiO2/SiC interface.

Session 22: Poster Session for Tracks:

- Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems
- Reliability & Failure Mechanisms in Packages and Assembly
- Reliability & Failure Mechanisms of Wide Bandgap Devices
- Reliability & Failure Mechanisms of MEMS and sensors

Power cycle reliability of Cu nanoparticle joint dependent on a mismatch of coefficients of thermal expansion

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The power cycle reliability of Cu nanoparticle joints between Al2O3 heater chips and different heat sinks (Cu- 40wt.%Mo, Al-45wt.%SiC and pure

Cu) was studied to explore the effect of varying the mismatch in the coefficient of thermal expansion (CTE) between the heater chip and the heat sink from 4.9 to 10.3 ppm/K. These joints were prepared under a hydrogen atmosphere by thermal treatment at 250, 300 and 350 °C using a pressure of 1 MPa, and all remained intact after 3000 cycles of 65/200 °C and 65/250 °C when the CTE mismatch was less than 7.3 ppm/K, despite vertical cracks forming in the sintered Cu. When the CTE mismatch was 10.3 ppm/K, the Cu nanoparticle joint created at 300 °C endured the power cycle tests, but the joint created at 250 °C broke by lateral cracks in the sintered Cu after 1000 cycles of 65/200 °C. The Cu nanoparticle joint created at 350 °C also broke by vertical cracks in the heater chip after 1000 cycles of 65/250 °C, suggesting that although sintered Cu can be strengthened to tolerate the stress by increasing the joint temperature, this eventually causes the weak and brittle chip to fracture through accumulated stress. The calculation results of stresses on the heater chip showed that the stress can be higher than the strength of Al2O3 when the CTE mismatch is 10.3 ppm/K and the Young's modulus of the sintered Cu is higher than 20 GPa, suggesting that the heater chip can be broken.

Impact of work function of the silicon bottom-gates on electrical instability in InGaZnO thin film transistors

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The electrical instability in amorphous InGaZnO (IGZO) thin film transistors has been investigated for different doping types and concentrations of silicon bottom-gates. The gate current (IG) was measured to prove that the threshold voltage shifts (ΔVTH) were due to electron and hole trapped charges under positive and negative gate stress, respectively. After the gate stress, the ΔVTH in IGZO transistors depend on the work function of the silicon gates. The ΔVTH listed in order of magnitude are ΔVTH-n+=gate>ΔVTH-n-gate>ΔVTH-p-gate>ΔVTH-p+-gate after a positive gate stress and a positive thermal illumination stress, but this is reversed after a negative gate stress and a negative thermal illumination stress. The more significant ΔVTH after a negative thermal illumination stress than after positive thermal illumination stress may be attributed to the low-level injection under light illumination. To minimize ΔVTH in IGZO transistor with a silicon bottom-gate, a low-doped gate is recommended.

Device instability of amorphous InGaZnO thin film transistors with transparent source and drain

Sang Min Kim, Incheon National University, Korea; Min Ju Ahn, Won Ju Cho and Jong Tae Park, Kwangwoon University, Korea

The investigations on the device instabilities of a-InGaZnO thin film transistors with transparent source and drain have been performed according to the different thermal annealing treatment after positive gate bias stress (PBS) and hot carrier stress. The controlled devices with a rapid thermal processing (RTP) treatment in addition to conventional thermal annealing showed less degradation after PBS and hot carrier stress at the same stress biases. The reason for lower device degradation could be explained by the higher effective barrier energy which may be resulting from oxygen outdiffusion. However, the controlled device showed more serious degradation at the same actual stress voltages to the intrinsic part of device. This result may be attributed to the increased channel electron concentrations which were resulted from the increased oxygen vacancies. The degradation of the controlled devices was more serious after hot carrier stress than after PBS. From C-V measurement and transfer characteristics in forward and reverse mode measurements, hot carrier induced degradation could be attributed to the interface state generation and the electron trappings at interface between the active channel layer and the gate dielectric layer.

Negative bias illumination stress instability in amorphous InGaZnO thin film transistors with transparent source and drain

Jong Hoon Lee, Seul Ki Yu, Jae Won Kim, Jong Tae Park, Incheon National University, Korea; Min Ju Ahn, Won Ju Cho, Kwangwoon University, Korea

The investigations on the device instabilities in amorphous InGaZnO TFTs with metal (Ni) and transparent (ITO and InGaZnO) source and drain electrodes have been performed under negative bias stress (NBS), negative bias thermal stress (NBTS), negative bias illumination stress (NBIS) and negative bias thermal and illumination stress (NBTIS). From the measured device parameters in dark and under illumination conditions, a-IGZO TFTs with InGaZnO source and drain show an excellent device performances and lower device degradation than the devices with Ni and ITO source and drain under NBS and NBTS. However, amorphous IGZO TFTs with InGaZnO source and drain electrodes show more significant device degradation under NBIS and NBTIS. In order to explain our experimental results, we propose that the center responsible for the device instability is the processrelated defects under NBS and NBTS, and the oxygen vacancy under NBIS and NBTIS, respectively.

Effects of drain quiescent voltage on the ageing of AlGaN/GaN HEMT devices in pulsed RF mode

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The reliability of RF AlGaN/GaN HEMT devices on SiC substrate is investigated here in pulsed RF condition at nominal and maximum rating drain quiescent bias. During these 3500 hours tests, high voltage especially during the RF pulse leads to a progressive decrease in gm and IDS S while trap concentration increases. These evolutions may be attributed to trap generation by hot carrier injection and highlight the importance of drain quiescent voltage as an important acceleration factor for this technology's reliability in pulsed RF conditions.

On the need for a new ESD verification methodology to improve the reliability of ICs in advanced 28nm UTBB FDSOI technology

Benjamin Viale, Mathieu Fer, Lionel Courau, Philippe Galy, Bruno Allard, STMicroelectronics, France

The need for a novel multi-scale ESD (ElectroStatic Discharge) network recognition and verification methodology is described in this paper. The proposed solution is used to limit the risk of ESD design errors and to enhance IC reliability, independently of the implemented ESD protection strategy and the type of package assembly technique. This method relies on a topology-aware & graph-based verification paradigm which is generic enough to be usable at every step of the design flow. Its efficiency is illustrated with examples involving custom I/O ring portions in 28nm UTBB FD-SOI High-K metal gate technology.

Instability of oxide thin film transistor under electrical-mechanical hybrid stress for foldable display

Dongseok Shin, Min Soo Bae, Ilgu Yun, Yonsei University, Korea

Degradation mechanism of foldable thin film transistors (TFTs) is investigated experimentally by electrical, mechanical and electrical-mechanical hybrid stress experiments. Mechanical and electrical stress environment was set for foldable TFTs and the degradation effect according to the applied stress is investigated and analyzed. Degradation mechanism model that can explain the defect generation is suggested to explain the result of electrical-mechanical hybrid stress experiment.

FESeR: a data-driven framework to enhance sensor reliability for the system condition monitoring

Liansheng Liu, Datong Liu, Harbin Institute of Technology, China

The collected system information is critical for Condition Monitoring (CM) which is mainly implemented by utilizing various types of sensors. Hence, the reliability of sensors directly influences the evaluation result of CM. One type of data-driven framework to enhance sensor reliability is realized in this article. To be specific, the combination of sensor selection method and data anomaly detection is achieved by information theory and Kernel Principle Component Analysis (KPCA). The sensors which can provide more valuable information for system CM are selected. The correlations among sensors are analysed by mutual information. Finally, the data anomaly detection is conducted by utilizing the correlations among sensor data sets and KPCA. The effectiveness is proved by employing sensor data sets from National Aeronautics and Space Administration Ames Research Center.

An in depth analysis of pull-up capacitance-voltage characteristic for dielectric charging assessment of MEMS capacitive switches

Matroni Koutsoureli, Dimitrios Birmpiliotis, Loukas Michalas, George Papaioannou, University of Athens, Greece

The present paper aims to provide a better approach on the analysis of pull-up capacitancevoltage characteristic of MEMS capacitive switches by introducing an analytical model that takes into account the case of a real device, where the charge is not uniformly distributed at the surface of the dielectric film and the capacitor armatures are not parallel. The proposed model allows the use of capacitance-voltage characteristic's derivative, which slope is directly related to the device mechanical characteristics and the stress induced during charging. The application of the model on a MEMS switch with asymmetric capacitance-voltage characteristic and on a switch with a parabolic up-state capacitance-voltage characteristic during charging and discharging processes allows the draw of some initial conclusions on the charging and the mechanical performance of the devices. Further investigation is in progress in order to extract important information on the device degradation.

Role of Two-Dimensional Electron Gas (2DEG) in AlGaN/GaN High Electron Mobility Transistor (HEMT) ON-State Degradation

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We have investigated the influence of the two-dimensional electron gas (2DEG) in AlGaN/GaN high electron mobility transistors (HEMTs) on their reliability under ON-state conditions. Devices stressed in the ONstate showed a faster decrease in the maximum drain current (IDmax) compared to identical devices stressed in the OFF-state with a comparable electric field and temperature. Scanning electron microscope (SEM) images of ON-state stressed devices showed pit formation at locations away from the gate-edge in the drain-gate access region. Cross-sectional transmission electron microscope (TEM) images also showed dark features at the AlGaN/SiN interface away from the gate edge. Electron energy loss spectroscopy (EELS) analysis of the dark features indicated the presence of gallium, aluminum and oxygen. These dark features correlate with pits observed in the SEM micrographs. It is proposed that in addition to causing joule heating, energetic electrons in the 2D electron gas contribute to device degradation by promoting electrochemical oxidation of the AlGaN.

Structural disturbances in GaN HEMT layers as source of leakage current, influencing device performance and reliability

Sven Besendörfer, University of Erlangen-Nuremberg, Germany; Elke Meißner, Jochen Friedrich, Fraunhofer Institute for Integrated Systems and Device Technology, Germany; Lothar Frey, University of Erlangen-Nuremberg, Germany

In this paper we report on investigations of the effect of structural disturbances in GaN HEMT layer stacks on the electrical characteristic. It will be shown that one can clearly resolve vertically highly conductive leakage paths corresponding to threading dislocations which terminate at the surface of the topmost epitaxial layer. Moreover there is evidence that different types of dislocations do have different electrical properties relevant for the electrical performance of devices. This fact motivates the preference of specific growth technologies hampering the most deleterious types of dislocations.

Component Reliability Importance assessment on complex systems using Credible Improvement Potential

Marcantonio Catelani, Lorenzo Ciani, Matteo Venzi, University of Florence, Italy

Nowadays system reliability performance represents a key issue and being reliable become a fundamental requirement of products in many manufacturing fields. The paper is focused on the reliability improvement of fault tolerant complex systems using component Reliability Importance (RI) procedures in order to assess the impact of each component on the overall system reliability. This study is focused on RI assessment during design stage with the aim of optimizing engineers' efforts and focusing on components with the greatest effect on the whole system. The first part of the paper focuses on a particular Reliability Importance measure, the Credible Improvement Potential (CIP), which is the most suitable RI metric for our purpose. The Reliability Importance assessment on a dedicated case study based on fault tolerant complex system is then proposed and results are discussed in detail.

Fatigue Life Prediction Model for Accelerated Testing of Electronic Components under Non-Gaussian Random Vibration Excitations

Yu Jiang, Junyong Tao, Yun'An Zhang, National University of Defense Technology, China

In this paper, a novel fatigue life prediction model for electronic components under non-Gaussian random vibration excitations is proposed based on random vibration and fatigue theory. This mathematical model comprehensively associates the vibration fatigue life of electronic components, the characteristics of vibration excitations (such as the root mean square, power spectral density, spectral bandwidth and kurtosis value) and the dynamic transfer characteristics of electronic assembly (such as the natural frequency and damping ratio) together. Meanwhile a detailed solving method was also presented for determining the unknown parameters in the model. To verify the model, a series of random vibration fatigue accelerated testing were conducted. The results obtained show that the predicted fatigue life based on the model agreed with actual testing. This fatigue life prediction model can be used for the quantitative design of vibration fatigue accelerated testing, which can be applied to assess the long-term fatigue reliability of electronic components under Gaussian and non-Gaussian random vibration environment.

DRES: Data recovery for condition monitoring to enhance system reliability

Liansheng Liu, Yujie Zhang, Harbin Institute of Technology, China

The system reliability depends heavily on the sensed condition data which are mainly collected by various types of sensors. The missing or faulty condition data can result in wrong decision-making or lead to system fault. To realize data integrity for system condition monitoring, one data-driven framework for recovering condition data is proposed in this article. The proposed model is combined by mutual information and Multivariable Linear Regression (MLR). The correlations among condition monitoring data sets are firstly analysed by mutual information. Then, MLR is utilized to recover condition monitoring data. A case study of aircraft engine condition monitoring data sets which are offered by National Aeronautics and Space Administration Ames Research Center is carried out to evaluate the performance of the data-driven framework.

The radiation test based assessment of process quality and reliability for conventional 65-nm CMOS technology

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This work presents a solution for radiation hardness assessment using compact and productive X-ray facilities, as well as the automated measurement system. The radiation test procedure can be integrated in commercial IC's process as a mandatory option for providing high reliability and radiation hardened IC projects. Using the radiation test procedure as a one of technology stage, the assessment of total ionizing dose (TID) hardness was done for test structures, which were fabricated in conventional 65nm CMOS technology.

Chemical rate phenomenon approach applied to Lithium battery capacity fade estimation

Issam Baghdadi, Olivier Briat, Jean-Yves Delétage, Jean-Michel Vinassa, IMS Labs, France; Philippe Gyan, Renault, France

This paper deals about a lithium battery capacity aging model based on Dakin's degradation approach. A 15 Ah commercial lithium-ion battery based on graphite/iron-phosphate technology was used for this purpose and aged at nine different conditions. In fact, the effect on aging of temperature (30, 45, and 60°C) and battery state of charge (30, 65, and 100 %) is studied. The Dakin's degradation approach based on chemical kinetics is used to establish the battery aging law. The aging rate expres-

sion is then deduced and found equivalent to Eyring's law. The aging rate increases exponentially with rising temperature and SOC. Model simulation is compared with experiment, literature and results are discussed.

Reliability assessment of ultra-short gate length AlGaN/GaN HEMTs on Si substrate by on-state step stress

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Step-stress experiments are performed to investigate reliability assessment of ultra-short gate AlGaN/GaN high electron mobility transistor (HEMT) on Si substrate. A methodology based on a sequence of step stress tests has been defined for in-situ diagnosis of permanent degradation. The same stress conditions were applied on HEMTs with different geometries. It is found no evolution of the drain current during non stressful steps. The value of the critical degradation voltage beyond which the stress drain current starts to decrease significantly is also found dependent on the stress bias conditions, the gate-drain distance and the gate length.

Requirements for the Application of ECUs in E-mobility Originally Qualified for Gasoline Cars

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Electronic control units (ECUs) are widely spread over the automotive industry with lots of applications. At this time more than 100 ECUs are used in a medium-sized vehicle. Development, test and qualification of ECUs are time and cost extensive. That is why they are often used in more than one generation and more than one model of vehicles. Present ECUs are developed and qualified for vehicles with combustion engines. Since the introduction of hybrid and fully electrical cars the requirements on the ECUs changed drastically. With respect to the engine ECUs temperature maxima is lower. On the other hand due to charging the batteries and other continuous voltage stresses, the time of operation (active and passive) is massively growing. The central question is: Is it possible to use ECUs qualified for gasoline car in electric cars without any reliability risks? To answer this question we start with a comparison of mission profiles of electrical cars and combustion engine cars. Based on the mission profiles we show the different requirements on the electronics robustness and use time. Afterwards we investigate the qualification process of an exemplary ECU from a combustion engine car and identify differences in comparison to the hybrid and fully electrical variant. As an example, a measurement of temperatures in a car driven under reasonably realistic conditions indicates the influence of the combustion engine on the thermal behaviour of the electronics as a key driver for failures. We provide a generic procedure that can be used for the design of future ECUs and compare it with expected temperature distributions in electric cars. Based on our results recommendations for the applicability of the use of existing ECUs in electric cars are discussed.

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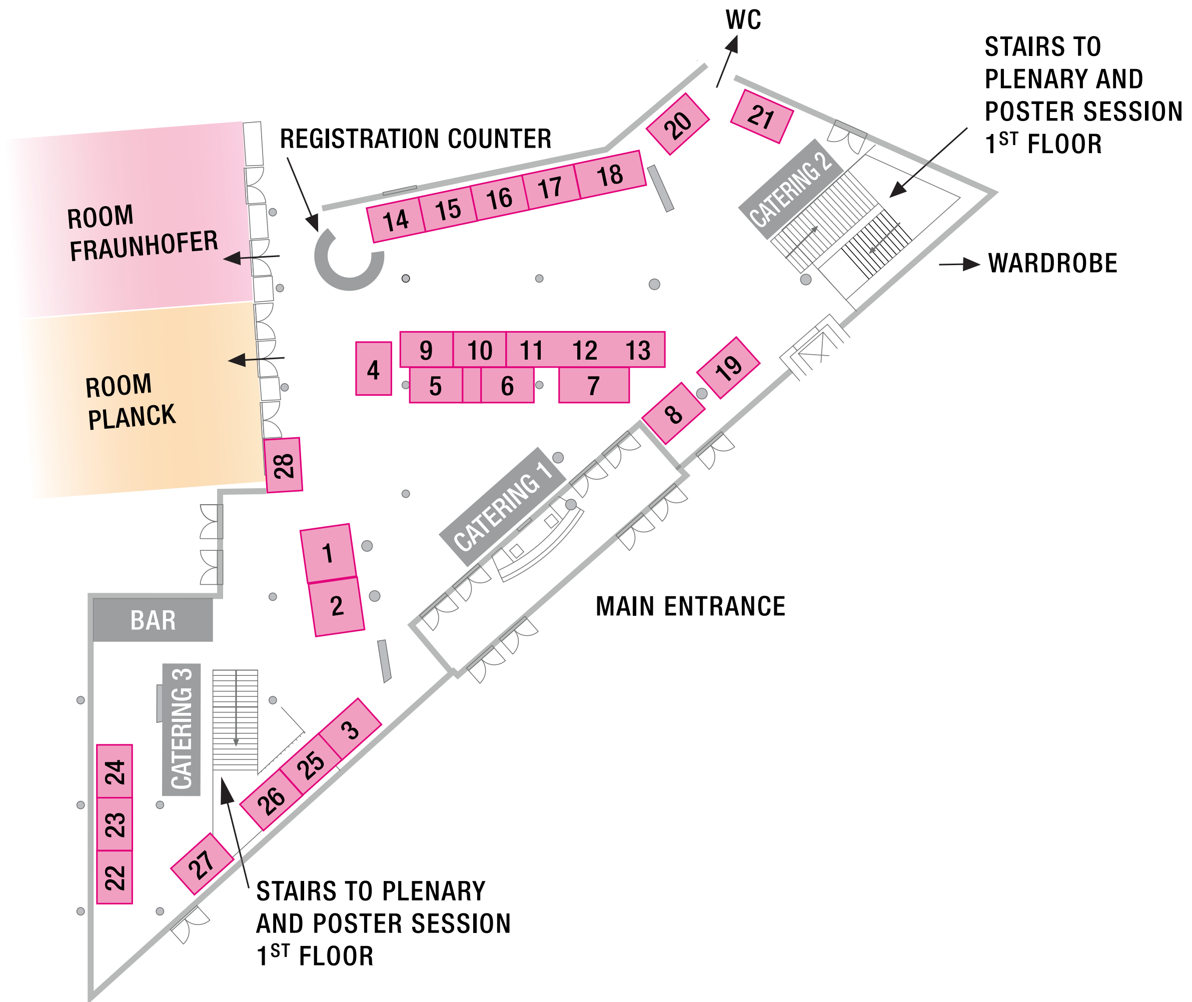

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Georg-Friedrich-Händel-HALLE

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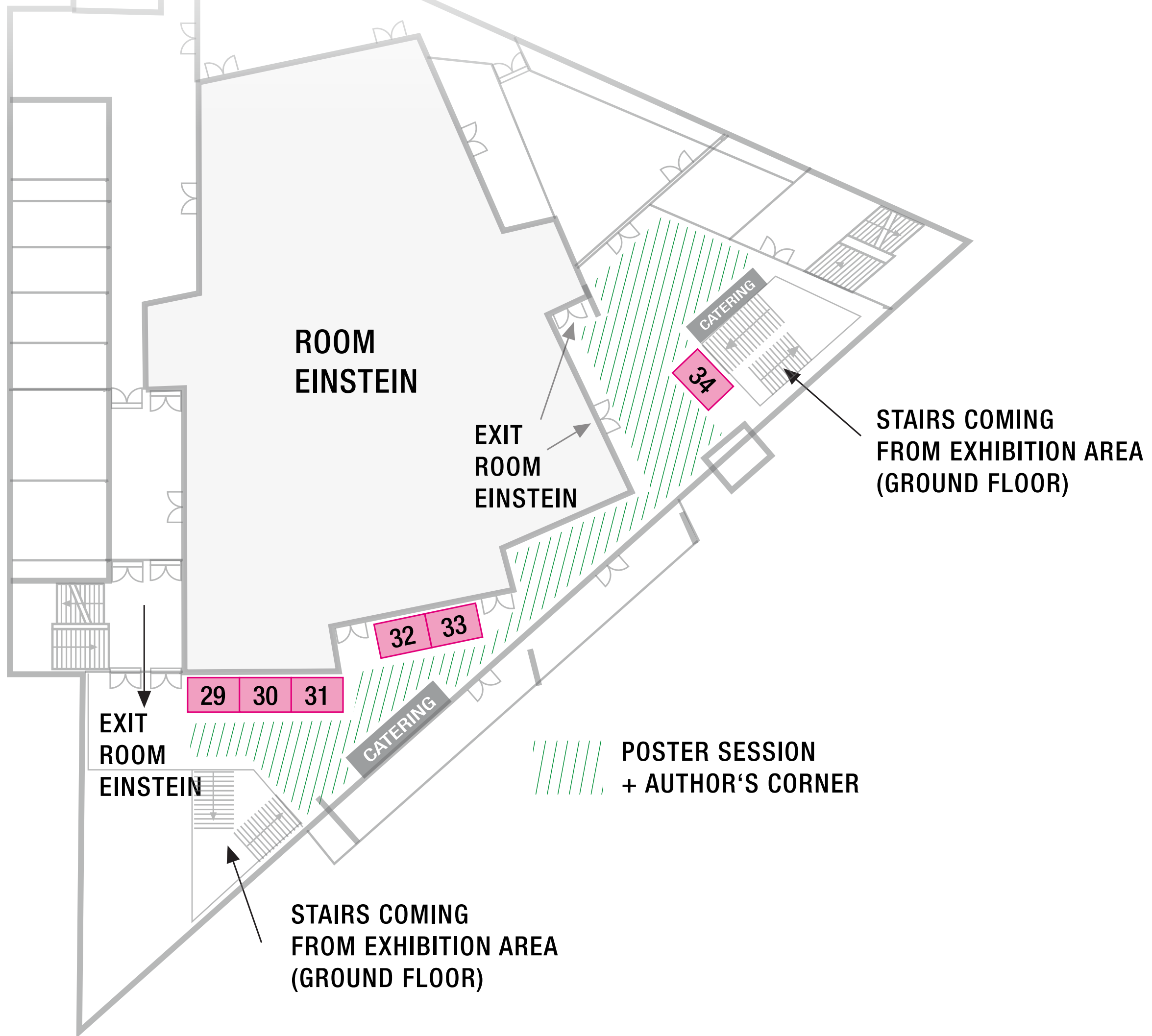

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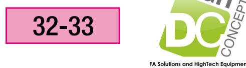
32-33 

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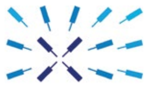
Exhibitors

We welcome our exhibitors of ESREF 2016 and their newest products and achievements within the electronics manufacturing chain from material supply, semiconductor and component manufacturing, packaging and assembly, service and instrumentation providers, system supply up to global OEMs.



Zurich Instruments

Zurich Instruments Ltd - Booth 1

Zurich Instruments makes lock-in amplifiers and phase-locked loops that have revolutionized instrumentation in the high-frequency and ultra-high-frequency ranges by combining frequency-domain tools and time-domain tools within each product. This reduces the complexity of laboratory setups, thus removing sources of potential problems and so allows researchers to focus on their experiments. The new MFLI instrument for low-frequencies makes these advantages available to a wider range of users.

PVA TePla Analytical Systems GmbH - Booth 2

Discover the world of Scanning Acoustic Microscopy

The unique characteristic of Scanning Acoustic Microscopy is its ability to non-destructively examine the interior of opaque materials with the resolution of optical light microscopy. New ways of thinking and visionary ideas are behind our successful concepts of trend-setting scanning acoustic microscopy technologies. In almost all fields of modern science and technology the demands for innovative, advanced solutions for non-destructive imaging with scanning acoustic microscopy have increased. PVA TePla Analytical Systems develops, produces and delivers scanning acoustic microscopes. Our unique transducers with frequencies from 3 to 2000 MHz extend imaging and analytical resolution beyond previously achievable limits. PVA Tepla Analytical Systems GmbH works successfully on the development and production of next generation scanning acoustic microscope.

CHECKPOiNT TECHNOLOGIES - Booth 3

Checkpoint Technologies is the world leader in optical based semiconductor failure analysis, fault isolation and circuit debugging. Checkpoint's LSM and emission tools lead the market in sensitivity and Resolution.

Hamamatsu Photonics - Booth 4

Hamamatsu Photonics is a worldwide leading manufacturer of opto-electronic components and systems. Among others we offer sensors and systems for spectroscopy (including

ultra fast), scientific-grade cameras, beam monitoring solutions, photon counting detectors and systems, photomultipliers, photodiodes, IR detectors.

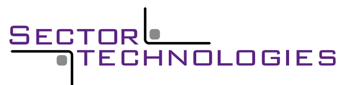
Products for the ESREF: Systems for failure localisation on integrated circuits based on emission microscopy (EMMI), laser based techniques (OBIRCH, OBIC, SDL, EOP) and lock-in thermography techniques (LIT)

Kleindiek Nanotechnik - Booth 5

Kleindiek Nanotechnik is a young, customer oriented high-tech company. With an innovative and powerful driving concept we are entering new space in micro- and nano-positioning. Due to miniaturisation in semiconductor technology, optics, micro-mechanics, medicine, gene- and bio-technology, highly precise positioning techniques are becoming increasingly important. Our products meet and exceed customer's requirements, offering them a new level of precision. Our customer-driven approach is focused on providing complete and innovative solutions for each of our market segments: researchers, industrial customers and enterprises. Our product develop-ment philosophy is the direct solution of the specific underlying problem. The simplicity, homogeneity and harmony of our designs guarantee maximum manoeuvrability and highest resolution while maintaining the smallest outer dimensions.

Imina Technologies SA - Booth 6

Imina Technologies, Exhibitor of ESREF 2016 Imina Technologies SA designs, manufactures and distributes complete lines of robotics solutions for electron and light microscopes. Using on a novel mobile motion technology, our robots for microscopes combine nanometer resolution of positioning, unprecedented ease-of-use and flexibility. Their ultra compact design provides high stability ensuring steady pose over long measurement sequence, while preventing sample damages. Our robots can be easily integrated onto optics based investigation tools or inside a SEM for micro- or nano-probing investigations. Overall, this enables FA Engineers to quickly gather data to understand the failure cause.



Sector Technologies - Booth 7

SECTOR TECHNOLOGIES is a European Company providing Sales and Maintenance Services on high tech Equipments for the

Semiconductor and Electronics laboratories. It proposes to its Customers a very large product portfolio for digital and power

semiconductors devices but also for electronic parts and board assemblies:

- Emission microscopy tools, Laser Scanning Microscopes and Laser Voltage Imaging
- Nanoprobing equipments
- Lockin Thermography and Infrared camera systems
- Circuit Modification tool by Focus Ion Beam
- 3D Xray tomography and microscopy
- Terahertz TDR systems
- Electrical test equipments
- Chemical and Laser decapsulation tools

EO Elektronen-Optik-Service GmbH - Booth 8

The EO Elektronen-Optik-Service GmbH has been known as a reliable and expert partner in sales and service of high-quality SEMs, FIB-SEMs, analysis and preparation systems for 35 years now. EO is the general agency and service base for several manufacturers such as TESCAN (SEMs), Cressington (coating systems), Technoorg Linda (ion mills) or Nanomechanics (nanoindenters) in German speaking countries and beyond. Our aim as an independent sales and service company is to offer our customers innovative and technically sophisticated equipment – like the TESCAN FERA or XEIA Xenon Plasma (UHR) FIB-SEM with 50x faster milling rate compared to conventional FIB-SEMs.

Allied High Tech Products - Booth 9

Technology for a Materials World

For more than 30 years, Allied has offered customers superior quality products for metallographic sample preparation and analysis, experienced technical assistance, and warm, friendly service. Our measure of success has always been your complete satisfaction.

Mesoscope - Booth 10

MESOSOCPE Technology is Nano Scale Probe Tip maker that has capability to manufacture the most advanced tips in the world.

Following as MESOSCOPE Technical road map and requesting from customers.

- MESOSCOPE starts to provide 35nm tip since 2011
- MESOSCOPE provides 20nm to one of the leading semiconductor companies since 2012 in Taiwan.
- MESOSCOPE provides the most advanced 10nm & 5nm Nano-Scale probe tips since 2013.
- MESOSCOPE develops Ultra CR5 for below 5nm device measurement since 2014.
- MESOSCOPE provides CR10 and CR5 for 10nm and 7nm devices measurement since 2015.
- MESOSCOPE will develop the most advanced CR2nm probe tip for below 5nm devices since 2016.
- MESOSOCPE is now the leading Nano-Scale probe tip and un-traditional probe tip designer and manufacturing provider in the world.

John P. Kummer GmbH - Booth 11-13

The John P. Kummer Group has served as a specialist distributor of instruments, used in the manufacturing of semiconductors, for several decades. Taking advantage of our long established relationships within the worldwide Industry, we bring the newest and most technologically advanced products to the European Microelectronics Community.

The focus of John P. Kummer Group combines equipment for failure analysis, reliability testing and process tools as well as specialty adhesives for use in advanced technology applications.

The fields of product applications are various as semiconductor, hybrids microelectronics, circuit/electronic assembly, medical devices and optical materials.

XYZTEC bv - Booth 14

XYZTEC is the technology leader in bond testing worldwide. The Condor Sigma is the most advanced bond tester on the market, providing leading customers with fully automated solutions. The Revolving Measurement Unit (RMU) enables continuous operation with up to six different test types on the one machine at forces up to 200kgf. Additionally, you can also choose for dedicated systems. XYZTEC is also unique in its high force products and next generation Sigma W12.

MASER Engineering B.V. - Booth 15

MASER Engineering is an independent engineering service provider for reliability test and failure analysis of micro-electronic components and systems. We offer advanced facilities for Integrated Device Manufacturers, Fabless and Labless IC manufacturers as well as the Original Equipment Manufacturing companies in our main lab in Enschede, The Netherlands.

Materials Analysis Technology Inc. - Booth 16

Materials Analysis Technology Inc. (MA-tek) is a leading laboratory in materials analysis. Accompanying with the fast growing pace of business development, MA-tek has successfully expanded to provide Failure Analysis and Reliability Testing. Now MA-tek has set up 7 laboratories and 1 sales office worldwide, providing around-the clock services in logistic support and technical services.

INTRASPEC TECHNOLOGIES - Booth 17

At Intraspec Technologies we sell the most advanced tools for Magnetic Microscopy, the Magma systems, offering a very wide range of localization techniques for all types static defects: shorts, resistive opens, dead opens and leakages.

Intraspec Technologies also offers services in the domain of reliability and failure analysis for electronic devices and systems. We are highly specialized in non-destructive techniques, such as Magnetic Microscopy, Lock-in Thermography and X-Ray Computed Tomography.

We are very active in the domain of 3D packaging and assembly thanks to our innovative, patented approaches: we keep performing multiple R&D activities for non-destructive localization techniques.

Part of our laboratories are at the French Space Agency (CNES), in Toulouse, allowing us to offer our customers the very latest analysis techniques.

Professional Maintenance Service & Wartungs GmbH

PM Professional Maintenance Service und Wartungs GmbH - Booth 18

PM Professional Maintenance- Service und Wartungs- GmbH is supplier of

equipment and service for semiconductor technology. We are acting in the sections of failure analysis, photolithography and

microelectronics. By cooperating with our valued partners we are able to offer a wide range of failure analysis equipment. We provide the full-spectrum of support to your company.

Exhibitors

point electronic GmbH - Booth 19

Point electronic GmbH supplies detectors, acquisition systems and microscope controls for SEM, TEM and Micro-analysers. The company was established in 1992 by a team from the Physics Department of the Martin Luther University to focus on digital image acquisition and analysis products for SEM, and has extended over time to cover complete electronics and software for electron-optic columns. Recent product developments include electron beam current instruments (EBIC and EBAC) and topographic imaging (3D).

The company is an established leader in development of custom microscopes for industrial applications and surface science. For this, the point electronic GmbH is employing its own platform of highly modular parts designed for highest performance and productivity. Alongside upgrades for new microscopes, point electronic GmbH provides SEM and TEM upgrade paths for customers that wish to maintain their instruments and workflows beyond the support period of their manufacturer.

As a vendor independent supplier, Point Electronic GmbH has completed over 2,000 installations on electron microscopes from all major manufacturers. Worldwide distribution and service is provided through a network of more than 30 partners. Point electronic GmbH is based in the Weinberg Science and Technology campus in Halle (Saale), Germany.

Serma Technologies - Booth 20

SERMA TECHNOLOGIES provides analysis, control, expertise and consulting services to major companies manufacturing/using electronic components, boards and systems on issues such as: development, technical choices, quality, reliability and security.

CASCADE MICROTECH - Booth 21

Cascade Microtech (NASDAQ: CSCD) is a leading supplier of solutions that enable precision measurements of integrated circuits (ICs) at the wafer level. Cascade Microtech delivers access to electrical data from wafers, ICs, IC packages, circuit boards and modules, MEMS, 3D TSV, LED devices and more. Cascade Microtech's leading-edge stations, probes, probe cards, advanced thermal subsystems and integrated systems deliver precision accuracy and superior performance both in the lab and during production manufacturing of high-speed and high-density semiconductor chips. We also offer both package-level and wafer- level reliability test systems which provide early analysis and lifetime predictions.

Mentor Graphics' Mechanical Analysis Division - Booth 22

Mentor Graphics' Mechanical Analysis Division is the synthesis of several long-standing successful companies within the computational fluid dynamics and electronics thermal fields.

Engaging with us gives you immediate access to a pool of specialist technical knowledge.

FloTHERM® perform thermal analysis, create virtual models and test design modifications, before physical prototyping.

FloTHERM XT® for seamless handling of complex MCAD geometry, with a familiar CAD look-and-feel, compatible for import of models from FloTHERM.

FloEFD™ is the only fully CAD embedded CFD software that really provides the frontloading benefit of simulation driven design in the native CAD environment of Catia V5, Siemens NX and PTC Creo.

MicReD® family of hardware and software products enables component and system suppliers to accurately and efficiently thermally test, measure and characterize integrated circuit packages amongst many other uses.

Our award winning T3Ster® software will be available at the show for demonstrations.

SmarAct GmbH - Booth 23

We at SmarAct develop, produce and distribute piezo-based high-performance micro- and nanopositioners, advanced control systems and micro-tools.

Furthermore, we manufacture complete miniaturized manipulation systems, ranging from single linear axes and rotary positioners to XY tables and compact 6D manipulators to multi-manipulator systems. Our microscopy products, which can be applied in normal pressure as well as in vacuum conditions, are used in a wide range of industries.

Our customers benefit from our over 10 years of experience in several scientific fields. This, accompanied by the entire value-added chain of development, production, distribution and a professional service, enables us to react fast to almost any of your demands, when it comes to customization and complexity.

PacTech - Packaging Technologies GmbH - Booth 24

PacTech consists of two business units:

1. Manufacturer of equipment for the Advanced Packaging and Microelectronics Industry
2. Provider of high-quality, subcontract Wafer Level Bumping and Packaging Services.

Out of its German based headquarter and their subsidiaries in California and Malaysia, the corporation supplies its outstanding solutions in these relevant business regions.

With more than 20 years of experience, PacTech is a prime manufacturer of leading-edge technology equipment and processes for the advanced packaging industry. PacTech designs, manufactures and supports solder jetting equipment, wafer-level solder ball transfer systems, wafer-level solder rework equipment, laser assisted flip-chip bonders and automatic plating tools for high volume electro-less Ni/Au and Ni/Pd/Au Under Bump Metallurgy (UBM) and Over Pad Metallurgy (OPM) through its global sales network. In its worldwide sales and application centers PacTech offers demonstration capabilities, including assembly of samples and prototyping under ISO certified production conditions.

It is PacTech's mission to provide the highest level of innovative technology solutions with an unparalleled degree of customer service orientation, corporate integrity and attention to its clients' individual technology demands.

RoodMicrotec GmbH - Booth 25

With 45 years' experience as an independent value-added microelectronics and optoelectronics service provider, RoodMicrotec offers a one-stop shopping proposition to fabless companies, OEMs and other business partners.

RoodMicrotec has built up a strong position in Europe with its powerful solutions. Its services comply with the highest industrial and quality requirements as demanded by the high-reliability/aerospace, automotive, telecommunications, medical, IT and electronics sectors.

Certified by RoodMicrotec' concerns certification of products inter alia to the stringent ISO/TS 16949 standard for suppliers to the automotive industry. The company has an accredited laboratory for testing and calibration activities in accordance with the ISO/IEC 17025 standard.

The value-added services include eXtended supply chain management from ASIC design via industrialization to mass production and shipment control, automotive competence centre, failure & technology analysis, qualification & monitoring burn-in, test- & product engineering, production test (including device programming and end-of-line service), ESD/ESDFOS assessment & training, quality & reliability consulting and total manufacturing solutions with partners.

RoodMicrotec has facilities in Germany (Dresden, Hannover, Nördlingen, Stuttgart), Bath(UK) and in the Netherlands (Zwolle).

Advantest Corporation - Booth 26

A world-class technology company, Advantest is the leading producer of automatic test equipment (ATE) for the semiconductor industry and a premier manufacturer of measuring instruments. The company's leading-edge systems and products are integrated into the most advanced semiconductor production lines in the world. The company also focuses on R&D for emerging markets that benefit from advancements in nanotech and terahertz technologies, and has recently introduced critical multi-vision metrology scanning electron microscopes and 3D imaging analysis tools for pharmaceutical and industrial applications. Founded in Tokyo in 1954 has subsidiaries worldwide.

Hitachi Power Solutions Co., Ltd. - Booth 27

Hitachi Power Solutions develops and provides our original Scanning Acoustic Tomographs and their transducers. Our products' lineup consists of FineSAT series, FS-Line series, Wafer-Line and ES-5100. The FineSAT series can be utilized for non-destructive testing of wide variety of electronic devices and materials not only in laboratories but also in mass-production lines. FS-Line series are optimum for large scale mechanical parts and materials such as sputtering targets. The Wafer-Line is an automated system for bonded Si wafers. ES-5100 can realize extremely high-speed testing on combination with phased array transducers. We can also provide optimum transducers from our wide variety of transducers to customer's samples.

Attolight AG - Booth 28

Attolight builds fully integrated cathodoluminescence systems with best-in-class collection efficiency and reproducibility. All products feature Attolight's proprietary quantitative cathodoluminescence technology. The company's products are used in FA laboratories, material research laboratories, and semiconductor industry. Major application fields include: R&D and reliability assessment for LEDs, lasers, power transistors, nano-electronic devices, and solar cells. The company also provides analytical services in its privately owned laboratory in Switzerland.

Oxford Instruments NanoAnalysis - Booth 29

Oxford Instruments NanoAnalysis provides leading-edge tools that enable materials characterisation and sample manipulation at the nanometre scale.

Used on electron microscopes (SEM and TEM) and ion-beam systems (FIB), our tools are used for R&D and failure analysis across a wide range of academic and industrial applications.

Fraunhofer CAM - Booth 30

Based on twenty years of experience in microstructure diagnostics and material assessment for semiconductor technologies, microelectronic components, microsystems and nano-structured materials, Fraunhofer CAM is tying the entire flow from non-destructive defect localization to high precision target preparation right up to cutting edge nanoanalytics supplemented by micro-mechanical testing, finite element modeling and numerical simulation.

Exhibitors

Gatan GmbH - Booth 31

Gatan, Inc. is the world's leading manufacturer of instrumentation and software used to enhance and extend the operation and performance of electron microscopes. Gatan products, which are fully compatible with nearly all electron microscope models, cover the entire range of the research process—from specimen preparation and manipulation to imaging and analysis. The Gatan brand name is recognized and respected throughout the worldwide scientific community and has been synonymous with high quality products and leading technology for more than 50 years. Gatan is headquartered in Pleasanton, California, U.S.A.

Digit Concepts - Booth 32+33

However, it is possible to be the best at understanding the actual needs for today's decapsulations of IC packages, the needs of the future, as well as the needs for those technologies that have been in existence for some time.

That is why we became a fabless company, which allows us to focus on the techniques of decapsulation, developing the equipment necessary for the task through collaboration with the leading manufacturers in each of the 4 ways of decapsulation. With 20 years of experience in IC decapsulation, a young international team of experts, and an understanding of the needs of our clients, we have become the leader in decapsulation in just a few years.

Since 1992 DIGIT CONCEPT has been supplying tools for semiconductor Failure Analysis. DIGIT CONCEPT invests considerable time and effort in the development of new and innovative techniques for the semiconductor industry, but also in developing new techniques and improvements for existing Technologie.

Micro to Nano - Booth 34

Micro to Nano, based in Haarlem, Netherlands, specialises in consumable and supplies for SEM, FIB, TEM and AFM.

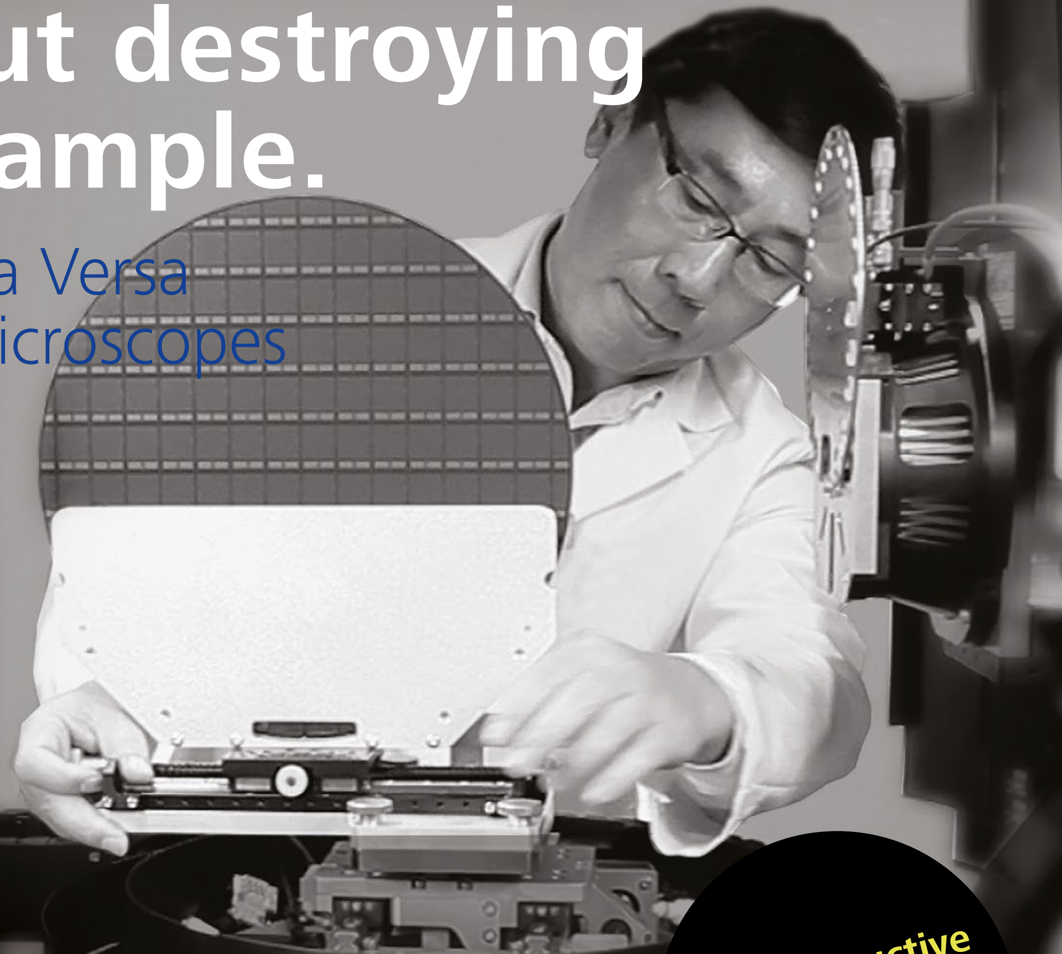
Many of the microscopy consumables we offer, are designed by us and manufactured for us. This enables us to supply our customers quickly with innovative, high quality products coupled with competitive pricing. Micro to Nano ships directly to all European countries from our facilities based in Haarlem, NL. All information about the complete product range is available from the www.microtonano.com website supported by state of the art e-commerce.

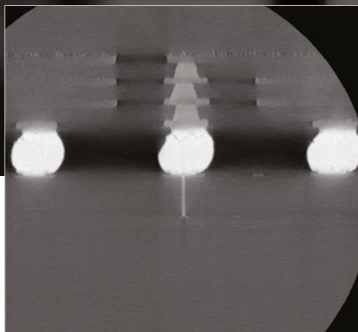
Core product lines are calibration standards, SEM sample holders, TEM & FIB grids, specimen supports & substrates and sample preparation tools. We also design and manufacture custom SEM sample holders.

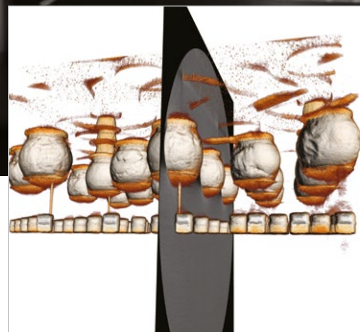
Explore and discover the innovative, unique and high quality products at: www.microtonano.com

Cross-sectioning without destroying your sample.

ZEISS Xradia Versa
3D X-ray Microscopes







Virtual cross section **Reconstructed 3D dataset**
Acquired by ZEISS Xradia 520 Versa 3D X-ray microscope.

Identify and visualize failure locations in advanced packaging technologies.
Interconnect levels are increasing while pitch is shrinking. Defects can be missed in the standard failure analysis process of physical cross sectioning. Stress relief produced by destructive sample preparation may obscure the original root cause by inducing further crack initiation or propagation, introducing debris, and damaging soft materials.

ZEISS Microscopy offers 3D X-ray microscopes (XRM) that provide submicron resolution and contrast for a wide variety of electronics samples, regardless of sample size. With ZEISS XRM, resolution does not degrade as sample sizes increase so whether you are visualizing a 10 mm flip chip package or a 300 mm wafer, you can maintain close to one-micron resolution for any point on your sample.

www.zeiss.com/manufacturing-assembly

About Halle

Welcome to Halle (Saale) – a town packed with history. It is home not only to the largest timbered house in Europe and the third-biggest glockenspiel in the world but also the oldest German chocolate factory.

Halle with its 232.000 inhabitants is an economic and educational center in central-eastern Germany. It looks back at a long and prosperous history. Halle's early history is connected with the harvesting of salt since the Bronze Age (2300–600 BC). The name Halle originates from an early Germanic or Celtic settlement – hal or halla – which is the Brythonic (Welsh/Breton) word for salt (cf. salann in Irish). The name of the river Saale also contains the Germanic root for salt.

The town itself was first mentioned in AD 806. Since then, it has grown over the centuries to become a unique cultural point of interest. Many epochs have left their characteristic imprints. The New Residence, the Cathedral and Moritzburg castle in the North West of the older part of the town bear witness to the late middle ages and the age of the Reformation. During the early 16th century this was the residence of Cardinal Albrecht, the Archbishop of Mainz and Magdeburg. He was not only one of Martin Luther's most powerful rivals, but also a passionate art lover. It is, thus, fitting that his former residence now houses an arts museum which is recognised of being of national importance.

Later on, Halle played a leading role in the realm of science. In 1694, the university opened its gates and the town became a center of one of the most influential intellectual movements of the age – Enlightment. Christian Wolff was an important proponent of rationalism. He influenced many German scholars, such as Immanuel Kant. Christian Thomasius was at the same time the first philosopher in Germany to hold his lectures not in Latin, but German. He contributed to a rational programme in philosophy but also tried to establish a more common-sense point of view, which was aimed against the unquestioned superiority of aristocracy and theology. The institutionalisation of the local language (German) as the language of instruction, the prioritisation of rationalism over religious orthodoxy, new modes of teaching, and the ceding of control over their work to the professors themselves, were among various innovations which characterised the University of Halle, and have led to its being referred to as the first "modern" university.

Apart from rigorous science, beautiful arts have always been at home in Halle. Georg Friedrich Handel was born here and it was here that he took up his first post as a church musician. The German-American expressionist painter Lyonel Feininger worked in Halle on an invitation by the city from 1929 to 1931. Today, the Burg Giebichenstein Art Academy is one of Germany's leading places of education for graphic designers, sculptors and designers.

The history of the old salt town is visible everywhere. For example, there is now a museum in the house Handel resided in, and, in the market-church the original death-mask of Martin Luther is on display.

Social Programme

Monday, September 19, 2016 | 16:45–19:00 | Exhibition Area

Exhibition Opening / Get-together

A welcome get-together for all conference participants and exhibitors will be held Monday afternoon in the exhibition area of the conference venue. Do not miss this opportunity to network with other attendees and the chance to have a first look through our large exhibition.

Tuesday, September 20, 2016 | 18:30–20:30 | Art Museum, Castle Moritzburg

Drinks Reception

Castle, ruin and museum… more than 500 years of rich history in just one building – and a modern art exhibition on top. Join us at castle Moritzburg, the former residence of the Archbishops of Magdeburg, for some drinks and a leisurely stroll through its exhibition.

There will be a total of four guided tours, all starting at 18.30 with a maximum number of 30 participants each. Three of these tours will be held in English and a fourth will be in German.

These tours are free, but participants need to register since there is only a limited number of space on each of them. To register, please come to registation desk before 16.00 on the day of the reception.

Should you want to stroll through the exhibition on your own, you are more than welcome to do so. Please note that there are no drinks or food allowed within the exhibition area.

Wednesday, September 21, 2016 | 18:45–19:45 | Church of St. Ulrici

Concert

Halle has a long musical tradition dating back well into the middle ages. One of the bearers of this tradition is the "Stadtsingechor" – a boys' choir – which is celebrating its 900th anniversary in 2016.

They will join us for a concert in the Church of St. Ulrici and are looking forward to entertain you with a selection of musical works by Handel und Telemann.

Wednesday, September 21, 2016 | 20:00–22:00 | Dormero Hotel Rotes Ross

Gala Dinner

The conference gala dinner will take place in the Dormero Hotel Rotes Ross, on Wednesday, September 21st, 2016, at 20:00.

ESREF 2016 – The APP for your mobile device

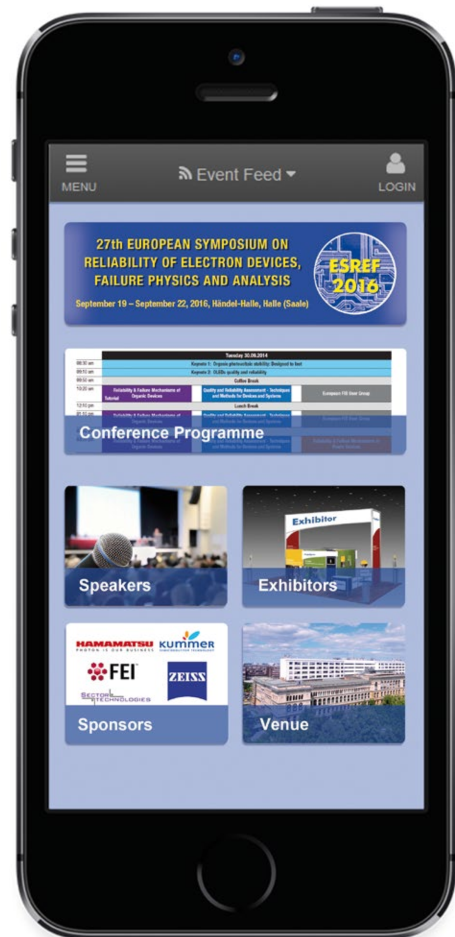
Visit

https://eventmobi.com/esref2016/

on you smartphone, tablet or personal computer

- to create and save your personal programme
- to get the full up-to-date information
- to search for speakers, presentations, and more
- to download the proceedings
- to connect with conference visitors, speakers, exhibitors
- to find your way around the venue or to the social event
- to receive instant messages about current conference events
- to experience one of the latest features of ESREF 2016

Works on Android 4.1, BlackBerry OS 10, iOS 6 and later, as well as on all mainstream desktop browsers.



Conference Registration

The conference registration fee includes admission to all conference sessions, the poster session and the exhibition. Regular participants (including speakers, poster presenters, session chairs and registered exhibitors) have free admission to all evening events. For accompanying persons, extra tickets can be purchased for these events.

Door Registration Fees

- Regular Fee . . . . .850,00 €
- VDE Member*. . . . . . .750,00 €
- Students* . . . . .550,00 €

Presenting Author Regular Registration fees apply

** Participants applying for the membership fee or student fee must provide a copy of their membership / student card at registration.*

Conference Language and proceedings

The offical language of all presentations is English. All conference papers are available for download through the ESREF conference app and will be published as a special issue of "Microelectronics Reliability".

Contact Information and Assistance during the Conference

Do not hesitate to approach us at the registration desk during the conference if you have any questions or requests.

Registration On-Site:

The registration desk on site will be open at the following office hours:

- Monday, September 19, 2016 . . . . . . 11:00 – 20:00
- Tuesday, September 20, 2016 . . . . . . 07:30 – 18:00
- Wednesday, September 21, 2016. . . . 07:30 – 17:30
- Thursday, September 22, 2016. . . . . . 07:30 – 15:30

Exhibition Hours:

- Monday, September 19, 2016 . . . . . . 16:40 – 20:30
- Tuesday, September 20, 2016 . . . . . . 08:00 – 18:00
- Wednesday, September 21, 2016. . . . 08:00 – 19:00
- Thursday, September 22, 2016. . . . . . 08:00 – 16:00

This event is organized by VDE Conference Services. Please contact with any questions regarding the registration, attendance and submission of papers:

VDE e.V.

Conference Services
Jasmin Kayadelen
Stresemannallee 15
60596 Frankfurt am Main / Deutschland
E-Mail: jasmin.kayadelen@vde.com
Mobil: +49 151-14 07 39 47

Local Organization:

Fraunhofer Institute for Microstructure of Materials and Systems (IWMS)
Center for Applied Microstructure Diagnostics (CAM)
Katja Stock
Walter-Hülse-Strasse 1
06120 Halle (Saale)
Phone: +49(0)345-5589-140
Fax: +49(0)345-5589-101
E-mail: Katja.Stock@imws.fraunhofer.de

Wifi at the conference

Wifi will be provided complementary at the conference location.

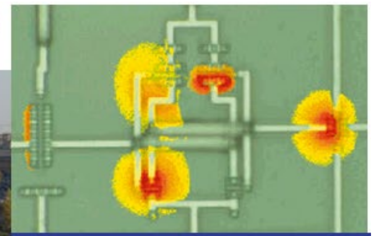
Network: ESREF 2016

Password: welcome!

Wifi will be sponsored by

Notes

28th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis



September 25-29, 2017
Cité Mondiale du Vin,
Bordeaux (France)

1st CALL FOR PAPERS

ESREF 2017, the 28th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, will take place in Bordeaux (France) from 25th to 29th September 2017.

This international symposium continues to focus on recent developments and future directions in Quality and Reliability Management of materials, devices and circuits for micro-, nano-, and optoelectronics. It provides a European forum for developing all aspects of reliability management and innovative analysis techniques for present and future electronic applications.

organized by :

with the technical co-sponsorship of :

IEEE - Electron Devices Society
IEEE - Reliability Society
ANADEF - The French FA Society
EUFANET - European Failure Analysis Network
ECPE - European Center for Power Electronics

A word from the conference chairs

ESREF 2017 will be held in Bordeaux – European capital for optical and laser engineering. The Laser Mégajoule is one of the most powerful lasers in the world. Some of the largest companies working for the aeronautic industry are located around Bordeaux. Falcon private jets are built there as well as the French military aircrafts, the Airbus A380 cockpit, the boosters of Ariane 5...

Bordeaux is located at the very heart of Southern Europe. It is part of the UNESCO World Heritage List, and classified as "City of Art and History".

The University of Bordeaux is leading the "Initiative of Excellence" (Idex) program in association with national research organizations and higher educational institutes. 53 000 students take benefit of this multidisciplinary and international framework of the "Investments for the Future" program.

Hosting ESREF 2017 in this rich environment is a great opportunity since reliability in these particular applications is a very hot topic with strong challenges such as zero ppm failure and harsh environments.

For this 28th edition, in addition to the core topics of the conference, we would like to involve the major actors of aeronautics, space and embedded systems industry to provide specific topics such as radiation hardening, very long-term reliability, high/low temperature challenges, obsolescence and counterfeit issues, wide band gap power devices for the more electric aircraft and other embedded system applications. ESREF 2017 is also hosting several workshops (EFUG, EUFANET, POWER…) and welcomes new ones related to these specific topics.

We are looking forward to welcoming you for a memorable experience!

Nathalie LABAT
ESREF 2017 Chair

François MARC .
ESREF 2017 Vice-Chair

LOCATION OF THE CONFERENCE:

CITE MONDIALE du VIN - BORDEAUX
20 quai des Chartrons - 33000 BORDEAUX – France
(20 min from the international airport of Bordeaux-Mérignac)

SUBMISSION GUIDELINES

The deadline for the submission of summaries is **March 12, 2017**. **The four-page extended** summaries must include a title page with a five-line abstract, the complete address, the fax number and e-mail address of the corresponding author and the preference for oral or poster presentation. Please note that abstracts and papers must be in English.

Authors are requested to upload an electronic file (in Adobe Acrobat PDF or WORD format) of the summary at:

http://www.esref.org

DEADLINES

12 March 2017 — **Submission of summary**
21 April 2017 — **Notification of acceptance**
21 May 2017 — **Submission of extended paper**

Elsevier Ltd will publish the ESREF 2017 proceedings as a special issue of the Microelectronics Reliability journal.

25 June 2017 — **Upload of final paper to the online Elsevier Editorial System (EES)**

Map of Halle

Tuesday, September 20, 2016 | 18:30 – 20:00
Drink Reception and Museum Tours

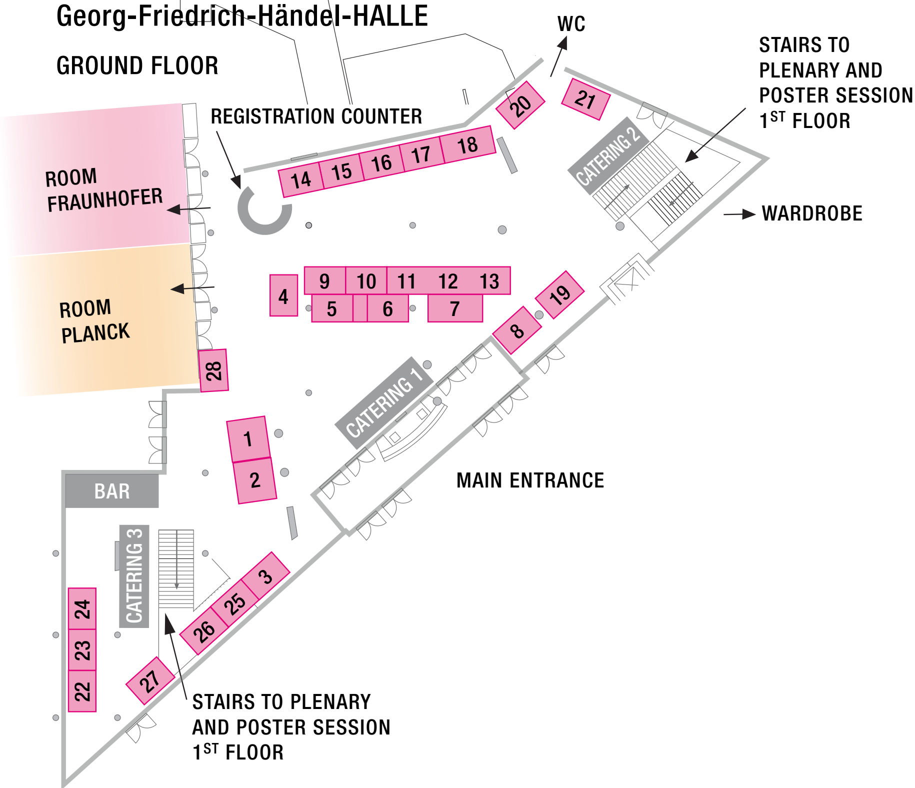
Conference Venue

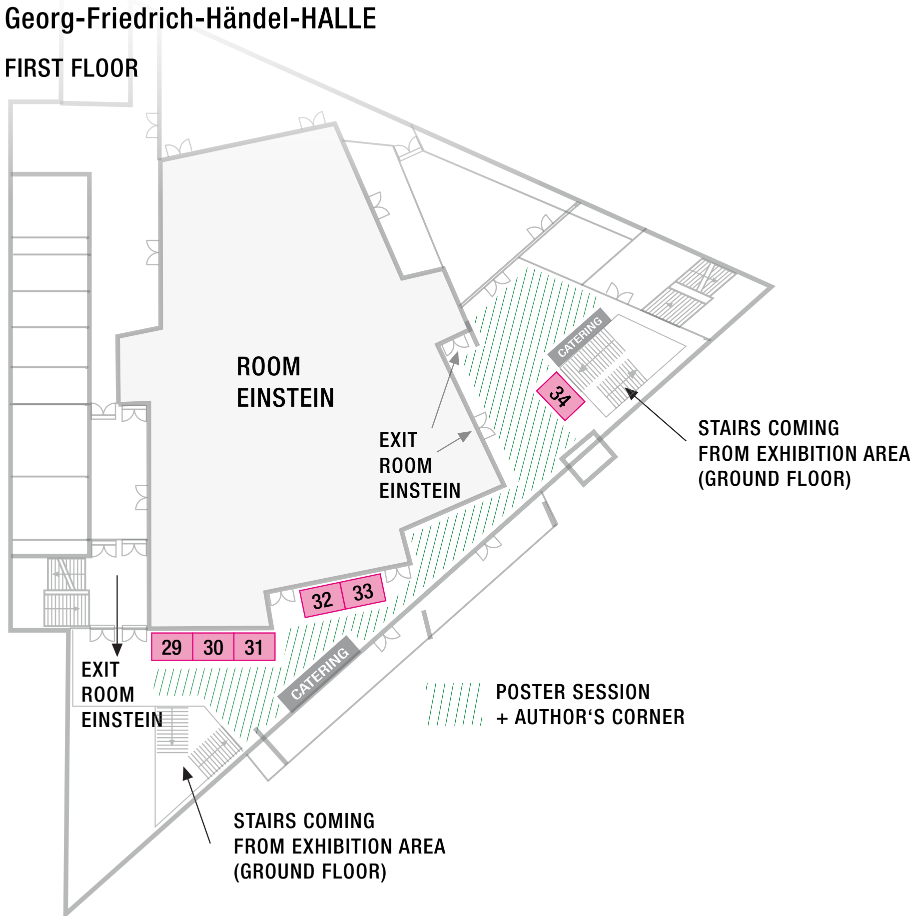
Wednesday, September 21, 2016 | 18:30 – 20:00
Concert at Church of St. Ulrici

Wednesday, September 21, 2016 | 20:00 – 22:30
Gala Dinner at Hotel "Rotes Ross"

Main Train Station

Conference Floorplan Overview





ESREF 2016 – Technical Programme Overview

Time	Room: Planck	Room: Einstein	Room: Fraunhofer
	Monday, 19th September 2016		
11:00 – 13:00	**Registration**		
13:30	Opening Session with Keynotes 1+2		
15:20	Coffee Break		
15:40	Opening Session - Exchange Papers		
16:40	Exhibition Opening / Get-together / Drinks Reception		
	Tuesday, 20th September 2016		
08:30	**Session 3B:** Power Devices Reliability: Tutorial	**Session 3A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Tutorial	**Session 3C:** Progress in Failure Analysis Methods: Laser probing techniques
09:30 / 09:50	**Session 4B:** Power Devices Reliability: Metallization and Interconnects	**Session 4A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories – Part 1	**Session 5:** Exhibitor Workshop: Defect Localization and Nanoprobing
10:50	**Coffee Break / Exhibition**		
11:10	**Session 6B:** Power Devices Reliability: SiC Devices	**Session 6A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories – Part 1 (continued)	**Session 6C:** Progress in Failure Analysis Methods: Nanoscale failure analysis
11:50		**Session 7:** Exhibitor Workshop: Sample Preparation	
12:50	**Session 8:** Poster Session for Tracks B / D / E /G		
13:50	**Lunch Break / Exhibition**		
15:10	**Session 9B:** Power Devices Reliability: Passives	**Session 9A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Logic ICs and Memories – Part 2	**Session 9C:** EFUG - Workshop (Part 1)
15:50	**Session 10:** Exhibitor Workshop: Failure Analysis		
16:50	**Coffee Break / Exhibition**		
17:10	**Session 11B:** Power Devices Reliability: Testing Methods	**Session 11A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Space and Radiation	**Session 11C:** EFUG - Workshop (Part 2)
18:30	**Drinks Reception – Castle Moritzburg**		
	Wednesday, 21st September 2016		
08:30	**Session 12A:** Semiconductor Reliability & Failure Mechanisms: FD-SOI and RRAM	**Session 12B:** Failure mechanisms and precautions in plug connectors and relays: Tutorial	**Session 12C:** Students Workshop
09:30 / 09:50		**Session 13:** EUFANET/CAM-Workshop “Automotive Electronics Systems Reliability” (Part 1)	**Session 14:** Reliability and Failure Mechanisms of special photonics and LED Devices: LED systems
10:50	**Coffee Break / Exhibition**		
11:10	**Session 15:** Panel Discussion + Keynote 3		
13:50	**Lunch Break / Exhibition**		
14:50	**Session 16A:** Semiconductor Reliability & Failure Mechanisms: BTI	**Session 16B:** EUFANET/CAM-Workshop “Automotive Electronics Systems Reliability” (Part 2)	**Session 16C:** Reliability and Failure Mechanisms of special photonics and LED Devices: LED; laser diodes and VCSELs
15:30	**Session 17:** Exhibitor Workshop: Reliability Testing and Failure Analysis		
16:30	**Coffee Break / Exhibition**		
16:50	**Session 18A:** Semiconductor Reliability & Failure Mechanisms: Miscellaneous	**Session 18B:** EUFANET/CAM-Workshop “Automotive Electronics Systems Reliability” (Part 3)	**Session 18C:** Progress in Failure Analysis Methods: Novel non-destructive testing
19:00	Concert / Ulrichskirche		
20:00	Gala Dinner / Hotel Rotes Ross		
	Thursday, 22nd September 2016		
08:30	**Session 19A:** Reliability & Failure Mechanisms of MEMS and sensors	**Session 19B:** Reliability & Failure Mechanisms in Packages and Assembly: Tutorial	**Session 19C:** Reliability & Failure Mechanisms of Wide Bandgap Devices: Tutorial
09:30		**Session 20A:** Reliability & Failure Mechanisms in Packages and Assembly: Moisture and corrosion related studies	**Session 20B:** Reliability & Failure Mechanisms of Wide Bandgap Devices: Microwave devices
10:50	**Coffee Break / Exhibition**		
11:10	**Session 21A:** Quality and Reliability Assessment – General Techniques and Methods for Devices and Systems: Miscellaneous	**Session 21B:** Reliability & Failure Mechanisms in Packages and Assembly: Reliability and Modelling	**Session 21C:** Reliability & Failure Mechanisms of Wide Bandgap Devices: GaN power devices and deep level transient spectroscopy
12:50	**Session 22:** Poster Session for Tracks A / C / F / H and Exhibition		
13:50	**Lunch Break / Exhibition**		
15:10	**Closing Ceremony**		